Department of Electrical and Computer Engineering, UC SANTA BARBARA

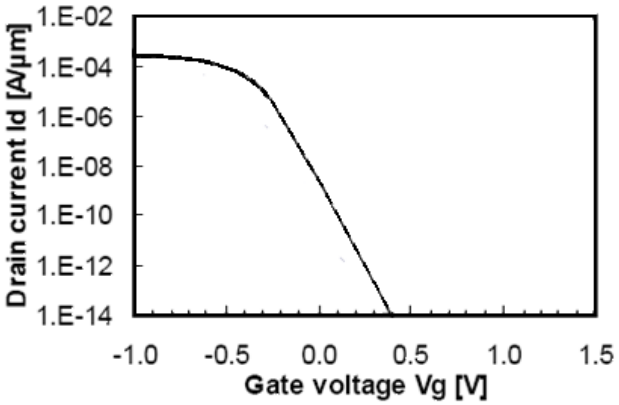
ECE124A VLSI Principles

Homework #4

Due Date: Nov. 7 Wed by 5:00pm

For all the questions, the dielectric constant of SiO_2 is $\varepsilon/\varepsilon_0$=3.9, where ε_0= 8.85×10^{-12} F m^{-1} is the vacuum dielectric constant. The dielectric constant of Si is $\varepsilon_s/\varepsilon_0$=11.7.
e =1.6×10^{-19}C; kT/e = 26mV.

Problem 1 MOSFET Threshold Voltage (1)



1. For the Id-Vg curve in the figure below, show linear and velocity saturation regions.
2. Find out subthreshold swing. Is this ideal value of sub threshold slope? If yes why? If no, what is ideal value of subthreshold swing?
3. If the threshold voltage is defined at a constant current of 10^{-7} A/μm, determine the threshold voltage of the device.
4. Read the paper "Threshold voltage definition and extraction for deep-submicron MOSFETs" by X. Zhou, K. Y. Lim and W. Qian, Solid State Electronics, 2001. (On the course website). If we use the maximum-gm method to define threshold voltage, would the new V_T be higher or lower compared to V_T in 3?
5. What are the main reasons for introduction of new threshold voltage definition in short channel devices compared to long channel devices?

Problem 2 MOSFET Threshold Voltage (2)

Consider an aluminum-SiO_2-Si MOSFET structure, where the Si channel is n-type with doping concentration N_D.

The work function difference between aluminum gate and channel is Φ_{GC} = -0.35V.
The oxide thickness is t_{ox} = 65nm and positive (trapped) charges density in oxide is $Q_{ox}/e=5\times10^{10}cm^{-2}$.

Design the semiconductor doping concentration N_D to yield a specified threshold voltage V_{TP} = - 1.0 V.

Hint: you need the formula for depletion charge.

Problem 3 MOSFET Substrate Bias Effect

An NMOS device has the following parameters:

N+ poly gate (work function difference between gate and channel is Φ_{GC} = -1.06V);
P-doped channel with doping concentration $Na=10^{15}$ cm^{-3}; $n_i=1.5\times10^{10}$cm^{-3}.

SiO_2 thickness is t_{ox} = 40nm;
Positive charges in oxide: $Q_{ox}=6.48\times10^{-9}$ C/cm^2.

1. Determine V_T.
   Hint 1: calculate substrate Fermi potential φ_F first.
   Hint 2: Inversion layer can be formed even in zero gate voltage due to the positive charges in oxide and the work function difference.
2. Is it possible to apply a V_{SB} voltage such that V_T=0? If so, what is the value of V_{SB}?
   Be careful about the sign of φ_F.

Problem 4 MOSFET Current Equation

I-V data of a short channel NMOS are measured and listed in the table. Given that the saturation voltage is V_{DSAT}=0.6V and $\beta=\mu C_{ox}$W/L= 100μA/V^2, calculate:

Data	V_{GS} (V)	V_{DS} (V)	V_{BS} (V)	I_D (μA)
1	2.5	1.8	0	1812
2	2.0	1.8	0	1297
3	2.0	2.5	0	1361
4	2.0	1.8	-1.0	1146
5	2.0	1.8	-2.0	1039

1. V_{T0} (threshold voltage with no substrate bias);
2. λ (channel length modulation coefficient)
3. γ (substrate bias coefficient)
4. φ_F (substrate Fermi potential)

Problem 5 MOSFET Capacitance

The figure shows the layout of an NMOS transistor with substrate doping $Na=2\times10^{16}$ cm^{-3}; source/drain doping $Nd=6\times10^{19}$ cm^{-3}; SiO_2 thickness t_{ox} = 8nm; junction depth X_j=0.4μm; effective mobility μn=550 cm^2/Vs.

Assume gate overlap L_D is 0 and the substrate is grounded (V_B=0).

1. What is the maximum drain-to-bulk capacitance C_{DB}? The drain voltage swings between 0V and 2V.
   Hint: $C_{DB}=C_{j0}/(1-V_D/V_0)^m \le C_{j0}$, where C_{j0} can be calculated using depletion region capacitance formula.
2. Now assume the substrate is biased at -1V, and grading coefficient m=0.5. What is the new maximum C_{DB}?