ECE124A VLSI Principles

Homework #6

Due Date: Dec. 7 Fri by 5:00pm

Problem 1 Pass Transistor Logic

The function F = A XOR B is to be implemented in pass transistor logic according to figure a below.

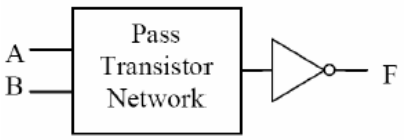


Figure a

(a) How would you implement the pass transistor logic with NMOS-only switches? Assume both true and complimentary input signals are available.

(b) What is the minimum voltage at which this circuit will operate correctly (and why)? For the NMOS switches use V_{TH0} = 0.5V, γ = 0.4V, $2\varphi_F$ = -0.6V. Assume that the inverter has an ideal VTC that switches when its input is at $V_{DD}/2$. (You may need MATLAB)

(c) A level restoring PMOS transistor is now added as shown in the figure b below. If the level restoring PMOS transistor has V_{TH0} = -0.5V and W/L = 4 and $\mu_N = 3\mu_P$, what is the minimum W/L for the NMOS switches in order for the circuit to function properly? (Assuming all inputs are driven by ideal voltage source)

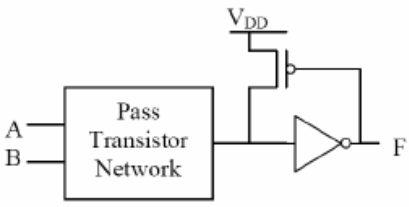
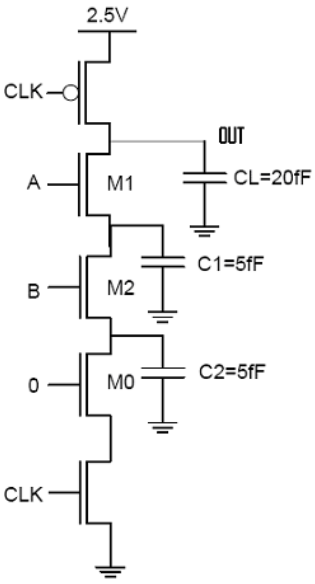


Figure b

Problem 2 Dynamic CMOS

(a) Assuming that all inputs of the circuit shown below are initially 0 during the pre-charge phase and that all internal nodes are at 0V, calculate the voltage drop on V(out), if A changes to V_{DD} during the evaluate phase. It is given that Vtn0=0.5V, $|2\varphi_F|$= 0.6V and γ=0.4V$^{0.5}$. Hint: Don't forget the body effect.



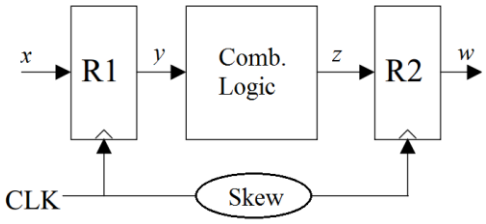
(b) Now calculate the voltage drop on V(out) if both A and B change to V_{DD} (under the above conditions).

(c) If we do not want V(out) to drop more than 10% V_{DD}, how big should we make C_L?

(d) What is the maximum number of transistors that can be connected in series to M1 and M2 (including M1 and M2, excluding M0) if the output should not fall below 0.5V during the evaluate phase? Assume that each one of the new transistors has the same intrinsic capacitance (to ground) as M1 and M2 (C=5fF).

(e) Now there is a static CMOS inverter with V_M=1.5V attached to V0. Also, node V has a constant current leakage of 1nA. Ignore charge-sharing (C1 = C2 = 0F), how long could V(out) stay valid, such that the inverter will output the correct result?

Problem 3 Sequential logic



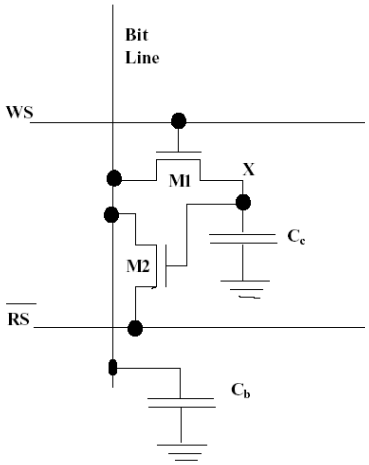
In the circuit below, setup time, hold time, propagation delay and contamination delay of flip-flops (R1, R2) are 1ns, 0.7ns, 2ns and 0.8ns, respectively. The maximum delay of the combinational logic is 3.3ns. Suppose there is a positive clock skew of 0.3ns.

i) draw a time diagram for signals x, y, z and w;

ii) calculate the minimum clock frequency;

iii) calculate the minimum delay allowed for the combinational logic.

Problem 4 DRAM



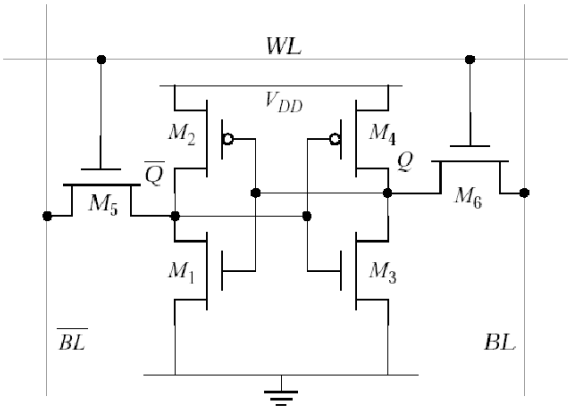
The 2-T memory cell shown below uses 2 identical transistors with W/L = 0.4/0.25. Separate lines are provided for the read select (RS) and write select (WS) signals, which both switch between 0 and 2.5V. The Bit Line is precharged to Vdd/2 prior to a read. A write is done by pulling the bit line either to Vdd or to GND. Ignore the body effect and channel-length modulation. (γ=0; λ=0). You may assume that kn' = 115 uA/V^2 , Vdd=2.5, Vt = 0.4.

i) Explain the operation of the memory. Draw waveforms for BL, WS, and RS and Vx for reads and writes of both '1's and '0's.

ii) Determine maximum current through M2 during a read operation.

iii) The bit line is connected to a single-ended sense-amp, which switches when the voltage reaches Vdd/2 - 200mV. Compute the time required to read a data bit. Assume that C_c=10fF and C_b=2pF. (You may need MATLAB)

Problem 5 SRAM



A generic SRAM cell is shown below. At first, it seems like the margins in such a memory cell should be good, since it contains two CMOS inverters, which we know have large margins. However, the problems are associated with those access devices connected to the cell. When cell is not accessed, it has great margins; when access devices are on, they act like load devices. Capacitance on bit lines is large enough to act like a voltage source.

(kn' = 115 uA/V^2 , kp' = 30 uA/V^2, $Vdsatn$=0.63V, $Vdsatp$=0.7V, Vtn=0.4 Vtp=-0.4)

i) Read Operation

Assume first that node Q is in the "1" state, we further assume that both bit line are precharged to VDD, 2.5V, before the read operation is initiated. Suppose that noise margin of inverter is 0.7V.

Please find out the dimension ratio of M5 and M1 to avoid "read upset" under the WORST case. (Note: During a correct read operation, the values stored in Q and *Q'* are transferred to the bit lines by leaving BL at its precharge value and by discharge *BL* through M1 – M5. A careful sizing of the transistors is necessary to avoid accidentally writing a "1" into the cell. This type of malfunction is called "read upset"). (You may need MATLAB)

ii) Write operation

Assume that a "1" is stored in the cell. A "0" is written in the cell by setting *BL* to "1" and BL to "0". The noise margin is given as in part a). What is the ratio of M4 and M6 to guarantee a successful write operation? (You may need MATLAB)

Problem 6 Datapath

A Carry-Bypass Adder consists of n 4-bit ripple-carry adders, as shown in the figure. P is carry propagation signal. Assume the delay of 1-bit adder is *Ta*=2ns (delay from {A, B, Cin} to {S, Cout}), and the time of generation of carry bypass propagation signal is *Tp*=2ns (delay from {A, B} to P). AND gate delay is *T1*=1ns while OR gate delay is *T2*=1ns. What is the time needed for the whole adder to finish the 4n-bit sum?