LAB 4 – INVERTER VTC; CMOS SIZING AND DELAY

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All the highlighted bolded underlined texts are what you should put in your report.

Use 65nm CMOS transistor model from http://ptm.asu.edu/

PREREQUISITE

Understanding of Lecture 11.

TASK I – INVERTER VTC

STEP 1 - VTC

Draw the VTC curves of minimum size inverter in 65nm technology with V_{DD} =1.5V.

Write (in text editors) or Generate (by SUE) the netlist.

Simulate it using HSPICE, and then

Plot the VTC using CosmoScope

STEP 2 - V_T VARIATION

Increase the threshold voltage of NMOS transistor by 0.15V and decrease the (absolute value) threshold voltage of PMOS by 0.2V.

Plot the VTC using CosmoScope. Compare the new VTC to previous case. Explain the shift in VTC curve.

Decrease the threshold voltage of NMOS transistor by 0.15V and increase the (absolute value) threshold voltage of PMOS by 0.2V.

Plot the VTC using CosmoScope. Compare the new VTC to previous cases. Explain the shift in VTC curve.

Note:

Refer to HSpice Manual Page 690/1714 (Session 15-12) where you can find out how to adjust V_T

TASK II – SIZING OF INVERTER CHAIN

STEP 1 MEASUREMENT OF THE PARASITICS OF INVERTER

Build an unit size inverter with 65nm model. Simulate it with HSPICE. Add this statement to your netlist:

```
.OP
```

In the lis file, you will find ‘cdtot’ and ‘cgtot’ for each transistor.

Note: values are different for cutoff, linear and saturation. Think about how to calculate the average.

Based on the values you find, calculate the input capacitance and self-load coefficient of the unit size inverter

STEP 2 INVERTER CHAIN SIZING, FOR GIVEN N

Use **THREE** inverters in series to drive a **5pF** capacitor,

Based on Lecture 11, calculate the optimal sizing for each stage

Write (in text editors) or Generate (by SUE) a netlist for the inverter chain you optimized; simulate for the delay.

Note: Refer to HSpice Manual Page 141/1714 (Session 4-19) where you can find out how to use .measure statement

Note: you might find these statements useful:

```
.subckt  INV  X  Y  Size=1   * Defining subcircuit with parameters
 M1  Y  X 0   0    NMOS L=65n W='Size*65n'
 M2  Y  X VDD VDD  PMOS L=65n W='Size*130n'
.ends
```

```
X2  2  3  INV   Size=4       * Using subcircuit with parameters
```

```
Cout out 0 5p                * Defining load capacitance
```

STEP 3 INVERTER CHAIN SIZING

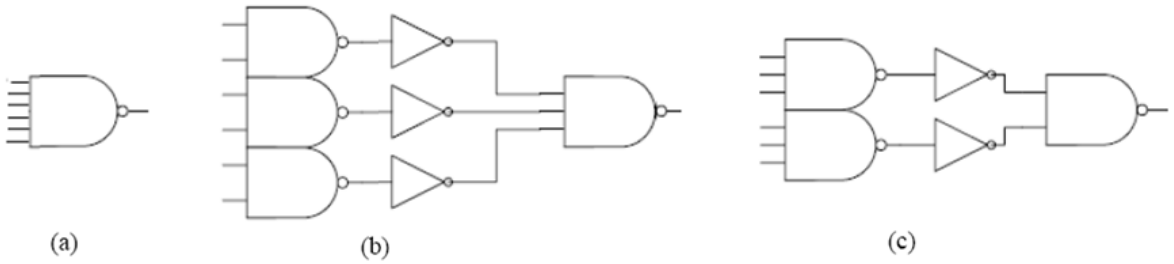
Now design another inverter chain to drive a **5pF** capacitor, with **OPITIMAL** number of stages.

Based on Lecture 11, calculate the optimal inverter number and the optimal sizing for each stage.

Write (in text editors) or Generate (by SUE) a netlist for the inverter chain you optimized; simulate for the delay.

TASK III – SIZING OF CMOS GATE

Consider the design of a six input NAND gate. In the figure below, three different approaches for implementation of such a gate are given. Use 65nm technology with V_{DD} =1.5V.



STEP 1 OPTIMIZATION OF GATES

Let the output node drive a **5pF** capacitor,

Based on Lecture 11, show how you will calculate the optimal sizing for each stage in (a) (b) and (c).

STEP 2 DELAY MEASUREMENT

Build netlists for the three circuits.

Attach your netlists.

Compare the delay *tp=(tplh+tphl)/2* of these three implementations. For low-to-high transition, assume that all but one of the inputs is high and transition begins when the last input goes high. For low-to-high transition, assume that just one of the inputs goes low and the other inputs remain high.

Measure the average power consumption *Pavg* of these circuits, when there is one low-to-high and one high-to-low at the output in a specified time period (use same input transitions as in part (a)).

Note: Refer to HSpice Manual Page 141/1714 (Session 4-19) where you can find out how to use .measure statement

Compare the three designs using energy-delay product (EDP) metric, which is defined as: $EDP = Pavg \cdot tp^2$

Fill the table below with simulation results and explain which circuit would be your choice if you want to optimize power, delay, or the EDP.

	Delay (tp)	Power	EDP
Circuit (a)			
Circuit (b)			
Circuit (c)			