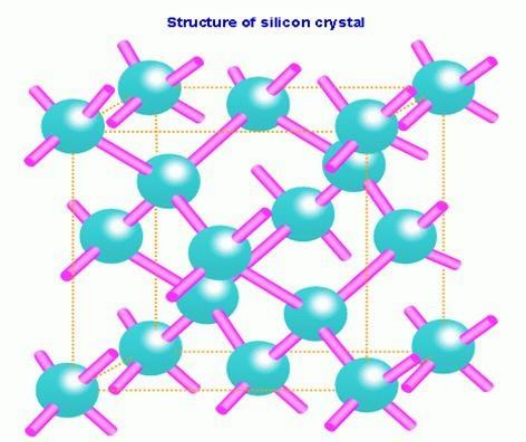
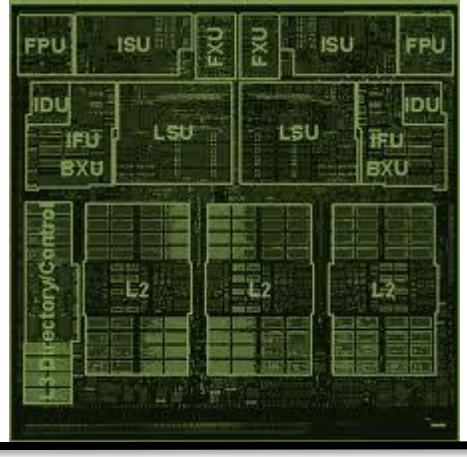
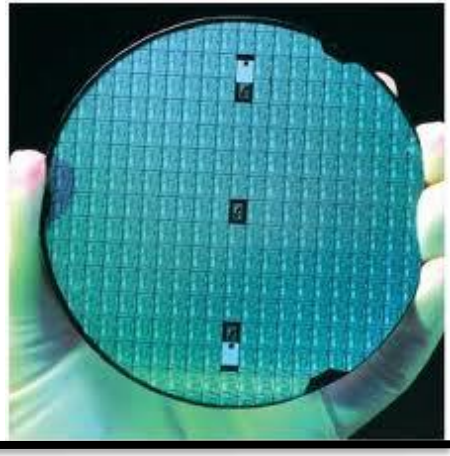






ECE 124A

VLSI Principles

Lecture 8

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

MOS Capacitor (Review)

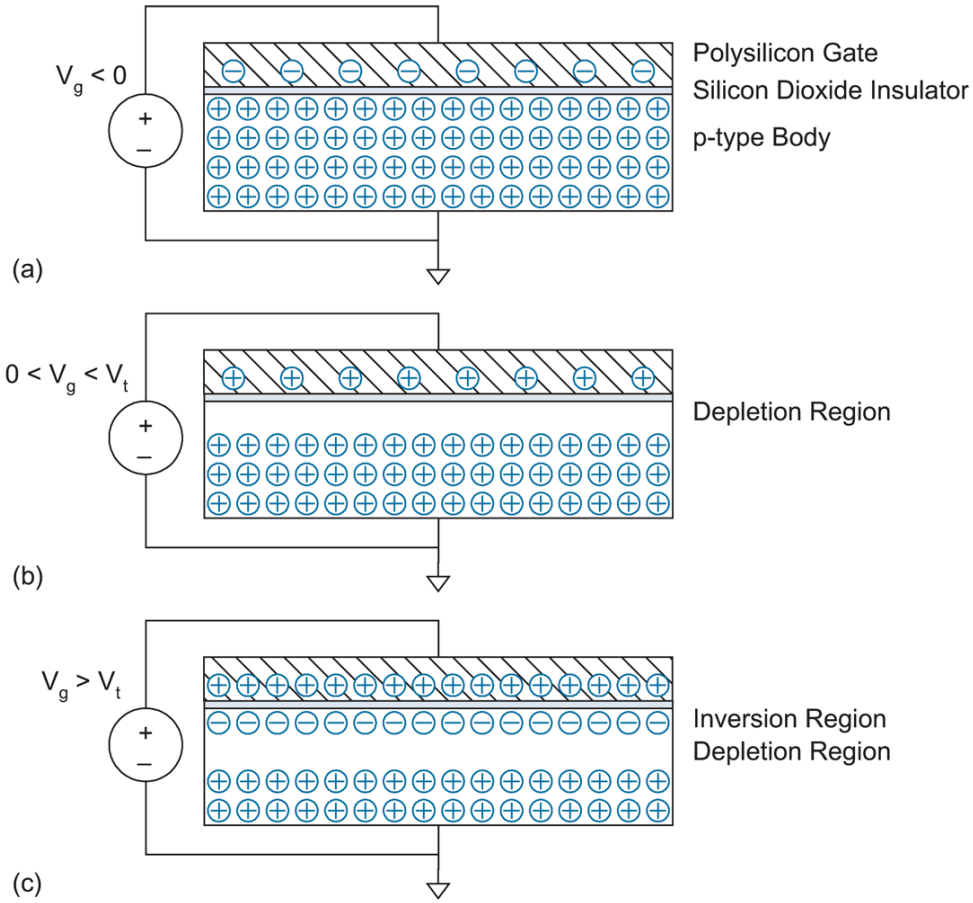
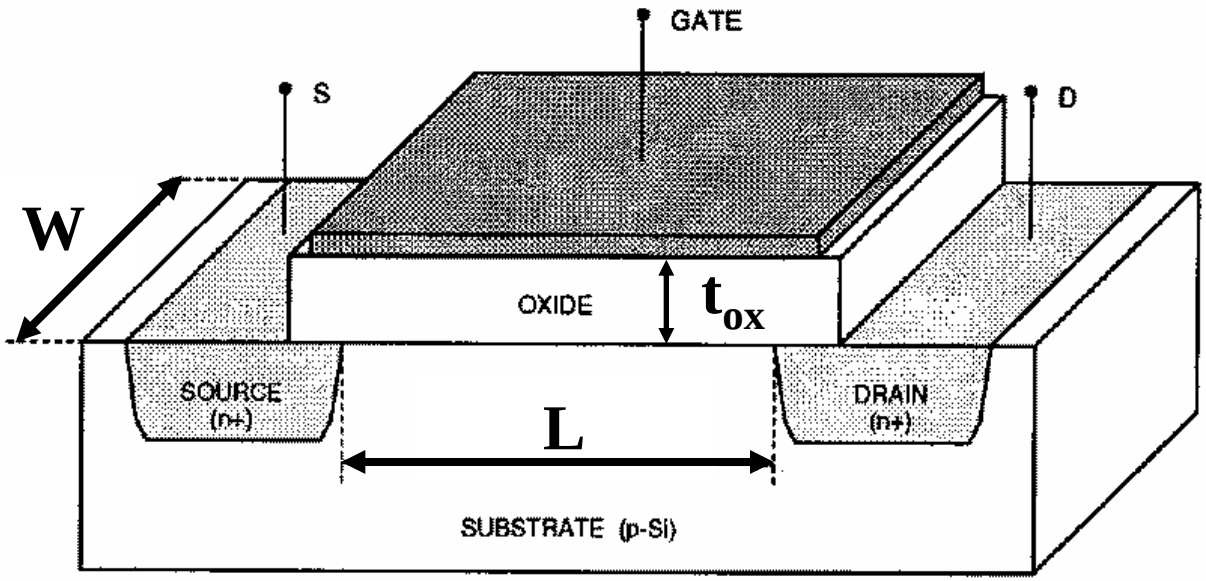


FIG 2.2 MOS structure demonstrating (a) accumulation, (b) depletion, and (c) inversion

MOS Transistor

- Important transistor physical characteristics
  - Channel length L
  - Channel width W



Threshold voltage, summary

- If $V_{SB} = 0$ (no substrate bias):

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

- If $V_{SB} \neq 0$ (non-zero substrate bias)

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

- Body effect (substrate-bias) coefficient:

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}}$$

+ for NMOS
- for PMOS

- Threshold voltage increases as V_{SB} increases!

(easy to explain with a band diagram….)

Threshold Voltage (NMOS vs. PMOS)

	NMOS	PMOS
Substrate Fermi potential	$\phi_F < 0$	$\phi_F > 0$
Depletion charge density	$Q_B < 0$	$Q_B > 0$
Substrate bias coefficient	$\gamma > 0$	$\gamma < 0$
Substrate bias voltage	$V_{SB} > 0$	$V_{SB} < 0$
Threshold voltage (enhancement devices)	$V_{T0} > 0$	$V_{T0} < 0$

Threshold voltage adjustment

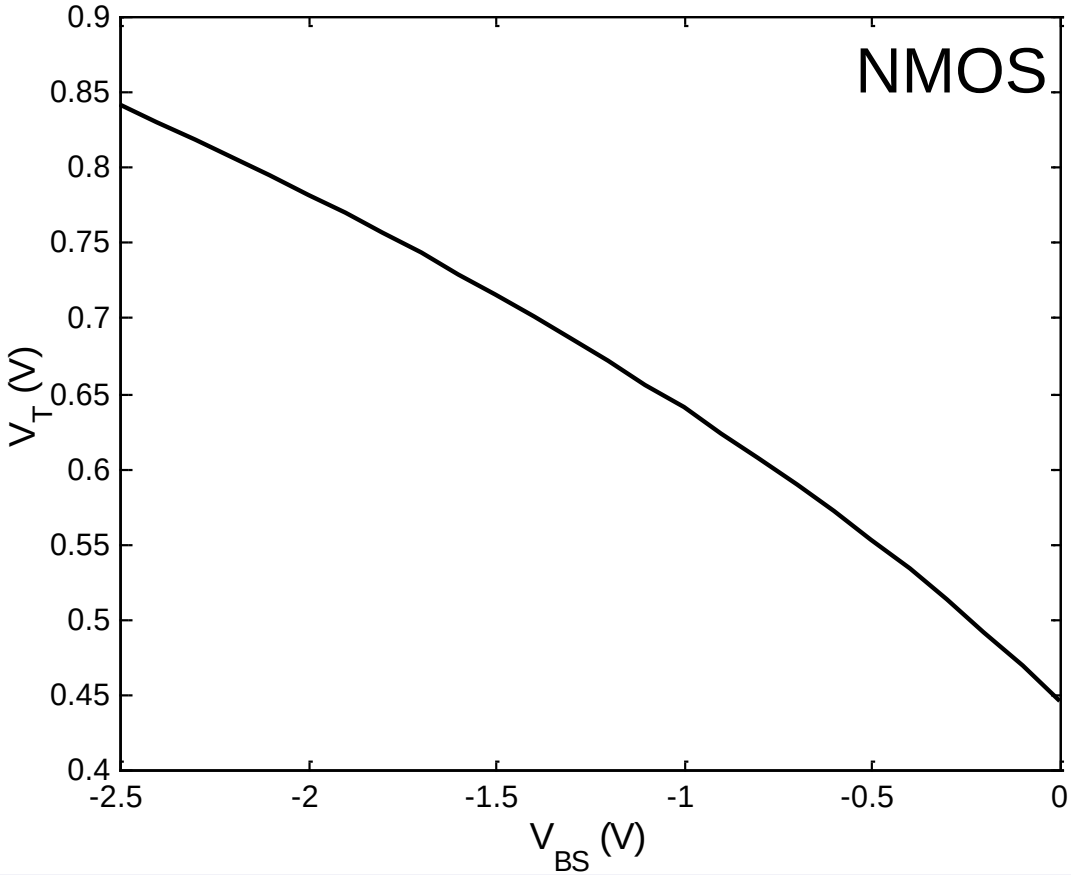
- Threshold voltage can be changed by doping the channel region with donor or acceptor ions
- For NMOS:
  - V_T increased by adding acceptor ions (p-type)
  - V_T decreased by adding donor ions (n-type)
  - Opposite for PMOS
- Approximate change in V_{T0}:
  - Density of implanted ions = N_I [cm^{-2}]
  - Assume all implanted impurities are ionized

$$\Delta V_{T0} = \frac{qN_I}{C_{ox}}$$

Example: V_{T0} Adjustment

- Consider an NMOS device:
  - P-type substrate: $N_A = 2 \times 10^{16}$ cm^{-3}
  - Polysilicon gate: $\Phi_{GC} = -0.92$V
  - $t_{ox} = 600$ Å (1Å = 1×10^{-8} cm)
  - $N_{ox} = 2 \times 10^{10}$ cm-2
  - $\varepsilon_{Si} = 11.7\ \varepsilon_0$, $\varepsilon_{ox} = 3.97\ \varepsilon_0$
- (a) Find V_{T0}
- (b) Find amount and type of channel implant to get $V_{T0} = 0.4$ V

The Body Effect



Draw a band diagram to convince yourself…

MOSFET Operation (NMOS)

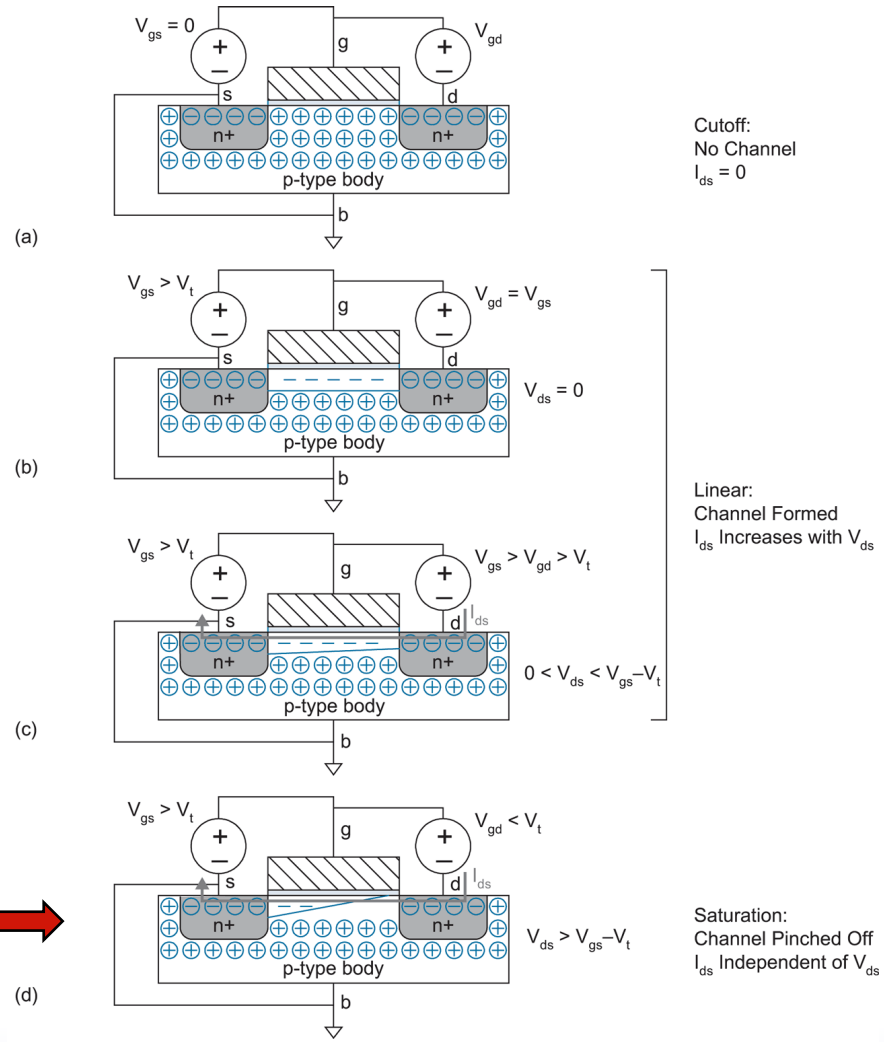


FIG 2.3 nMOS transistor demonstrating cutoff, linear, and saturation regions of operation

Remember, both drift and diffusion currents play a role…

***Pinch-off:* conduction still takes place from Source to Drain due to drift of electrons under the influence of the +ve drain voltage**

Channel voltage no longer > V_t all along the channel….

$V_{GS} - V(x) < V_t$

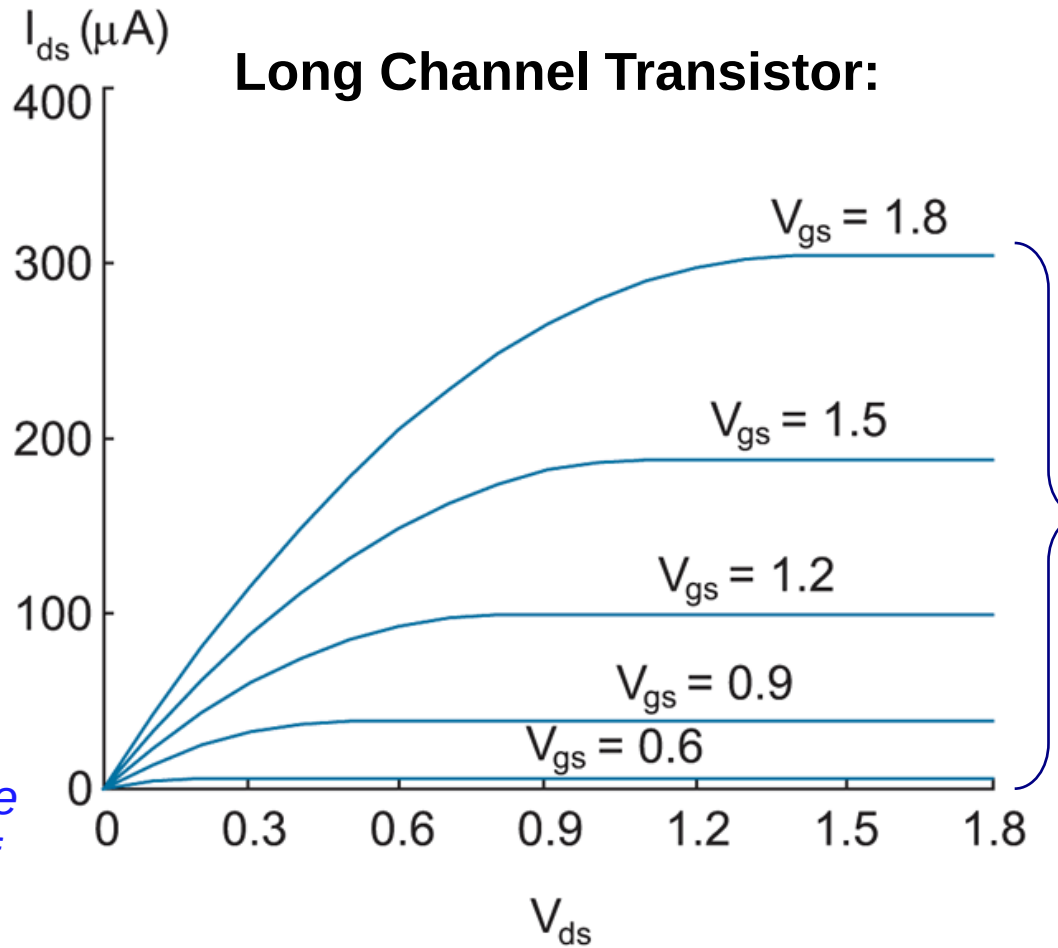
Conduction dominated by DRIFT

NMOS Characteristics

Recall that the surface channel vanishes at the drain end of the channel….when current saturates…known as "pinch-off"

Any voltage $V_{DS} > V_{DSAT}$ is dropped across the high-field pinch-off region…where inversion charge =0

Long Channel Transistor:



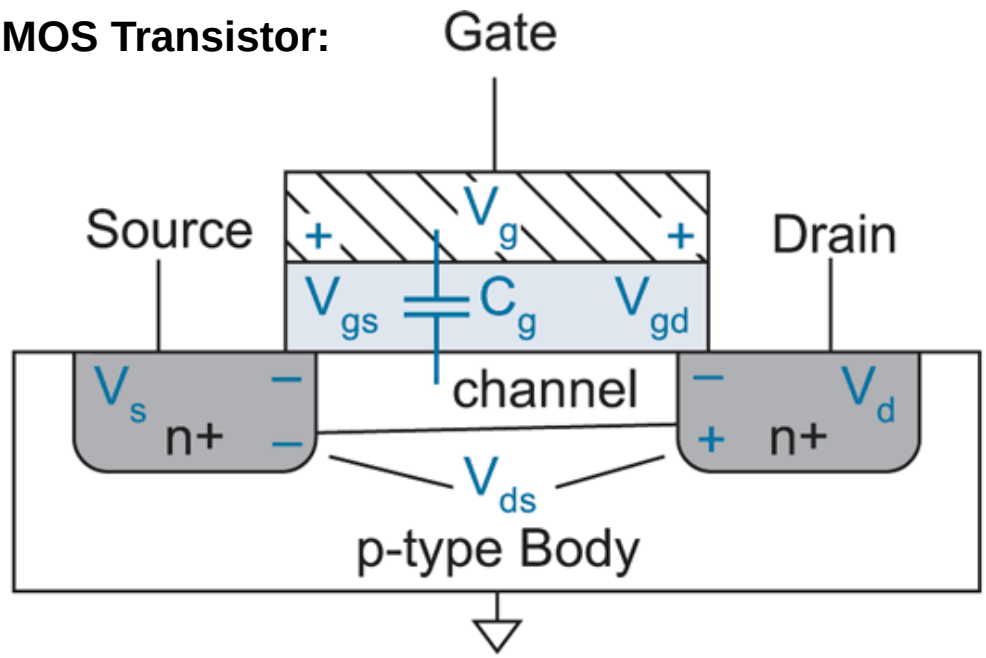
Quadratic Relationship

The saturation voltage V_{DSAT} can be estimated by equating dI_{ds}/dV_{ds} to zero

FIG 2.7 I-V characteristics of ideal nMOS transistor

Channel Charge

NMOS Transistor:



$V_{ds} = V_{gs} - V_{gd}$

Average gate to channel potential:

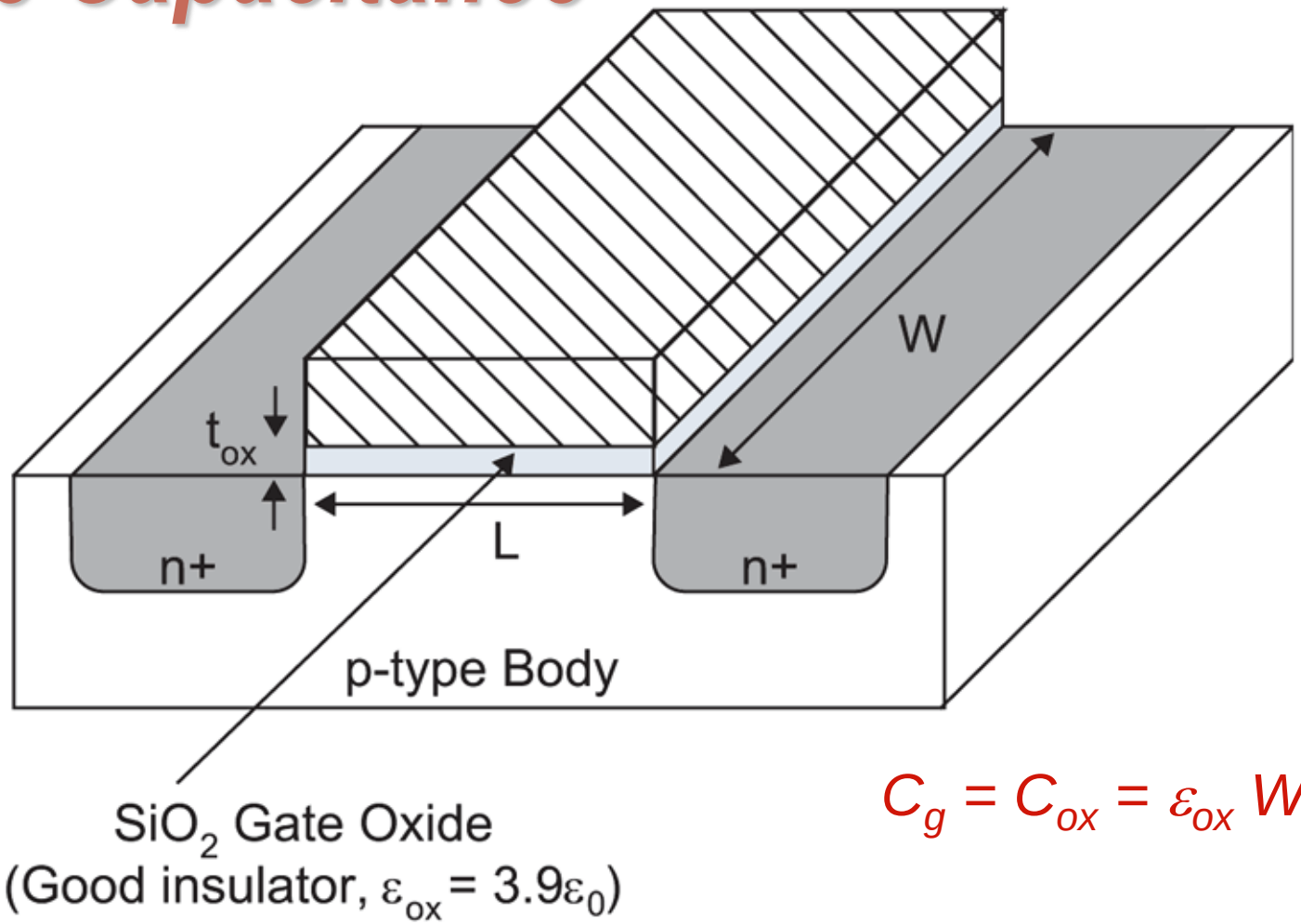
$$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$$

FIG 2.5 Average gate to channel voltage

Note: i) The inversion layer thickness is assumed to be zero: all charges are assumed to be located at the Si surface….like a sheet of charge….
ii) Hence, there is no potential drop or band bending across the inversion layer….

$$Q_{channel} = C_g (V_{gc} - V_t)$$

Gate Capacitance



$$C_g = C_{ox} = \varepsilon_{ox} WL/t_{ox}$$

FIG 2.6 Transistor dimensions

Transistor Currents (NMOS)

Cutoff Region: $I_{ds} = 0,\ V_{gs}<V_t$

Linear Region: $V_{gs}> V_t,\ V_{ds}< V_{gs}-V_t$

$I_{ds}= W\, Q_{channel}$ .carrier velocity(v)

$I_{ds} = \mu\, C_{ox}\, W/L\, (V_{gs}-V_t-V_{ds}/2)V_{ds}$

Since Vds is small, Vds/2 can be neglected…and Ids is linearly proportional to Vds….like a resistor

$$Q_{channel} = C_g\,(V_{gc} - V_t)$$
$$V_{gc} = V_{gs} - V_{ds}/2)$$

$$v = \mu E$$
$$E_{lateral} = V_{ds}/L$$
$$\beta = \mu\, C_{ox}\, W/L$$

Saturation Region: $V_{gs}>V_t,\ V_{ds} > V_{gs} - V_t$

Note: as Vds increases, average $Q_{channel}$ decreases…

$dI_{ds}/dV_{ds} = 0$ at $V_{ds}=V_{dsat}=V_{gs}-V_t$

Substituting V_{ds} with V_{dsat} above: $I_{ds} = \beta/2\,(V_{gs}-V_t)^2$

Note: for PMOS $V_{tp} = V_{tn}$ $\mu_p < \mu_n$, hence $(W/L)_{PMOS} \sim 2\,(W/L)_{NMOS}$

PMOS Transistor

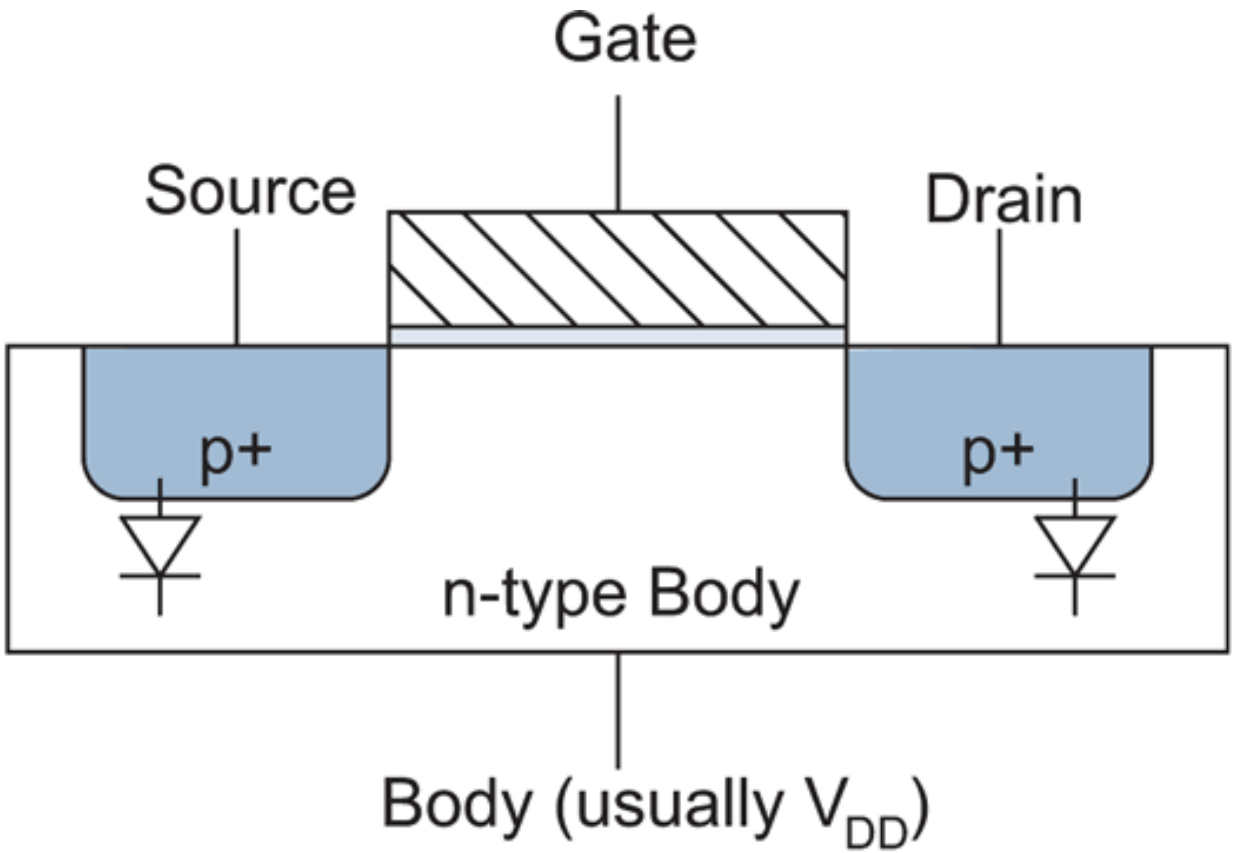


FIG 2.4 pMOS transistor

PMOS Characteristics

Long Channel Transistor:

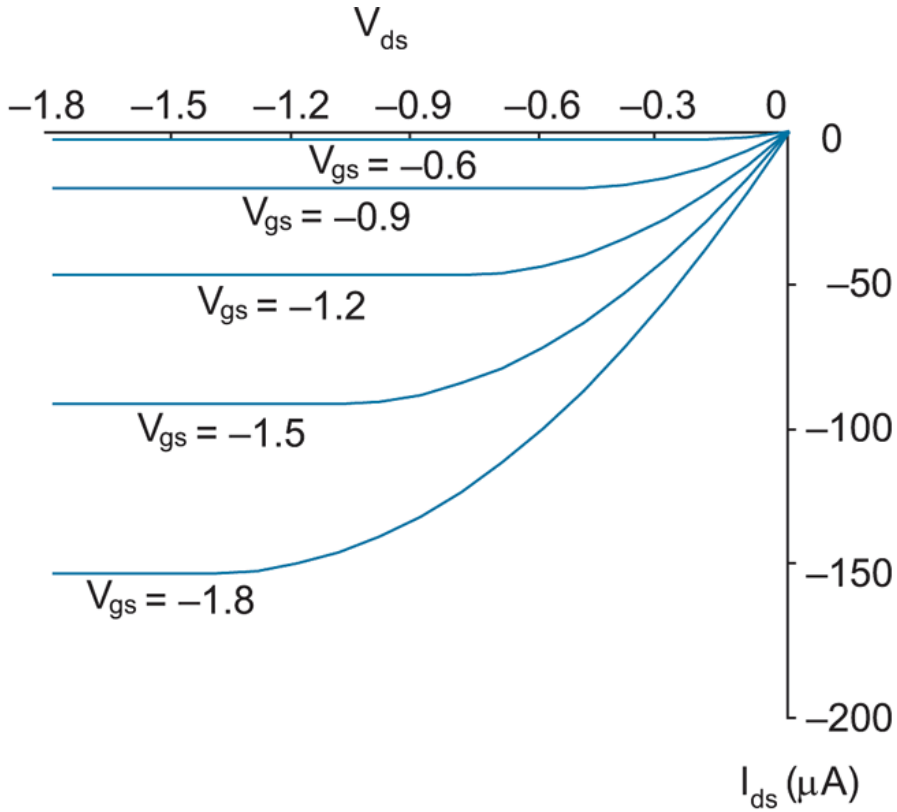


FIG 2.8 I-V characteristics of ideal pMOS transistor

Channel Length Modulation

- In saturation, pinch-off point moves
  - As V_{DS} is increased, pinch-off point moves closer to source
  - Effective channel length becomes shorter
  - Current increases due to shorter channel

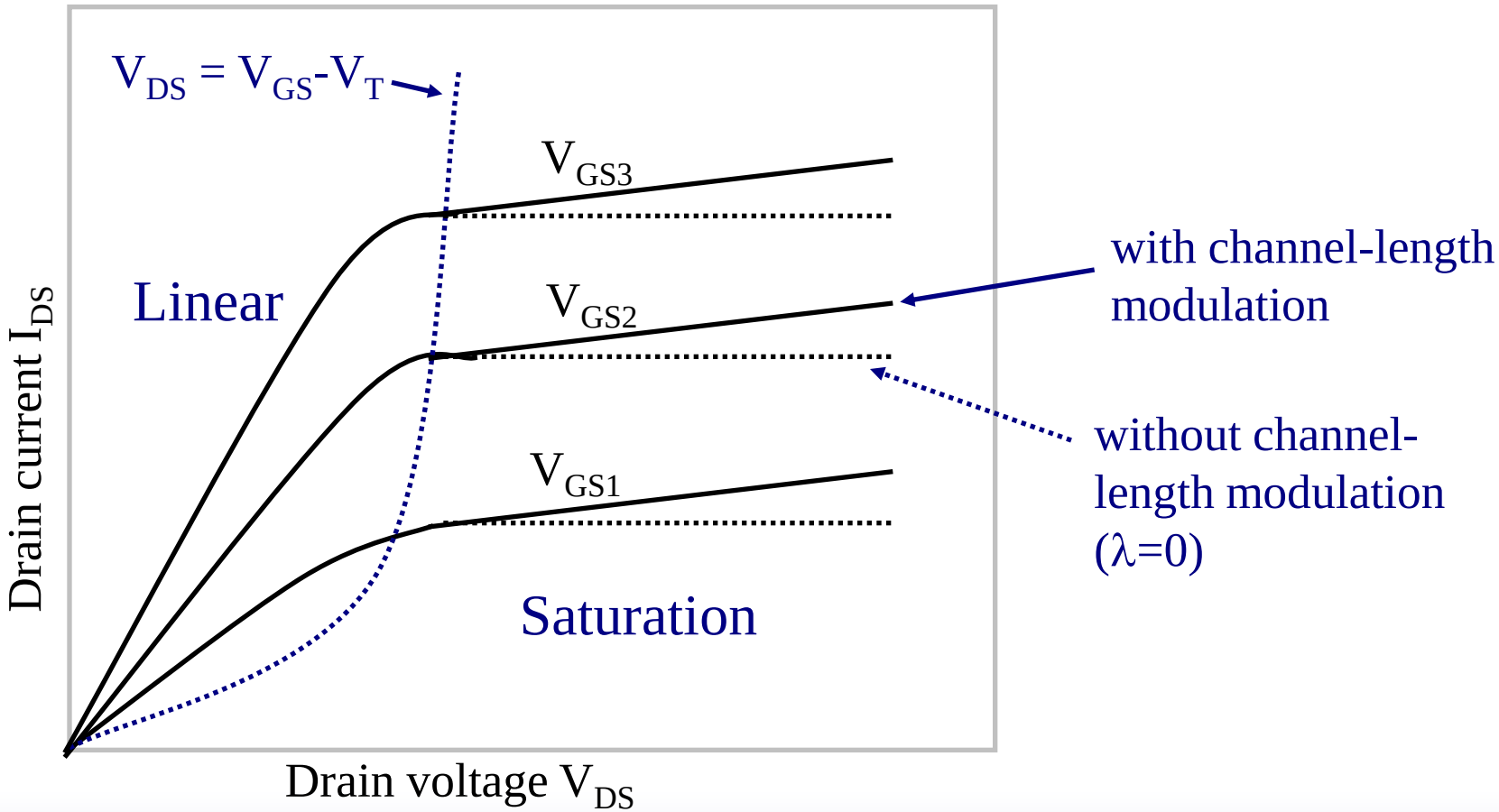
$$L' = L - \Delta L$$

$$\boxed{I_D = \tfrac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TN}\right)^2\left(1 + \lambda V_{DS}\right)}$$

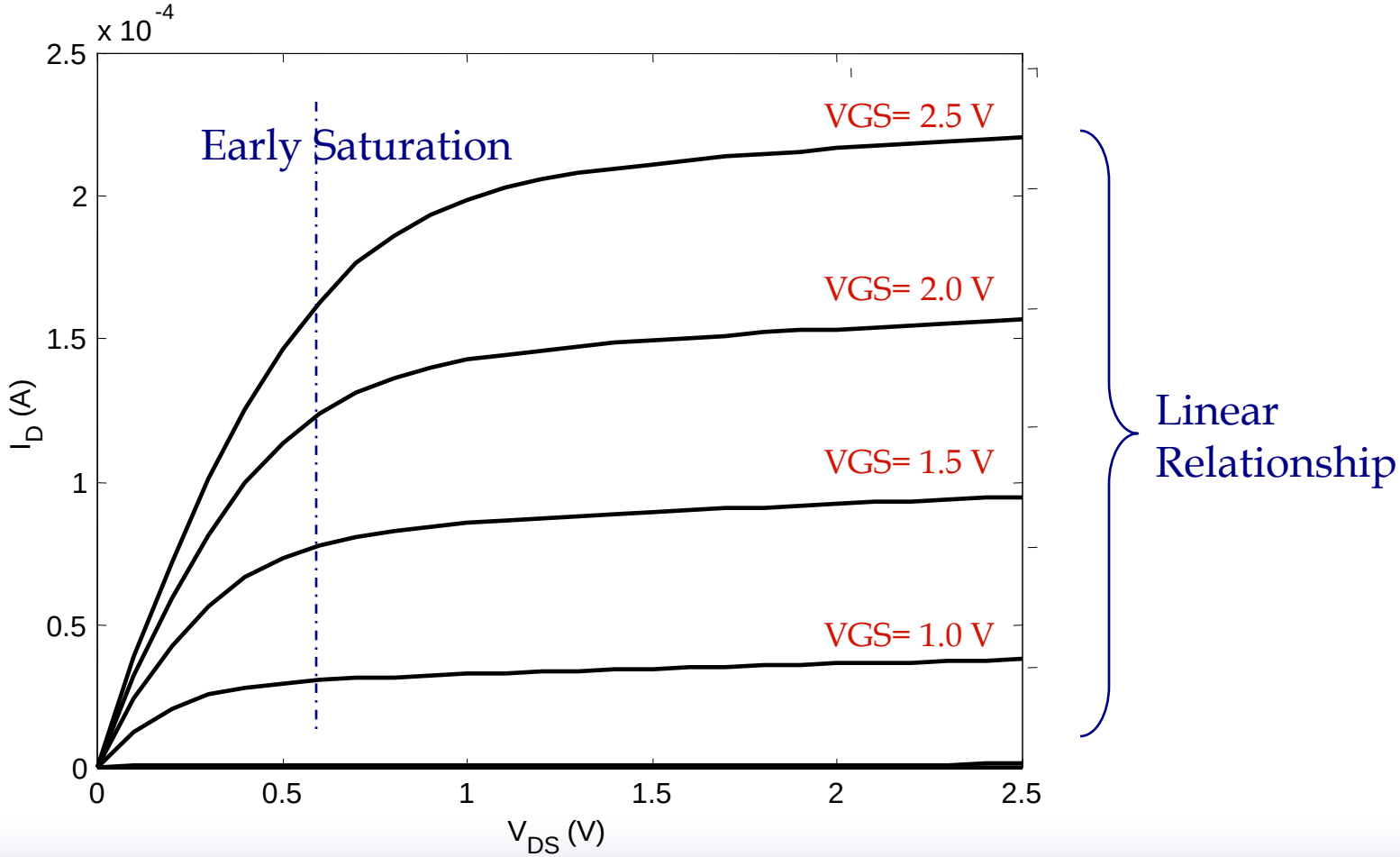
λ = channel length modulation coefficient

Summary: MOS I/V

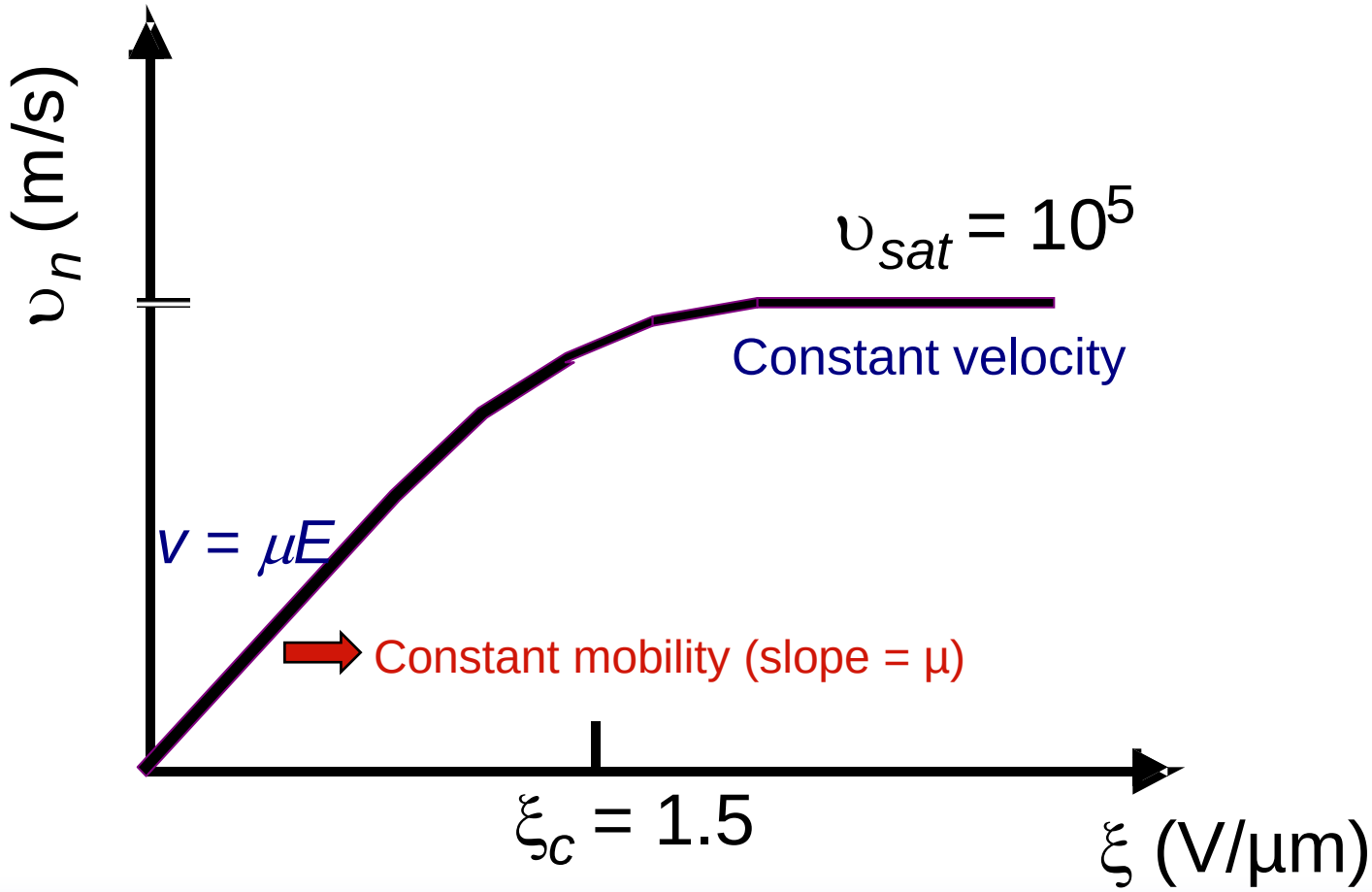
I/V curve for NMOS device:



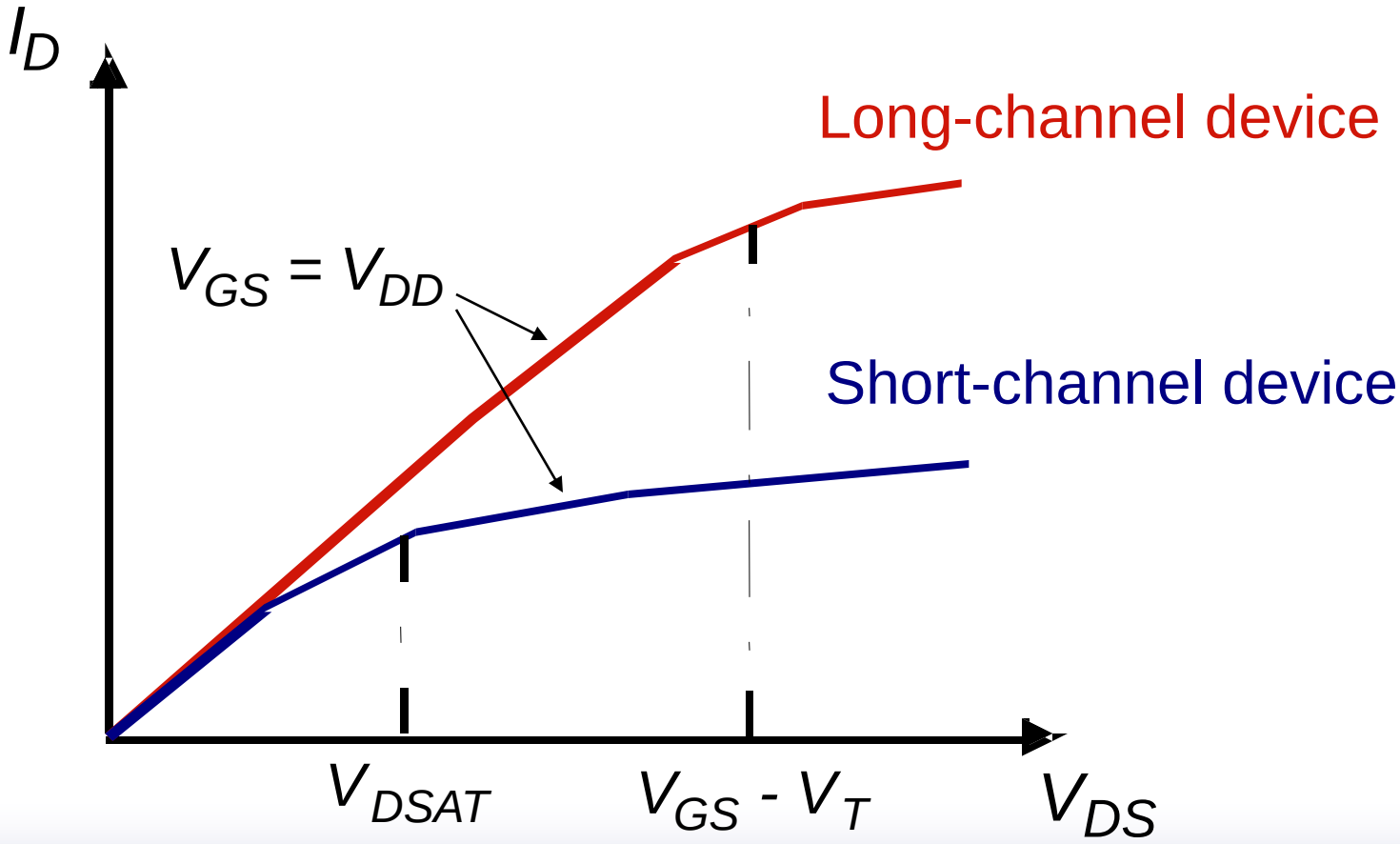
Current-Voltage Relations Short-Channel Transistors



Velocity Saturation



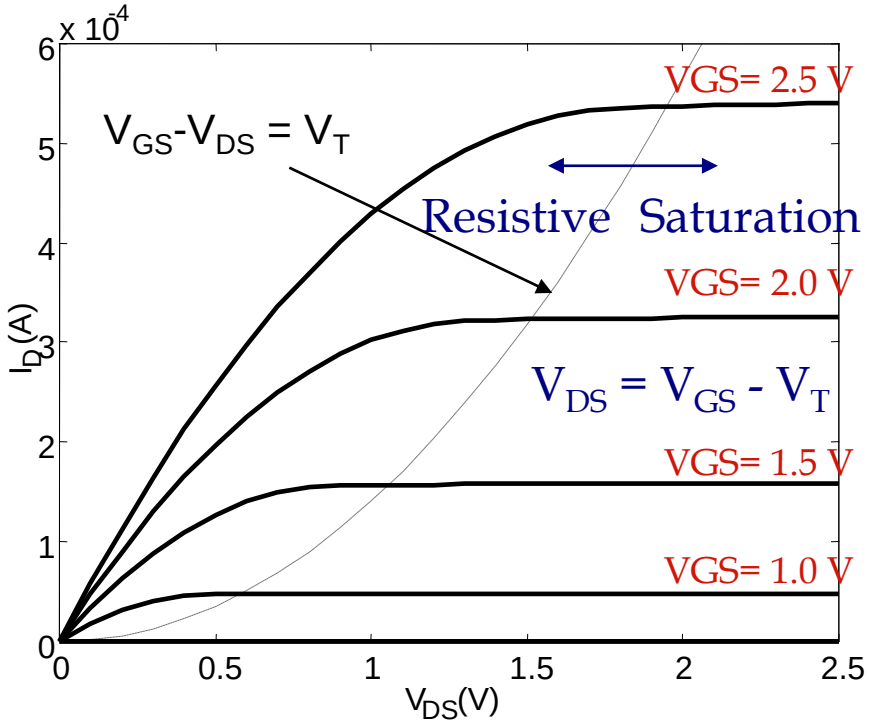
Perspective



I_D versus V_{DS}

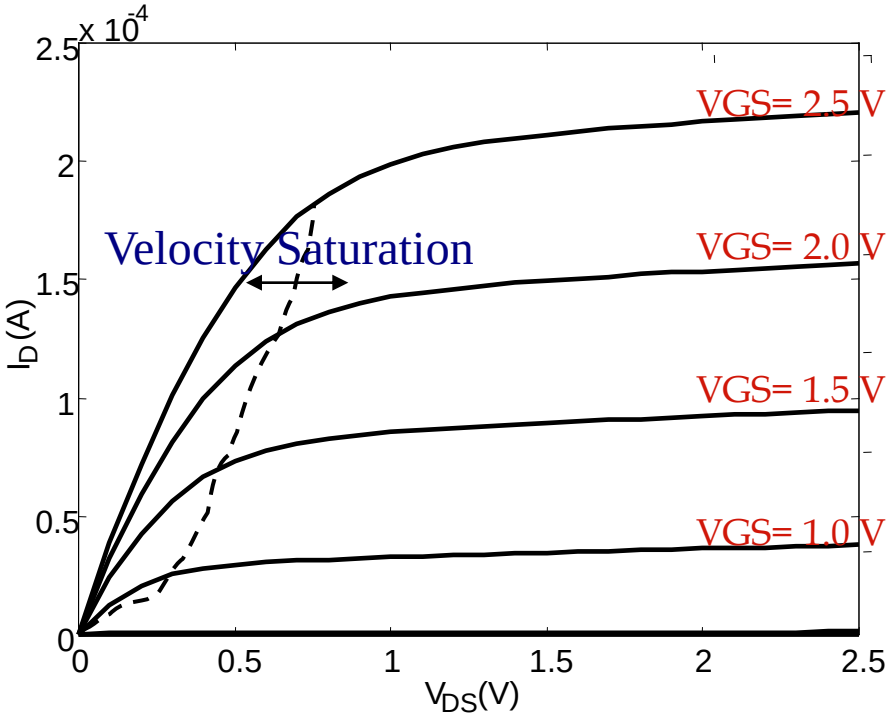
W/L = 1.5 for both cases….

L = 10 um



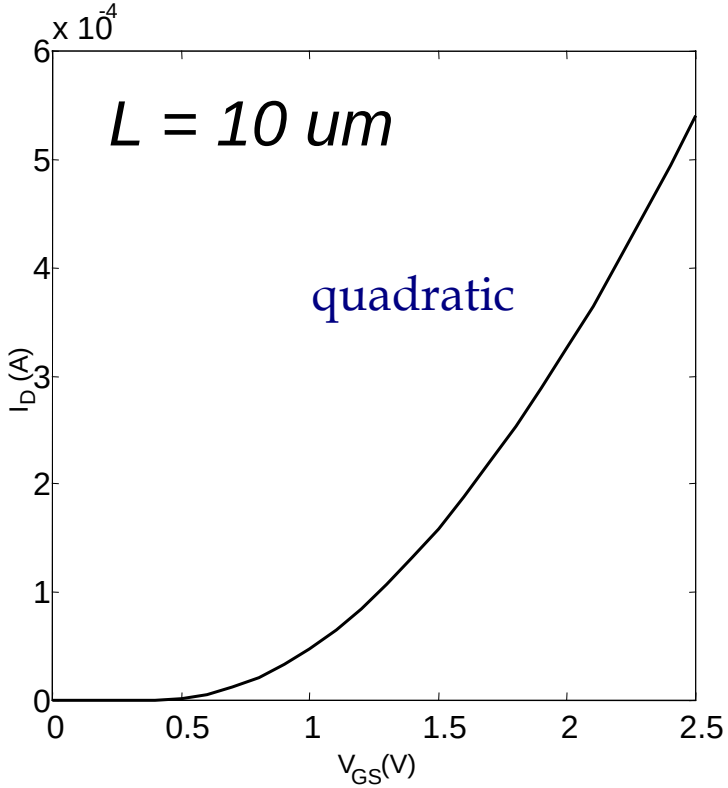
Long Channel

L = 0.25 um

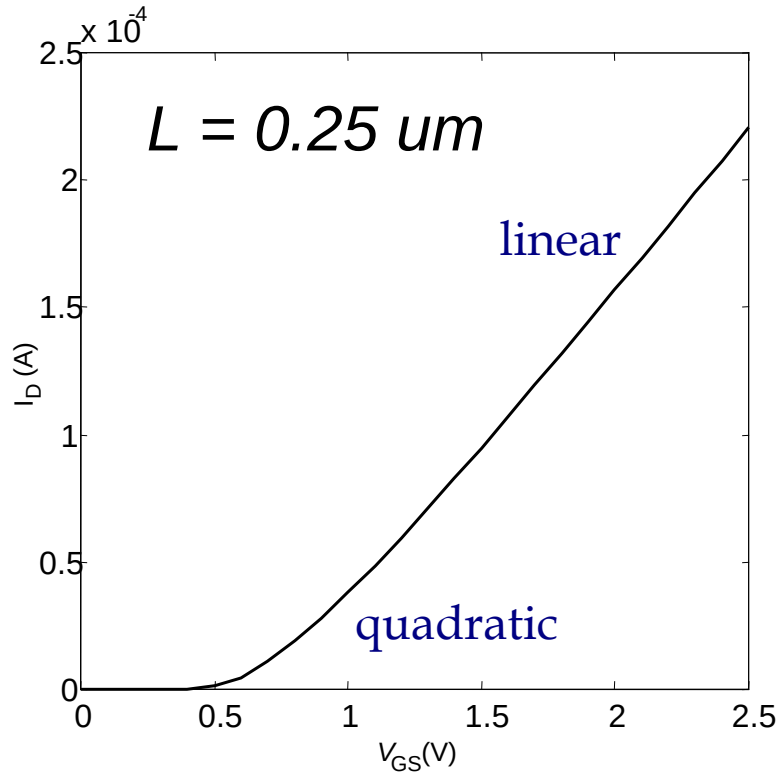


Short Channel

I_D versus V_{GS}

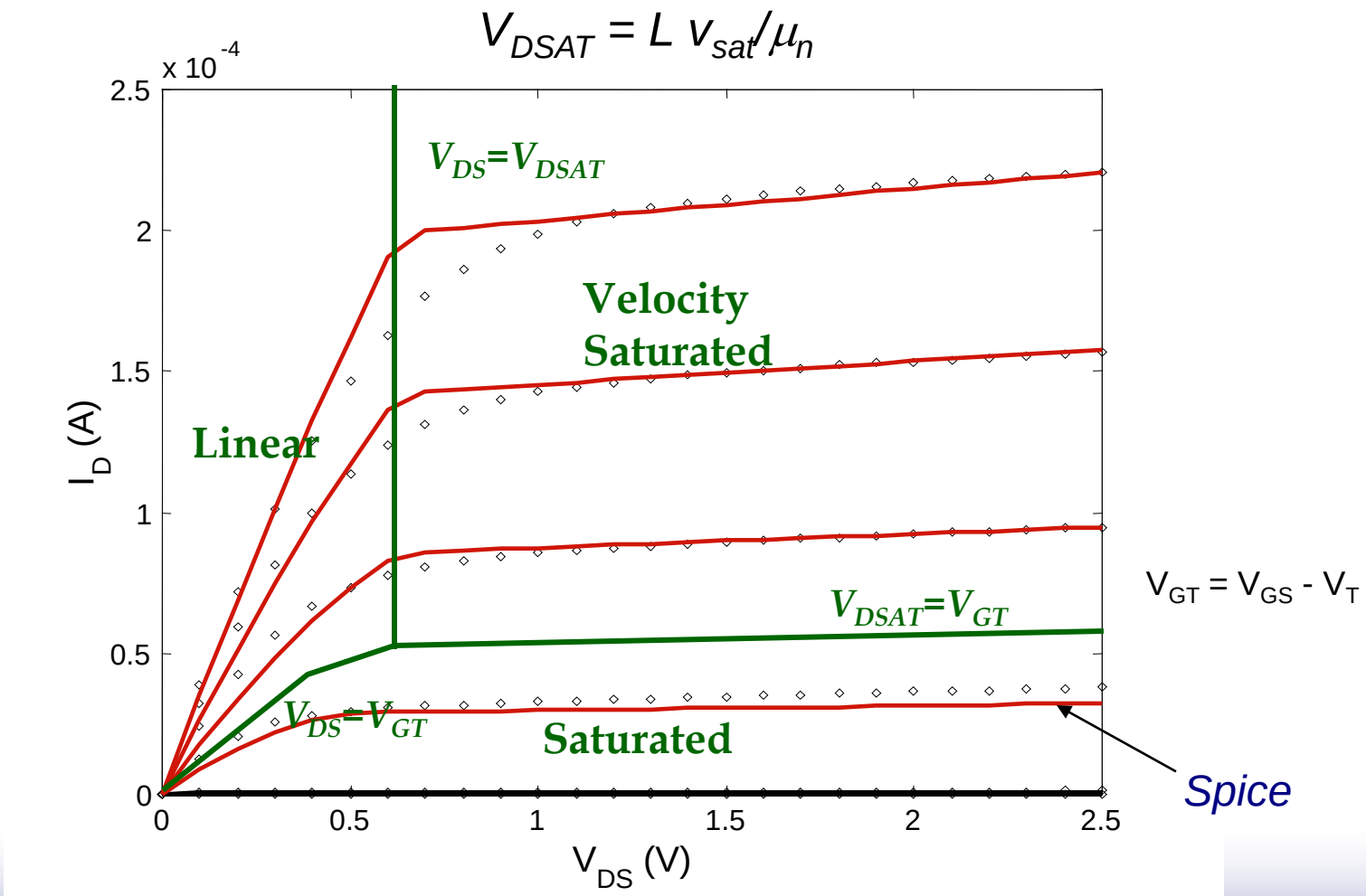


Long Channel

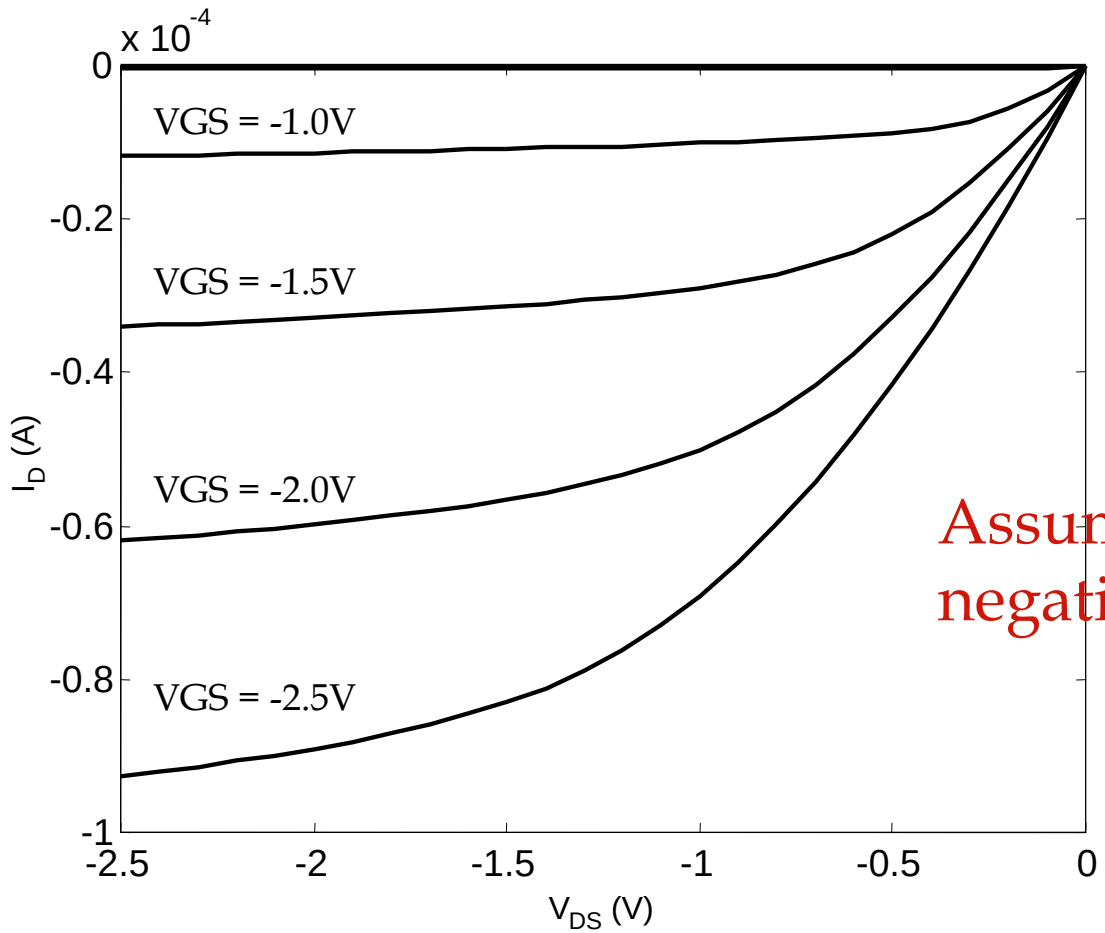


Short Channel

Simple Model versus SPICE



A PMOS Transistor (short-channel)



Assume all variables negative!

Alpha-Power MOSFET Model

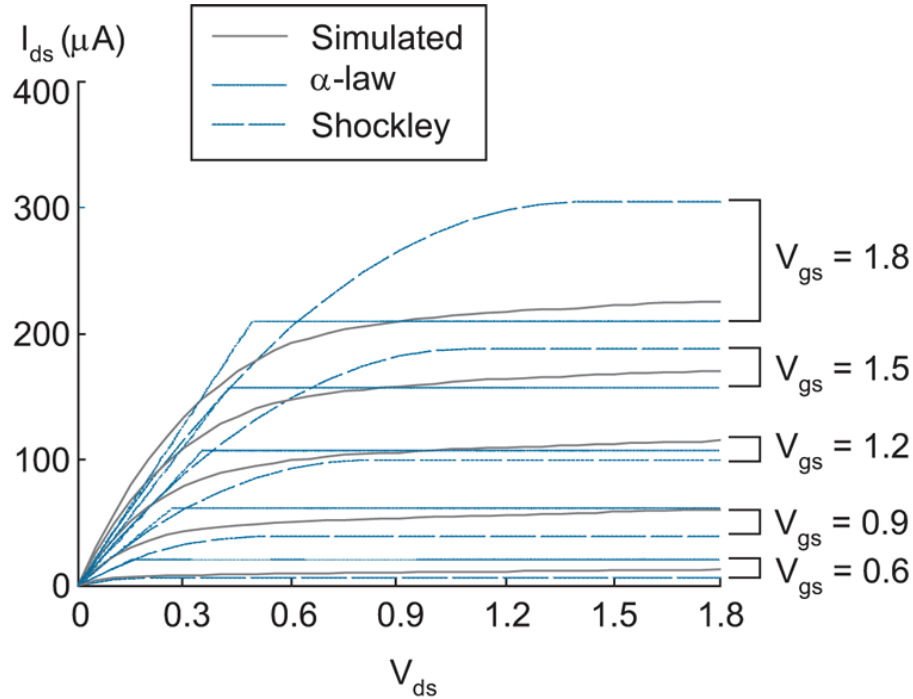


FIG 2.17 I-V characteristics for nMOS transistor with velocity saturation

At low lateral E-fields, V_{ds}/L, current increases linearly with E-field

At high fields, $E = E_{sat}$

Carrier velocity saturates due to carrier scattering = v_{sat} (= μE_{sat})

$I_{ds} = \mu C_{ox} W/L (V_{gs} - V_t)^2$

---no velocity saturation

$I_{ds} = C_{ox} W (V_{gs} - V_t) v_{sat}$

---complete velocity saturation

Practical situation: carrier velocity doesn't increase linearly with field but is not completely velocity saturated….

Sakurai Model: $I_{ds} \propto (V_{gs} - V_t)^{\alpha}$

$1<\alpha<2$, is the velocity saturation index, determined by curve fitting…..also accounts for mobility degradation due to high vertical field (V_{gs}/t_{ox})