

UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering

MIDTERM EXAMINATION-ECE124A

Room: ESB-Cooper Lab, November 7, 3:30-4:45 PM

READ CAREFULLY:

- **This is a CLOSED BOOK Exam. Any form of notes is not allowed. Calculators OK.**
- **READ the questions carefully before answering. Include all your answers in locations specified on these pages. Show ALL WORKING used to arrive at answers. Use space provided for all working. Use the back sides if necessary.**

Question	Scores
#1	/ 50
#2	/ 20
#3	/ 15
#4	/ 15
TOTAL	/ 100

Good Luck!

Perm No. _____

1. (50 pts) Short-Answer Questions: (suggested time: 35 minutes)

- a) CMOS processes often result in NMOS devices with negative threshold voltages. In order to get a positive V_T , additional channel doping is performed. Should the implanted ions be Boron or Phosphorus? Explain your answer. (6 pts)

Sol: The implanted ions should be P-type (Boron). This increases the amount of negative charge Q_{BO} , increasing the threshold voltage.

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (\text{The third term is affected by the channel doping})$$

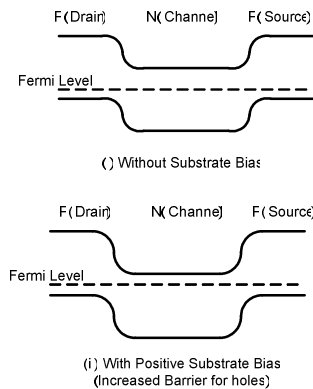
- b) What kind of substrate bias can be applied to a PMOS transistor to lower its leakage? Draw the band diagram of the transistor across source-channel-drain under such biasing condition. (7 pts)

Sol: Positive substrate bias (usually, $\geq V_{DD}$) can be applied to a PMOS in order to lower its leakage. That would increase the barrier for the holes and prevents sub-threshold leakage.

[3 pts]

Part (i) in the following figure shows PMOS channel band diagram from drain to source without any substrate bias. When we apply the bias, the bands near the channel move down by the amount of reverse bias applied, with reference to the position of source and drain, as shown in part (ii)

[4 pts]



- c) Explain why the C_{GD} capacitances at the output of a switching inverter are doubled in the calculation of load capacitance. (5 pts)

Solution: Due to Miller effect.

[2.5 pts]

When in transition, voltage changes on both side of C_{GD} capacitor and therefore the effective capacitance gets multiplied by 2.

[2.5 pts]

- d) A ring oscillator using 7 static CMOS inverters has been designed for a frequency of 2GHz. Neglecting interconnect and junction capacitance, what is the new frequency if all transistor widths are doubled? If all the transistor lengths are doubled? How is the operation of the ring oscillator changed if one extra static CMOS inverter is added? (10 pts)

Solution:

$$f = \frac{1}{2Nt_p} \text{ where } N=7, t_p = \frac{C\Delta V}{I_{avg}} \text{ where } I_{avg} \propto \frac{W}{L} \text{ and } C \propto WL \text{ Therefore, } t_p \propto L^2$$

(1) If all transistor widths are doubled, then t_p remains unchanged i.e. frequency=2GHz

[4.0 pts]

(2) If all transistor lengths are doubled, then new $t_p = 4X t_p$ i.e., frequency = 0.5 GHz

Perm No. _____

[4.0 pts]**(3) If one extra static CMOS inverter is added, it is no longer a ring oscillator.****[2.0 pts]**

- e) Show that the capacitive power consumption (P_{cap}) of a CMOS inverter is independent of the load capacitance (C_L) when operating at its maximum speed.

(6 pts)**Solution:**

$$P_{cap} = C_L (V_{dd})^2 f_{max} = C_L (V_{dd})^2 (1/\tau_{inv})$$

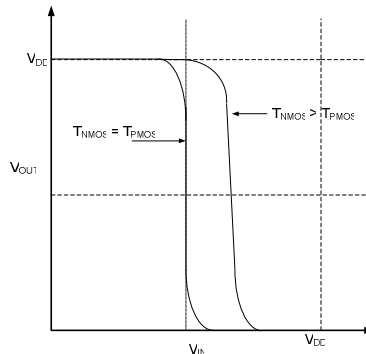
$$\tau_{inv} = C_L V_{dd} / I_{dsat}$$

$$\text{Hence, } P_{cap} = I_{dsat} V_{dd}$$

Clearly the capacitive power consumption is independent of the load capacitance.

- f) In a typical 2:1 CMOS inverter, if the PMOS can be made to operate at a lower temperature (say 20 degree C) than the NMOS (say 120 degree C), what will be the impact on: i) the voltage transfer curve (indicate with a sketch of the VTC), ii) inverter switching threshold, iii) gain, iv) noise margin (low and high), v) delay and vi) power (both switching and leakage)?

What can be done to the NMOS to make the inverter symmetric (without changing the temperature)?
(16 pts)

**Sol:**

1. Voltage Transfer Curve will move to the right (as shown in the above figure.) and it spreads slightly (transition is less abrupt). **[5.0 pts]**
2. Inverter switching threshold will increase since VTC has moved to the right. **[1.0 pts]**
3. Gain is given by the slope of the VTC. Since the VTC spreads slightly, the gain will decrease. **[2.0 pts]**
4. Noise Margin:
 - a. NM_L Increases because VTC has shifted to the right.
 - b. NM_H Decreases because VTC has shifted to the right. **[2.0 pts]**
5. Since we are only decreasing the resistance of the PMOS without affecting its capacitance, low-to-high out-put delay (T_{PLH}) will decrease. There would not be any change in the high-to-low output delay. **[2.0 pts]**
6. Power:
 - a. Switching power = $C_L(V_{DD})^2 f$.
 $f = 1/\tau$, $\tau = (\tau_{phl} + \tau_{plh})/2$

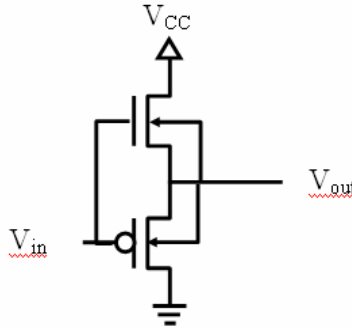
When PMOS operates at a lower temperature, τ_{plh} decreases. Hence, τ decreases and f increases. Hence, the switching power increases

- b. Leakage Power (Off-state): Here, we consider only off-state leakage. For the off-state leakage, same current has to flow through the NMOS and the PMOS and

Perm No. _____

because reduction in temperature will reduce the leakage in PMOS, leakage power of this inverter will decrease. [2.0 pts]
 We can increase the (W/L) ratio of the NMOS to make the inverter symmetric. [2.0 pts]

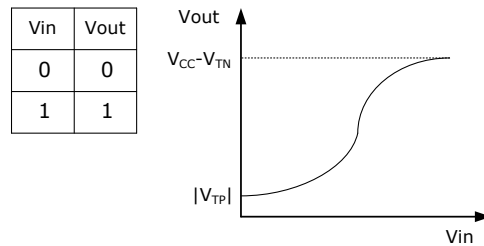
2. (20 pts) (suggested time: 15 minutes) Analyze the following two-transistor logic gate:



- a) Describe the operation of this gate (include a truth table and a VTC sketch). Is this gate ratioed or ratioless logic? (6 pts)
- b) Find the minimum and maximum output voltages, assuming the input is driven by a static CMOS inverter. Would these voltages change if the NMOS body terminal were connected to ground and the PMOS body terminal were connected to Vcc? If so, how? (6 pts)
- c) If this gate has a fanout of 4, what will be the switching power dissipation for 0 to 1 and 1 to 0 transitions at the output? (8 pts)

Solution:

(i) The gate is a buffer or delay. The logic level of output is identical to the input like a voltage follower. It is ratioless, since the output voltage levels do not depend on sizing. [6.0 pts]



(ii) When the input is low, the output is $-V_{tp}$. Hence the V_{SB} , which decides the ΔV_{th} due to body-effect, is V_{tp} . But when the PMOS body terminal is tied to V_{CC} , $V_{SB} = -V_{CC}$. Thus the body-effect increases, which in turn increases $-V_{tp}$. Thus the minimum voltage increases.
 When the input is high, the output is $V_{CC} - V_{tn}$. Hence $V_{SB} = V_{tn}$. When we tie the body of the NMOS to the ground, $V_{SB} = V_{CC}$. The body effect increases, increasing V_{tn} , which in turn reduces the maximum output voltage.
 The net effect is that the output voltage swing reduces when we tie the NMOS body to the ground and the PMOS body to V_{CC} . [6.0 pts]

(iii) In 0 to 1 transition, the output goes from $-V_{tp}$ to $V_{CC} - V_{tn}$ and it takes t_R , which is equal to :
 $t_R = 0.69R_{eqPMOS} \cdot C_L$ therefore power consumption would :

$$P_R = V_{CC} \cdot I_P = V_{CC} \cdot \frac{(V_{CC} - V_{tn} - |V_{tp}|)C_L}{t_R}$$

In 1 to 0 transition, the output goes from $V_{CC} - V_{tn}$ to $-V_{tp}$ and it takes t_F , which is equal to :

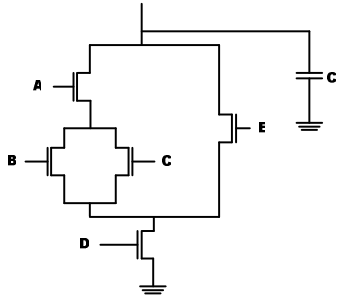
$$t_F = 0.69R_{eqNMOS} \cdot C_L \text{ therefore power consumption would be :}$$

Perm No. _____

$$P_F = V_{CC} \cdot I_N = V_{CC} \cdot \frac{(V_{CC} - V_m - |V_{tp}|)C_L}{t_F}$$

[8.0 pts]

3. (15 pts) (suggested time: 10 minutes) All transistors in the NMOS pull-down network below have a (L/W) ratio of α . Determine the best-case τ_{pHL} , if the worst-case (neglect body-effect) τ_{pHL} is 9 ns.



Solution :

Worst case path (ABD) or (ACD)

[5.0 pts]

Then worst-case $\tau_{pHL} \propto \left(\frac{L}{W}\right)_{ABD} \text{ or } \left(\frac{L}{W}\right)_{ACD} = 3 \times \left(\frac{L}{W}\right)_A = 3\alpha$

[3.0 pts]

Best case when all transistors are ON.

Therefore equivalent

$$\left(\frac{L}{W}\right)_{NMOS} = \alpha + (\alpha // (\alpha + \alpha // \alpha)) = \alpha + (\alpha // (\alpha + 0.5\alpha)) = \alpha + (\alpha // 1.5\alpha) = \alpha + \frac{3}{5}\alpha = 1.6\alpha \quad [4.0 \text{ pts}]$$

Since $\frac{\tau_{pHL_best-case}}{\tau_{pHL_worst-case}} = \frac{1.6}{3}$ therefore $\tau_{pHL_best-case} = 9ns \times \left(\frac{1.6}{3}\right) = 4.8ns$

[3.0 pts]

4. (15 pts) (suggested time 5 minutes) Draw an n-input pseudo-NMOS NAND gate. If this gate is being used to drive a total external load capacitance of C_L , and there are internal capacitances (between each of the NMOS transistors in the pull-down network), how will you size the transistors (relative to each other) so that the pull-down delay is minimum? What is the logical effort of this gate?

Solution:

(1) Since the internal capacitances are considered, the top NMOS needs to have bigger (W/L) ratio [5.0 pts]

i.e. $W_1 < W_2 < W_3 < W_4 \dots W_{n-1} < W_n$ (shown in the figure) [5.0 pts]

(2) Logical Effort:

For pseudo-NMOS logic, gate input is not connected to the PMOS. Hence, the logical effort of a pseudo-NMOS NAND gate would be less than that of a CMOS NAND gate. In addition, the size of each NMOS transistor is different, logical effort for each input in the pull down network would be different in this case. The logical effort of i^{th} input gate is equal to the average of logical efforts of pull-up (g_u) and pull-down (g_{di}) networks.

Logical effort for the i^{th} input $g_i = \frac{g_u + g_{di}}{2}$

[5.0 pts]

$$g_u = (W_{PMOS} / W_{Inverter-NMOS}) / 3$$

$$g_{di} = \frac{W_i / W_{Inverter-NMOS}}{3}$$

