

1.

- a. Assume the following timing for the input  $I$ . Draw the timing diagram for the signals  $a$ ,  $b$ ,  $c$ ,  $d$  and  $e$ . Include the clock in your drawing.

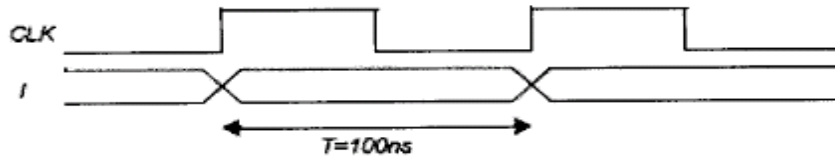
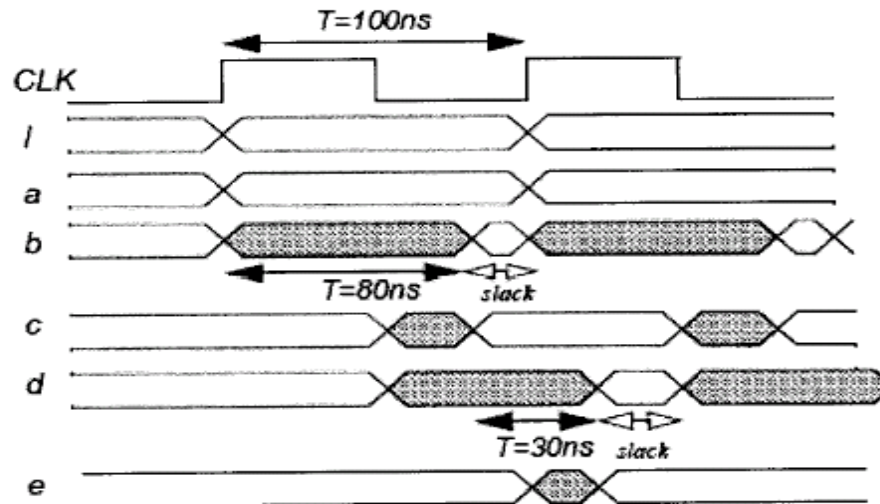


Figure 0.6 Input timing

Solution



- b. State the deadline for the computation of the signal  $b$  and  $d$ , i.e. when is the latest time they can be computed, relative to the clock edges. In your diagram for part (a), label with a “ $\leftarrow$ ” the “slack time” that the signals  $b$  and  $d$  are ready before the latest time they must be ready.

Solution

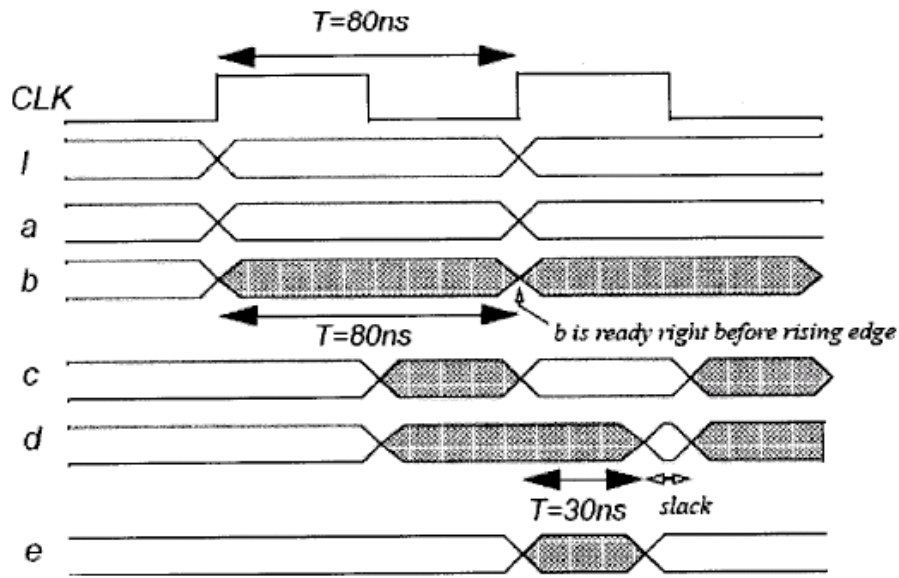
$b$  should be ready before the rising edge of  $CLK$  for the negative latch to latch and hold its value.  $d$  should be ready before the falling edge of  $CLK$  for the second positive latch to latch and hold its value.

- c. Hence deduce how much the clock period can be reduced for this shortened pipeline. Draw the modified timing diagram for the signals  $a$ ,  $b$ ,  $c$ ,  $d$ , and  $e$ . Include the clock in your drawing.

Solution

The clock can be reduced by 20 ns.

In general, it may be difficult to identify how much slack can be removed from the



clock because it depends on the length of the pipeline too.

2. The generic SRAM cell as shown below requires 6 transistors per bit. At first, it seems like the margins in such a memory cell should be good, since it contains two CMOS inverters, which we know have large margins. However, the problems are associated with those access devices connected to the cell. When cell is not accessed, it has great margins; when access devices are on, they act like load devices. Capacitance on bit lines is large enough to act like a voltage source.

Two issues that people will concern are:

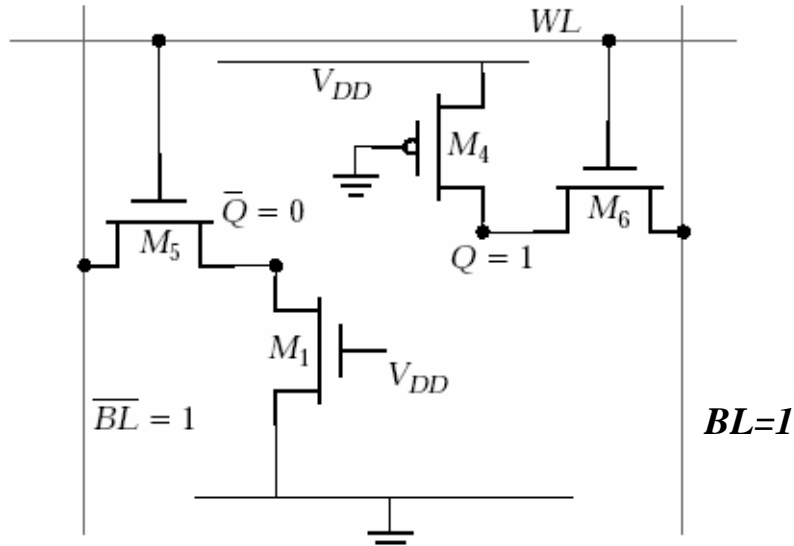
- 1) Can I read the cell and not write it;
- 2) Can I write the cell when I want to.

We will analyze these in this problem (ignore body effect, short channel effect).

a) Read Operation

Assume first that node  $Q$  is in the "1" state, we further assume that both bit line are precharged to  $V_{dd}, 2.5\text{V}$ , before the read operation is initiated. Suppose that noise margin of inverter is  $0.7V$ . Please find out the dimension ratio of  $M_5$  and  $M_1$  to avoid "read upset" under the WORST case.

The read cycle is started by asserting the word line, enabling both transistors  $M_5$  and  $M_6$ . During a correct read operation, the values stored in  $Q$  and  $\bar{Q}$  are transferred to the bit lines by leaving BL at its precharge value and by discharge  $\bar{BL}$  through  $M_1 - M_5$ . A careful sizing of the transistors is necessary to avoid accidentally writing a "1" into the cell. This type of malfunction is called "read upset".



Initially, upon the rise of the WL, the intermediate node between these two NMOS transistors  $M_1$  &  $M_5$ ,  $\bar{Q}$ , is pulled up toward the precharge value  $\overline{BL}$ . This voltage rise of  $\bar{Q}$  must stay low enough not to switch inverter of  $M_3$  and  $M_4$ , which will flip the cell. It is necessary to keep the resistance of transistor  $M_5$  large enough to prevent this from happening. The boundary constraints on the device sizes can be derived by solving the current equation at the maximum allowed value of the voltage ripple  $\Delta V$ , which is 0.7V in this case.

Both  $M_5$  and  $M_1$  are in velocity saturation region.

$$k'_n \left(\frac{W}{L}\right)_{M5} [(V_{dd} - \Delta V - V_{t,0})V_{DSATn} - \frac{V_{DSATn}^2}{2}] = k'_n \left(\frac{W}{L}\right)_{M1} [(V_{dd} - V_{t,0})V_{DSATn} - \frac{V_{DSATn}^2}{2}]$$

$$\frac{(W/L)_{M1}}{(W/L)_{M5}} = \frac{(2.5 - 0.7 - 0.4) \cdot 0.63 - \frac{0.63^2}{2}}{(2.5 - 0.4) \cdot 0.63 - \frac{0.63^2}{2}} = 0.6$$

We want that we size our transistors larger than the ratio given above to avoid “read upset”. In reality, BL clamps Q to  $V_{dd}$ , makes the inadvertent toggling of the cross-coupled inverter pair difficult. (One advantage of have this dual bit line architecture).

b) In the above process, what the critical sizing will be if the bit lines are precharged to  $V_{dd}/2$  instead?

Now,  $M_1$  is still in velocity saturation, but  $M_5$  is in triode region now.

$$k'_n \left(\frac{W}{L}\right)_{M5} [(V_{dd} - \Delta V - V_{t,0})V_{DS,M5} - \frac{V_{DS,M5}^2}{2}] = k'_n \left(\frac{W}{L}\right)_{M1} [(V_{dd} - V_{t,0})V_{DSATn} - \frac{V_{DSATn}^2}{2}]$$

$$V_{DS,M5} = \frac{V_{dd}}{2} - \Delta V$$

$$\frac{(W/L)_{M1}}{(W/L)_{M5}} = \frac{(2.5 - 0.7 - 0.4) \cdot (1.25 - 0.7) - \frac{(1.25 - 0.7)^2}{2}}{(2.5 - 0.4) \cdot 0.63 - \frac{0.63^2}{2}} = 0.55$$

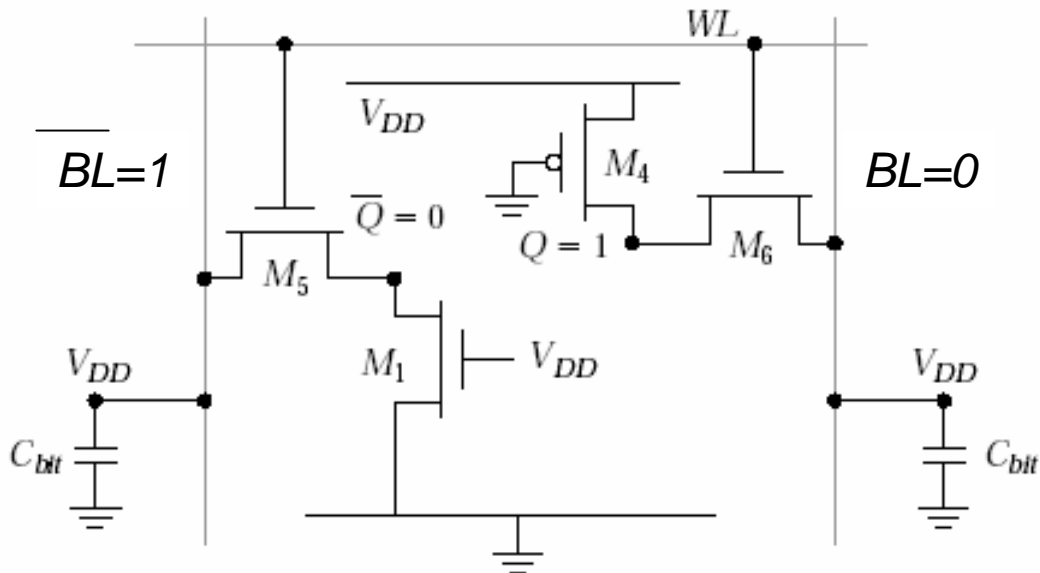
It could be inferred that precharging it to  $V_{dd}/2$  will help to prevent “read upset”. The “threshold” condition is loosened comparing to part a). But now, you need check if  $M_4$  &  $M_6$  are sized correctly.

c) Write operation

Assume that a “1” is stored in the cell. A “0” is written in the cell by setting  $\overline{BL}$  to “1” and  $BL$  to “0”. The noise margin is given as in part a). What is the ratio of  $M_4$  and  $M_6$  to guarantee a successful write operation?

A “0” is written in the cell by setting  $\overline{BL}$  to “1” and  $BL$  to “0”. During the initiation of a write, it is reasonable to assume that the gates of  $M_1$  and  $M_4$  stay at  $V_{dd}$  and GND respectively as long as the switching has not commenced.

Note that  $\overline{Q}$  side of the cell cannot be pulled high enough to ensure the writing. The sizing constraint, imposed by the read stability, ensures that this voltage is kept below 0.7V. Therefore, the new value of the cell has to be written through  $M_6$ .



A reliable writing of the cell is ensured if we can pull node Q low enough. The condition for this to occur can be derived by equaling current of M<sub>4</sub> and M<sub>6</sub>. Note that M<sub>4</sub> is in triode region, and M<sub>6</sub> is in velocity saturation.

$$k'_p \left(\frac{W}{L}\right)_{M4} [(V_{dd} - |V_{T,0}|) |V_{DS,p}| - \frac{V_{DS,p}^2}{2}] = k'_n \left(\frac{W}{L}\right)_{M6} [(V_{dd} - V_{t,0}) V_{DSATn} - \frac{V_{DSATn}^2}{2}]$$

$$|V_{DS,p}| = V_{dd} - V_Q = \Delta V$$

Same as part a),  $\Delta V = 0.7V$

$$\frac{(W/L)_{M4}}{(W/L)_{M6}} = \frac{115 \cdot [(2.5 - 0.4) \cdot 0.63 - \frac{0.63^2}{2}]}{30 \cdot [(2.5 - 0.4) \cdot 0.7 - \frac{0.7^2}{2}]} = 3.5$$

So we want to size transistors of M<sub>4</sub> and M<sub>6</sub> with smaller ratio than 3.5 to ensure write ability.

In real design, this is a symmetrical cell, so we will size M<sub>5</sub> and M<sub>6</sub> equally. Then size the rest of transistors according to the design equations you just derived.

### 3.

- (a) Because we are using an NMOS transistor to pull up the voltage on the capacitor C<sub>S</sub>, it only charges up to V<sub>DD</sub>-V<sub>T</sub>. V<sub>T</sub>, of course, is increased by the body effect, which is dependent on the voltage stored in the cell. By iteration, you can solve for this voltage (something you have done a gazillion times in this class):

$$V_{DD} - V_T = V_S$$

$$V_{DD} - [V_{T0} + \gamma(\sqrt{2\phi + V_S} - \sqrt{2\phi})] = V_S$$

$$V_S = 1.86V$$

- (b) During this operation, charge sharing occurs between C<sub>S</sub> and C<sub>BL</sub>

$$C_S V_S + C_{BL} V_{BL} = (C_S + C_{BL}) V_{final}$$

$$V_{final} = (50 \cdot 1.86 + 450 \cdot 1.25) / (50 + 450) = 1.31 V$$