

UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering

ECE225 High-Speed Digital IC Design

Homework #1

Due Date: Feb 1 by 5:00pm

- 1. Reading Assignment:** Chapter 5 and 6 of the book:
Digital Integrated Circuits: A Design Perspective (2nd Edition), Jan M. Rabaey et al., Prentice Hall, 2003.
- Design, layout, and simulate a CMOS four-input XOR gate in the standard 0.18 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use: you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 1.8V. Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit. The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.3 ns and occupy an area of no more than 350 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay. The design will be graded on the magnitude of the product of the area of your design and the square of the delay for the worst-case transition.
- Write a report detailing the various challenges in incorporating interconnect effects while using the logical effort method for performance optimization of combinational logic gates. Include a comprehensive list of all previous and related works in the literature. Discuss possible ways to incorporate the effect of interconnects.
(You may want to refer to the book on Logical Effort by Sutherland and Sproul)