UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering

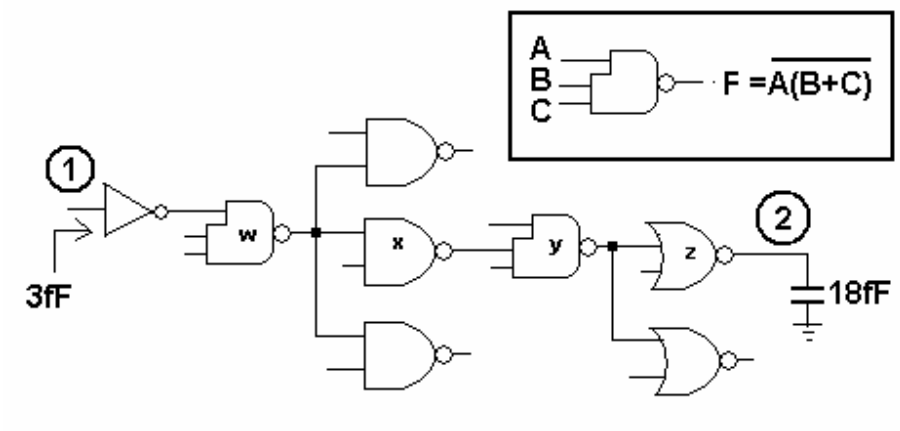
ECE225 *High-Speed Digital IC Design*

Homework #1

Due Date: Feb 4 by 5:00pm

1. ***Reading Assignment:*** Chapter 5 and 6 of the book:
   Digital Integrated Circuits: A Design Perspective (2nd Edition), Jan M. Rabaey et al., Prentice Hall, 2003.

2. *Logic and Logical Effort*



a) A three-input XNORT gate (see insert above) works like a two-input NOR as long as input A is high; otherwise, the output is stuck high. Implement the XNORT gate in complementary CMOS, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. Find the logical effort associated with each input.
b) Assuming all input combinations are equally likely, what is the transition activity (probability) of a XNORT gate? Averaged over many cycles, will a XNORT gate typically consume more or less power than a two-input NOR gate, if they both drive equally large output loads? What about a two-input XOR?
c) For the logic path from node (1) to node (2) shown in the figure above, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?
d) Find the input capacitances {w, x, y, z} necessary for each of the gates in the path in order to achieve the optimum effort per stage.

3. Write a report detailing the various challenges in incorporating interconnect effects while using the logical effort method for performance optimization of combinational logic gates. Include a comprehensive list of all previous and related works in the literature. Discuss possible ways to incorporate the effect of interconnects.
   (You may want to refer to the book on Logical Effort by Sutherland and Sproul)