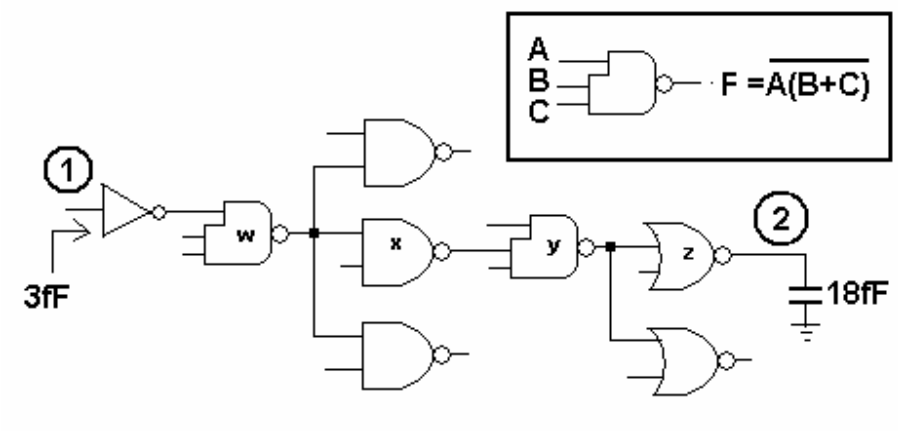
Logic and Logical Effort



a) A three-input XNORT gate (see insert above) works like a two-input NOR as long as input A is high; otherwise, the output is stuck high. Implement the XNORT gate in complementary CMOS, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. Find the logical effort associated with each input.

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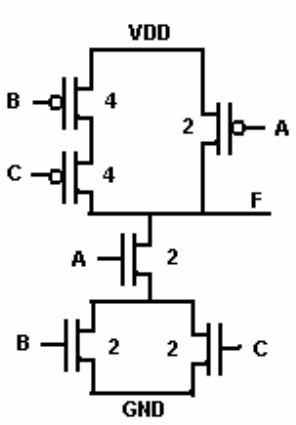

The complementary CMOS implementation is to the left. Logical effort is defined as the ratio of input capacitance of a gate (considering only one input) to the input capacitance of an inverter with the same output current. This gives us:

- $g_A=(2+2)/(2+1)=4/3$
- $g_B=(4+2)/(2+1)=2$
- $g_C=(4+2)/(2+1)=2$

b) Assuming all input combinations are equally likely, what is the transition activity (probability) of a XNORT gate? Averaged over many cycles, will a XNORT gate typically consume more or less power than a two-input NOR gate, if they both drive equally large output loads? What about a two-input XOR?

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

The transition probability of the gate is
$P(F:0\rightarrow1) = P(F=0)P(F=1) = 3/8 \bullet 5/8 = 15/64 \approx 0.23$

The transition probability of a two-input NOR (again with all inputs assumed equally likely) is 3/16 ≈ 0.19, lower than the XNORT. With the simplifying assumption that the output load is large (which lets us forget about differences in intrinsic capacitance), we can confidently assert that the XNORT will on average consume more dynamic power.

The transition probability of a two-input XOR is 0.25, which is slightly more than the XNORT. Therefore, we would expect the XNORT to consume less power, on average.

c) For the logic path from node (1) to node (2) shown in the figure above, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?

A missing piece of information in this problem is the size of the gates that are off-path. For simplicity, these can be assumed to be sized equal to the on-path gate of the same type, whatever that is chosen to be.

The path branching effort (product of stage branching efforts, which are the ratios of total driven capacitance to capacitance driven on the path) is:

$B = 1 \bullet 3 \bullet 1 \bullet 2 \bullet 1 = 6$

The path electrical effort (ratio of output capacitance to input capacitance) is:

$F = C_L/C_{in} = 18fF/3fF = 6$

The path logical effort (product of stage logical efforts), using results from both the lectures and earlier in this problem, is:

$G = g_{inv} \bullet g_{xnort,a} \bullet g_{nand} \bullet g_{xnort,b} \bullet g_{nor} = 1 \bullet 4/3 \bullet 4/3 \bullet 2 \bullet 5/3 = 160/27$

The total path effort is then $H = GBF = 160/27 \bullet 6 \bullet 6 = 160 \bullet 4/3$.

The optimum effort per stage for this five stage path is $H^{1/5} \approx 2.92$.

d) Find the input capacitances {w, x, y, z} necessary for each of the gates in the path in order to achieve the optimum effort per stage.

The electrical effort for the nor (last gate in the path) is:
$f = C_L/z$
The effort for the stage is $h = gf \Rightarrow z = g_{nor}C_L/f \approx (5/3)/(2.9)\ 18fF \approx 10.3fF$

The electrical effort for the second xnort is:
$f \approx 2 \bullet 10.3fF/y$
Here, $y \approx 20.6fF\ g_{xnort,b}/h \approx 20.6fF\ 2/2.92 \approx 14.1fF$.

The electrical effort for the nand is:
$f \approx 14.1fF/x$
$x \approx 14.1fF\ g_{nand}/h \approx 14.1fF\ (4/3)/\ 2.92 \approx 6.4fF$

The electrical effort for the first xnort is:
$f \approx 3 \bullet 6.4fF/w$
$w \approx 19.2fF\ \ g_{xnort,a}/h \approx 19.2fF\ (4/3)/2.92 \approx 8.8fF$

As a check, we see that the first stage effort is
$h = g_{inv}f = 1 \bullet 8.8fF/3fF \approx 2.93$, which closely matches our calculated optimum effort per stage.