UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering

ECE225 *High-Speed Digital IC Design*

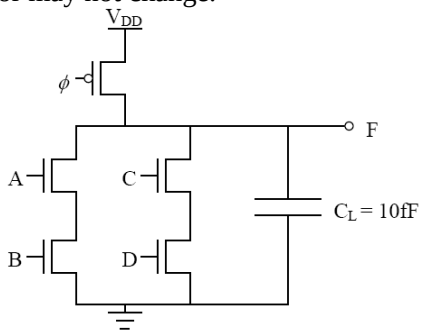
Homework #2

Due Date: Feb 23 by 5:00pm

1. Reading Assignment: Chapter 4 and 9 of the book:
Digital Integrated Circuits: A Design Perspective (2nd Edition), Jan M. Rabaey et al., Prentice Hall, 2003.

2. Draw the transistor level schematic of a 4-1 Multiplexer with;
a) transmission gate
b) pass transistor logic
c) pass transistor with restoring logic
d) static CMOS
e) Implement all above logic families in Hspice, use 65 nm technology. Compare power, delay and power-delay product of different multiplexers in room temperature.
f) Change temperature to 100^{o} C and repeat part (e).

3. A dynamic logic gate is shown below. During the pre-charge phase ($\varphi = 0$) output F is charged to VDD and it is given that A = B = C = D = 0V. During the evaluate phase ($\varphi = 1$), any of these inputs may or may not change.

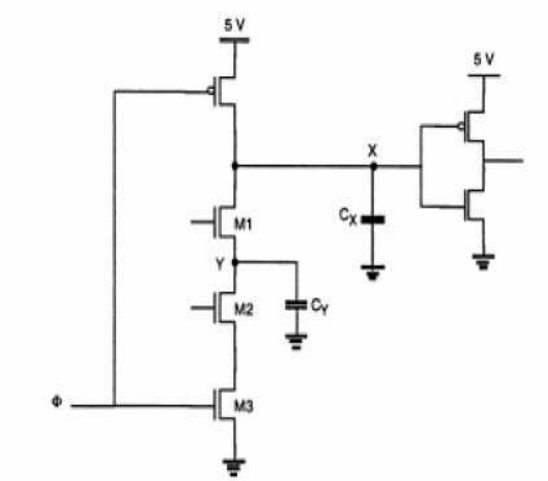


a) What is the worst-case combination of input transitions in terms of charge sharing? That is, what input combination will corrupt F the most when the output is supposed to remain high?

b) For the worst-case identified in part (a), what is the final voltage at node F? Use VDD = 1.5V, NMOS model VTH0 = 0.5V, $\gamma = 0.4$V, $2\varphi F = 0.6$V, assume that Cdb = Csb = 1fF for all transistors and ignore gate capacitance.

c) In addition to the charge sharing calculated in part (b), now assume that there is also a constant leakage current of 2nA discharging node F to ground. What is that *minimum* clock speed that this gate can operate at if the next gate has VIH = 1.0V? Assume that clock φ is high and low for equal periods of time.

4. Consider the CMOS logic circuit in figure below, which is a simple Domino circuit. Node X is connected to a CMOS inverter so that the output of the inverter can be directly fed to the next stage of the domino circuit.



a) Explain how the voltage level at node X, after it is pre-charged to 5 V, can be affected during "evaluate" by the charge sharing between node X and node Y. Express the final voltage at node X in terms of the initial voltage at node Y, when the charge sharing is completed following the full pre-charge operation. During pre-charge, the gate terminal of the transistor M2 is fixed at 0 V.

b) Determine the ratio between device transconductance parameters, k_p and k_n, of the inverter to prevent any logic error due to charge sharing between nodes X and Y under all circumstances. Assume that the magnitudes of threshold voltages in the inverter are equal to 1.0 V.

5. Multi-core designs are being adopted for future generations of high-performance ICs including microprocessors (see www.intel.com). For multi-core architectures, which alleviate power dissipation problems, interconnects are going to play a key role in determining the design and performance of such ICs. Write a report (*6 page, IEEE style*) detailing the main philosophy behind multi-core designs and its various challenges. In particular, discuss the role of interconnects. Include a comprehensive list of all previous and related works in the literature. Discuss (and quantify, if possible) various implications of interconnect variations on multi-core architectures.