# ECE 225
# High Speed Digital IC Design
## Lecture 2

## Discussion of Projects

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# Project Topics….design oriented

1. **Circuit Design Issues: (nanometer scale)**

   a. Variation/error tolerant design
   b. Low power design under noise margin, performance and area considerations: SRAM, DRAM, Flash, dynamic circuits, keepers etc.
   c. **Ultra low-voltage design/Sub-threshold circuit design**

2. **Device Circuit Co-design (emerging technologies):**

   a. Non-classical CMOS – SOI, FinFET, GAAFET.
   b. Non-Si Devices – CNFET, NWFET, SpinFET, Graphene-FET, NEMFET.
   c. Novel memory technologies like MRAM, FRAM, PCM etc.
   d. **Sub-kT/q devices – Tunnel FETs, IMOS, Fe-FET etc.**
   e. **Energy Management with Nanoelectronics: energy conversion, scavenging….**

3. **Interconnect System Design:**
   a. Variation aware design – signal, clocking, P/G (power / ground) Networks.
   b. Interconnect variations: parasitic (R,L,C) extraction, modeling and optimization
   c. Modeling of VHF (Very High Frequency) signals….substrate effects.
   d. Optimal inductor design
   e. Emerging Carbon nanotube and Graphene nano-ribbon based interconnects
   f. **Interconnects design and modeling for 3-D ICs: TSV design, alternate interconnection schemes (via C or L coupling)**

# Project Deadlines….

- Preliminary report due: Jan 30
  - At least complete literature review and identify problems to be addressed within a given topic.
  - Show some initial analysis….
- Final project presentations: during the last week of class (~ 30 mins per student)
- Final project report due in March (end of last week of class)