

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

CIRCUITS & ELECTRONICS I ECE 137A

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Name: Solutions

This is open book and open notes exam. For all questions make reasonable approximations. Unless otherwise specified *ignore body effect*. Relevant equations are given at the back of the examination for your convenience . GOOD LUCK!

Answer the questions in the spaces provided on the question sheets. If you run out of room for an answer, continue on the back of the page.

Question	Points	Score
1	35	
2	30	
3	35	
Total:	100	

1.

Question 1: 35points

a As you are perusing your old 2C notes you come across the op-amp RC integrator. You wonder what would happen if you replace the resistor with a MOSFET biased in the linear region as shown in figure 1. *NOTE: Linear does not mean you can ignore the V_{ds}^2 dependency, please use the full linear equation for the entire problem.*

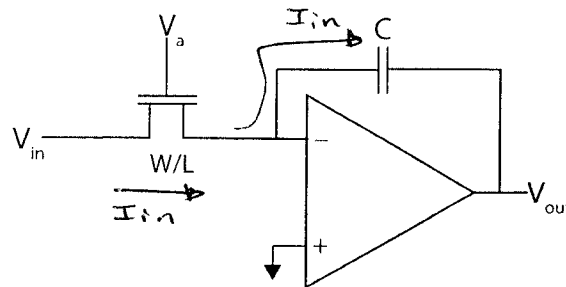


Figure 1: Circuit for Question 1

- (a) (10 points) Derive an expression for the output voltage V_{out} as a function of V_{in} and V_a

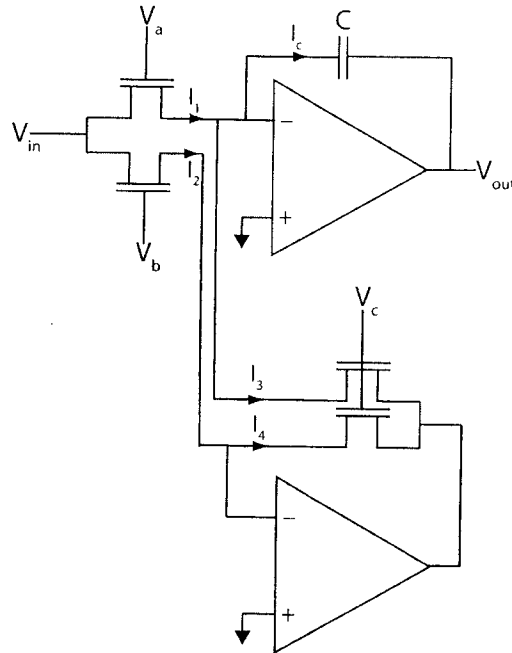
$$I_{in} = k_n \left(\frac{W}{L}\right) (V_a - V_{th} - \frac{V_{in}}{2}) v_{in}$$

$$I_{in} = -C \frac{dv_{out}}{dt} = k_n \left(\frac{W}{L}\right) (V_a - V_{th} - \frac{V_{in}}{2}) v_{in}$$

$$dv_{out} = -\frac{1}{C} k_n \left(\frac{W}{L}\right) (V_a - V_{th} - \frac{V_{in}}{2}) v_{in} dt$$

$$v_{out} = -\int_0^t \frac{1}{C} k_n \left(\frac{W}{L}\right) (V_a - V_{th} - \frac{V_{in}}{2}) v_{in} d\tau$$

You notice however when V_{in} is large that the circuit exhibits non-linear behavior due to the V_{ds}^2 term. You share this with your ECE 137A professor who shows you the circuit in figure a where all the transistors are *identical* and biased to be operating in the *linear* region and says that this should solve all your problems.



All transistors are identically sized and equal to W/L

Figure 2: Improved Circuit for Question 1

- (b) (10 points) Derive expressions for the currents I_1, I_2, I_3, I_4 and I_c is there a relationship between them?

$$I_1 - I_3 - I_c = 0$$

$$I_2 = I_4$$

$$I_3 = I_4$$

$$\Rightarrow I_1 - I_2 = I_c$$

$$I_c = K_n \left(\frac{W}{L} \right) (V_A - V_{th} - \frac{v_{in}}{2}) v_{in} - K_n \left(\frac{W}{L} \right) (V_B - V_{th} - \frac{v_{in}}{2}) v_{in}$$

$$= K_n \left(\frac{W}{L} \right) \left[V_A v_{in} - \cancel{V_{th} v_{in}} - \frac{v_{in}^2}{2} - V_B v_{in} + \cancel{V_{th} v_{in}} + \frac{v_{in}^2}{2} \right]$$

$$I_c = K_n \left(\frac{W}{L} \right) (V_A - V_B) v_{in}$$

- (c) (5 points) *Qualitatively* explain how circuit works and why it solves the issues with the V_{ds}^2 term

The output current I_c is the difference between I_1 and I_2 , and the V_{ds}^2 term is subtracted out. I_c depends only on $(V_A - V_B)v_{in}$.

The second op-amp copies the current in transistor controlled by V_B and reverses its direction, subtracting it from the current from the transistor controlled by V_A , this cancels out the V_{ds}^2 nonlinearity since both transistor have the same V_{ds} enforced by the virtual ground of the op-amp due to negative feedback

- (d) (10 points) Derive an expression for the output voltage V_{out} as a function of V_{in} , V_a and V_b

$$I_c = -C \frac{dv_{out}}{dt} = k_n \left(\frac{W}{L} \right) (V_A - V_B) v_{in}$$

$$dv_{out} = -\frac{1}{C} k_n \left(\frac{W}{L} \right) (V_A - V_B) v_{in} dt.$$

$$v_{out} = -\int_0^t \frac{1}{C} k_n \left(\frac{W}{L} \right) (V_A - V_B) v_{in} d\tau$$

2.

Question 2: 30points

Transistors, especially BJT's are highly nonlinear devices. However, one can exploit this non-linearity to design new computational circuits. One useful embodiment of this is shown in figure 3

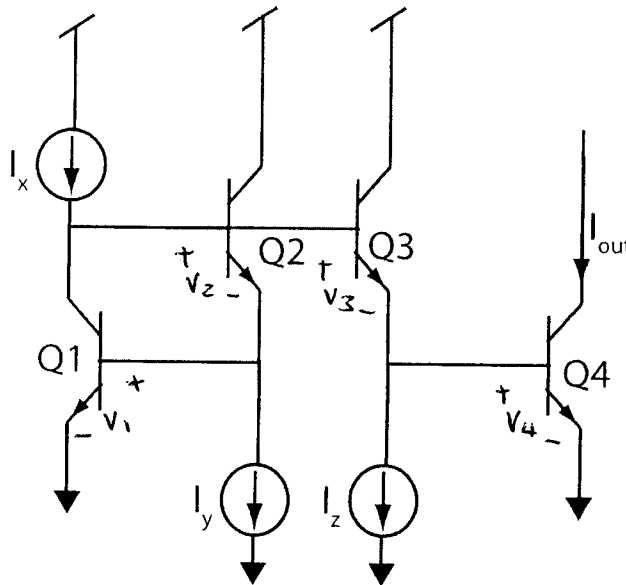


Figure 3: Circuit for Question 2a

- (a) (15 points) What function does this circuit implement i.e. derive I_{out} in terms of I_x , I_y and I_z

$$V_1 + V_2 - V_3 - V_4 = 0 \Rightarrow V_1 + V_2 - V_3 = V_4$$

$$V_1 = \frac{kT}{q} \ln\left(\frac{I_x}{I_s}\right)$$

$$\frac{kT}{q} \ln\left(\frac{I_x}{I_s} \frac{I_y}{I_s} \frac{I_s}{I_z}\right) = \frac{kT}{q} \ln\left(\frac{I_{out}}{I_s}\right)$$

$$V_2 = \frac{kT}{q} \ln\left(\frac{I_y}{I_s}\right)$$

$$V_3 = \frac{kT}{q} \ln\left(\frac{I_z}{I_s}\right)$$

$$V_4 = \frac{kT}{q} \ln\left(\frac{I_{out}}{I_s}\right)$$

$$\boxed{\frac{I_x I_y}{I_z} = I_{out}}$$

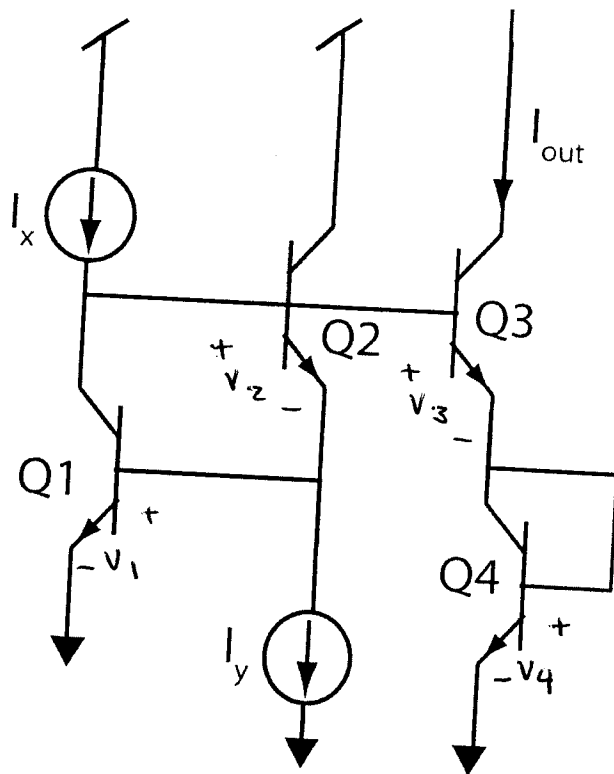


Figure 4: Circuit for Question 2b

- (b) (15 points) If we now set $I_z = 0$ and connect a diode connect transistor at the emitter of Q3, as shown in figure 4 and take the output out of the collector of Q3 the function changes, what would this function be?

$$v_1 + v_2 - v_3 - v_4 = 0$$

$$\Rightarrow v_1 + v_2 = v_3 + v_4$$

$$\Rightarrow \frac{kT}{q} \ln\left(\frac{I_x}{I_s} \cdot \frac{I_y}{I_s}\right) = \frac{kT}{q} \ln\left(\frac{I_{out}}{I_s} \cdot \frac{I_{out}}{I_s}\right)$$

$$I_x I_y = I_{out}^2$$

$$I_{out} = \sqrt{I_x I_y}$$

3.

Question 3: 35points

The cascode is useful technique that you will learn later, in this problem you will learn how to optimally bias the cascode. As supply voltages shrink every small bit counts so we generally would like to bias our MOS devices at the edge of saturation i.e.

For an NMOS device $V_{ds} = V_{gs} - V_{tn}$

Now $V_{gs} - V_{tn}$ keeps appearing everywhere so circuit designers have developed a shorthand for it and some call it V_{eff} for the *effective voltage* that drives the transistor. If two transistors are placed in series, as shown in figure 5, then the minimum gate voltage that they both can possess while having them both in saturation can be derived as follows. Both transistors carry the same current therefore they must have the same gate source voltages the minimum V_{ds} for the bottom transistor is V_{eff} , therefore the gate voltage of the top device needs to offset by a V_{eff} resulting in $V_{tn} + 2V_{eff}$ as shown in figure 5.

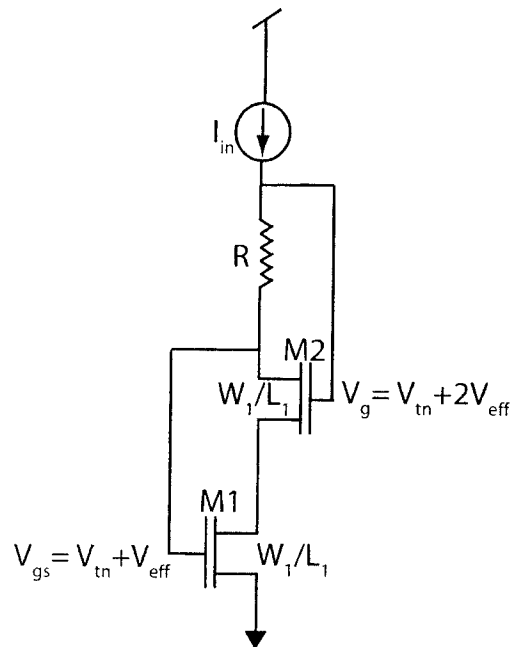


Figure 5: Circuit for Question 3a

- (a) (5 points) Design the resistor R such that you can generate this bias, you need to only come up with an equation

$$\frac{(V_g - V_{gs})}{R} = I_{in}$$

$$R = \frac{V_{eff}}{I_{in}}$$

$$\frac{V_{tn} + 2V_{eff} - V_{tn} - V_{eff}}{R} = I_{in}$$

- (c) (25 points) Size M3 and M4 such that the right voltage is generated. (Hint: W/L of all transistors are related).

if we pick $\boxed{\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_1}$

then $V_{gs4} = V_{gs}$ since both M4 and M1 are carrying the same current I_{in}

$$V_{gs4} = V_x - V_g$$

$$\Rightarrow V_{tn} + V_{eff} = V_x - (V_{tn} + 2V_{eff})$$

$$V_x = 2V_{tn} + 3V_{eff}$$

We know that M3 is in linear region:

$$I_{in} = k_n \left(\frac{W}{L}\right)_3 \left[(V_x - V_{gs}) - V_{tn} - \frac{V_{ds3}}{2} \right] V_{ds3}$$

$$V_{ds3} = V_g - V_{gs} = V_{eff}$$

$$\Rightarrow I_{in} = k_n \left(\frac{W}{L}\right)_3 \left[(2V_{tn} + 3V_{eff} - V_{tn} - V_{eff}) - V_{tn} - \frac{V_{eff}}{2} \right] V_{eff}$$

$$I_{in} = k_n \left(\frac{W}{L}\right)_3 \frac{3}{2} V_{eff}^2$$

$$\text{But } I_{in} = \frac{k_n}{2} \left(\frac{W}{L}\right)_1 (V_{gs} - V_{tn})^2 = \frac{k_n}{2} \left(\frac{W}{L}\right)_1 V_{eff}^2$$

$$\Rightarrow \frac{k_n}{2} \left(\frac{W}{L}\right)_1 V_{eff}^2 = k_n \left(\frac{W}{L}\right)_3 \frac{3}{2} V_{eff}^2$$

$$\left(\frac{W}{L}\right)_1 = 3 \left(\frac{W}{L}\right)_3 \quad \text{or} \quad \boxed{\left(\frac{W}{L}\right)_3 = \frac{1}{3} \left(\frac{W}{L}\right)_1}$$

