

Problem Set 6 Solutions

1.

(a) The gate voltage of transistor M2, $V_G = V_{ref} + V_{gs2} = V_{ref} + V_{eff} + V_T$

V_{ref} is given. V_{gs2} is the DC voltage across the gate and source of M2, which is determined by the bias current and W/L ratio of M2. You don't need to find the exact number of V_{gs2} , since bias current and W/L ratio are not given.

(b) A is usually very large, so the negative feedback loop forces the source voltage of M2 to be equal to V_{ref} . Thus, the drain voltage of transistor M1 is V_{ref} .

(c) The output impedance of the circuit,

$$R_{OUT} = R_L \parallel (r_{O2} + r_{O1} + g_{m2}(1+A)r_{O2}r_{O1})$$

The feedback amplifier effectively increases g_{m2} by $(1+A)$. After you understand this point, you can treat the active cascode stage as a simple cascode stage with an enhanced transconductance for M2. The rest is the same. The purpose of the feedback amplifier is two-fold: set the gate bias voltage of M2, enhance the output impedance of the cascode stage. It doesn't change the transconductance of the whole amplifier.

(d) The small signal input impedance looking into the source of transistor M2

$$\approx \frac{1}{(1+A)g_{m2}}$$

The reason is the same as above: The feedback amplifier effectively increases g_{m2} by $(1+A)$.

(e) The minimum voltage the o/p of this stage can swing to before one of the transistors drops out of saturation = $V_{ref} + V_{eff}$

This is found by simply subtracting the gate bias voltage of M2 by V_t (threshold voltage). If the drain voltage of M2 is lower than its gate voltage by V_t , then M2 is in linear region, and it essentially becomes a small resistor.

(f) The small signal gain of this circuit $\approx g_{m1} \times [g_{m2}(1+A)r_{O2}r_{O1} \parallel R_L]$

2.

(a) The gate voltage of transistor M2 = $V_{gs3} + V_{gs2}$

Common source amplifier of M3 provides of the feedback, and Vref is now given by Vgs3. A is $g_{m3} * r_{o3}$ (assuming the top current source is ideal).

After you understand the first problem, the rest of this problem is simply the same.

(b) The output impedance of the circuit, $R_{OUT} = R_L \parallel [g_{m2}(1 + g_{m3}r_{o3})r_{o2}r_{o1} + r_{o1} + r_{o2}]$

(c) The minimum voltage the o/p of this stage can swing to = $V_{gs3} + V_{gs2} - V_T$

(d) The small signal gain of this circuit

$$\approx g_{m1} \times [R_L \parallel g_{m2}(1 + g_{m3}r_{o3})r_{o2}r_{o1}]$$

