University of California, Santa Barbara

Department of Electrical & Computer Engineering

Circuits & Electronics II ECE 137B

Professor Theogarajan

Midterm Exam II, May 26, 2010

Name: MODEL ANSWER

This is open book and open notes exam. For all questions make reasonable approximations. All design curves are given at he back of the exam. Show all your work, any answers without explanations will not be given credit . GOOD LUCK!

Answer the questions in the spaces provided on the question sheets. If you run out of room for an answer, continue on the back of the page.

Question	Points	Score
1	100	
Total:	100	

1. Question 1: 100points

(a) (10 points) Calculate the small-gain, in terms of device parameters, of the differential amplifier shown in figure 1. *Transistors* $M_{Bn1}, M_{Bn2}, M_{Bn3}, M_{Bp1}, M_{Bp2}$ *and* M_{Bp3} *are there for biasing purposes and do not play a role in the gain calculation*

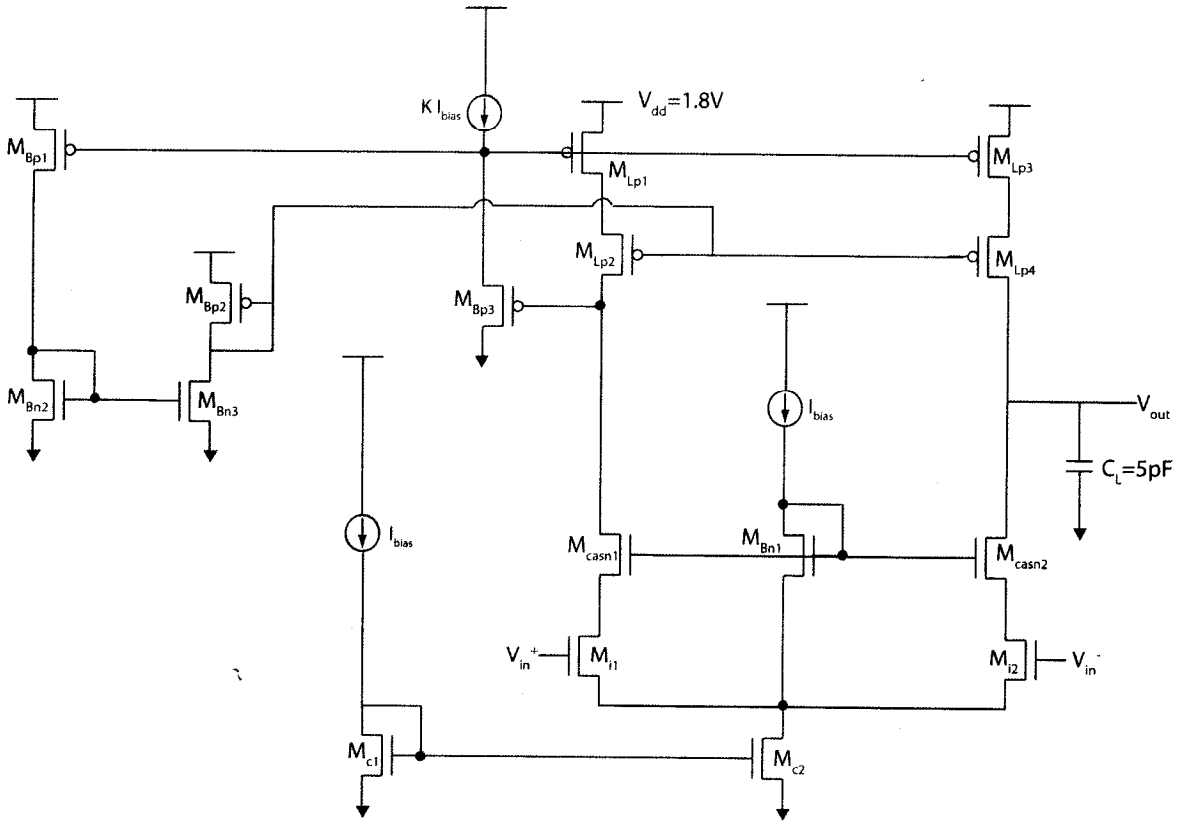


Figure 1: A telescopic cascode amplifier

Gain = $g_{m_{i_{1,2}}} \cdot R_{out}$

$R_{out} = (g_{m_{n_2}} r_{o_{n_2}} r_{o_{i_2}}) \,//\, (g_{m_{p_4}} r_{o_{p_4}} r_{o_{p_3}})$

contd..

(b) (20 points) Given that the gain of the amplifier needs $\geq 70dB$ and the unity gain bandwidth $\geq 2MHz$, what is the bias current needed for this amplifier. Assume that the most dominant capcitance is the load capacitor

Unity gain B.W = DC gain * dominant pole location

$$= \frac{g_{mi_{1,2}}}{2\pi C_L} \geq 2MHz$$

$$\therefore g_{mi_{1,2}} \geq 62.8\,\mu S \Rightarrow \boxed{g_{mi_{1,2}} \geq 6.28 * 10^{-5}\ S}$$

Using Figure 2 (Note that there is no single answer for this design problem)

$I_{density} \geq 3.5\,\mu A/\mu m$ (per input device)

If we pick $I_{bias} = 8\,\mu A$ ($4\,\mu A$/device), we need to make sure that the gain condition is satisfied

At $4\,\mu A$, $g_{mi_{1,2}} \approx 6.5 * 10^{-5}$

but gain = $g_{mi_{1,2}} [g_{mn_2} r_{on_2} r_{oni_2} // g_{mp_4} r_{op_4} r_{op_3}] \geq 70dB$

$\therefore R_{out} = g_{mn_2} r_{on_2} r_{oni_2} // g_{mp_4} r_{op_4} r_{op_3} \geq 48.65\,M\Omega$

From Figure 3: $g_{mn_2} r_{on_2} \approx 80$ (for $L = 360nm$)

From Figure 4: $r_{oni_2} \approx 1.5\,M\Omega$ (for $L = 360nm$)

From Figure 7: $g_{mp_4} r_{op_4} = 68$ (For $L = 360nm$)

From Figure 8: $r_{op_3} = 2\,M\Omega$ (For $L = 360nm$)

You can choose $L = 540nm$ to boost R_{out}

This yields $R_{out} = 63.75\,M\Omega$ ∴ satisfies gain requirment

$\therefore \boxed{I_{bias} = 8\,\mu A}$ ($4\,\mu A$ per input device)

(c) (20 points) Given that the output quiescent operating point needs to be at $V_{dd}/2$ size transistors $M_{Bp3}, M_{Lp1}, M_{Lp2}, M_{Lp3}$ and M_{Lp4} and the K factor.

We want $V_{SG_{LP_1}} + V_{SG_{BP_3}} = \frac{V_{DD}}{2} = 0.9V$

Using Figure 9

For current / branch = 4μA in MLP_1, it corresponds to

$V_{SG} = 0.7V$ (For 1μm device) or 0.5 V (for 10 μm device

$L = 360nm$ $L = 360nm$

∴ we can size $\left[\left(\frac{W}{L}\right)_{MLP_1} = \left(\frac{W}{L}\right)_{MLP_3} = \left(\frac{10\,\mu m}{0.36\,\mu m}\right)\right]$

To make $V_{SG_{BP_3}} = 0.9 - 0.5 = 0.4V$, we must lower the current density flowing through M_{BP_3}

we can pick $\boxed{K = 0.1}$ ($I_{density} = 4 * 10^{-7}\ A/\mu m$)

& $\left[\left(\frac{W}{L}\right)_{M_{BP_3}} = \left(\frac{10\,\mu m}{0.36\,\mu m}\right)\right]$ to yield $V_{SG} = 0.4V$

MLP_2 & MLP_4 can be sized the same as $\left(\frac{W}{L}\right)_{MLP_1}, MLP_3$

∴ $\left[\left(\frac{W}{L}\right)_{MLP_2} = \left(\frac{W}{L}\right)_{MLP_4} = \frac{10\,\mu m}{0.36\,\mu m}\right]$

contd..

(d) (20 points) Given the gain requirement and the lowest input common voltage is 400mV what are the sizes of transistors M_{i1} and M_{i2}

$$V_{ic_{min}} = 0.4V = V_{ds_{M_{C_2 min}}} + V_{gs_{in}}$$

we can make M_{C_2} operate in subthreshold & $\therefore V_{ds_{M_{C_2 min}}} \simeq 100mV$

$\therefore$ we want $V_{gs_{in}} = 300mV$ & at the same time support $4\mu A$ of current through each device.

For $V_{gs} = 300mV$, $I_{density} = 1.5 * 10^{-8} A/\mu m = 15\ nA/\mu m$ (Figure 5)

$\therefore$ we want

$$W_{i1} = W_{i2} = \frac{4\mu A}{15\ nA/\mu m} \simeq 266.67\ \mu m$$

& $L_{i1} = L_{i2} = 360nm$ (or 540 nm)

contd...

(e) (20 points) Size the transistors M_{Bn2}, M_{Bn3}, M_{Bp1} and M_{Bp2} so the pmos cascode is optimally biased (i.e. maximum allowable swing) given $V_{dssat} = 200mV$ for strong-inversion and $V_{dssat} = 100mV$ for sub-threshold.

MLP_1 is in subthreshold & $\therefore V_{dsat} = 100mV$

$\therefore$ we want $V_{g_{MLP_2}} = 1.8 - 0.1 - 0.5 = 1.2V$

(bec MLP_2 has same size & carry same current as MLP_1 & $\therefore$ has $V_{sg} = 0.5V$)

$\therefore$ we want $V_{sg_{MBP_2}} = 0.6V$

we als know that $V_{sg_{MBP_1}} = 0.5V$

From figure 9 we see that $V_{sg_{MBP_2}} = 0.6V$ if $I_{density} \approx 2\mu A/\mu m$ ($L = 360nm$)

$\therefore$ we can make $\left(\frac{W}{L}\right)_{MBP_2} = \frac{1\mu m}{0.36\mu m}$, If we ensure that the current flowing through it = $2\mu A$

The current is determined by MBP_1 & the current mirror ratio $M_{Bn2} : M_{Bn3}$

$\therefore V_{sg_{MBP_1}} = 0.5V \therefore I_{density} = 5 * 10^{-7}\ \mu A/\mu m$

$\therefore$ we can size $\left(\frac{W}{L}\right)_{MBP_1} = \frac{4\mu m}{0.36\mu m}$ & $\therefore I_{MBP_2} = 2\mu A$ if the current mirror ratio is 1:1

To size M_{Bn2} & M_{Bn3}, they have current = $2\mu A$ flowing through them & also note that $V_{ds_{MBn3}} = 1.2V$ which will be different than $V_{ds_{MBn2}}$

contd...

∴ It is better to make them operate in subthreshold such that they have better r_o & thus less variation to V_{ds}

For $I = 2\mu A$, we can make $W_{Bn2} = W_{Bn3} = 10\mu m$ to make $I_{density} = 2\times10^{-7}\ A/\mu m$

$$\therefore \boxed{\left(\frac{W}{L}\right)_{M_{Bn2}} = \left(\frac{W}{L}\right)_{M_{Bn3}} = \frac{10\ \mu m}{0.36\ \mu m}}$$

(f) (10 points) Size the transistors $M_{c1}, M_{c2}, M_{casn1}, M_{casn2}$ and M_{Bn1}, given the bias current requirements of you amplifier.

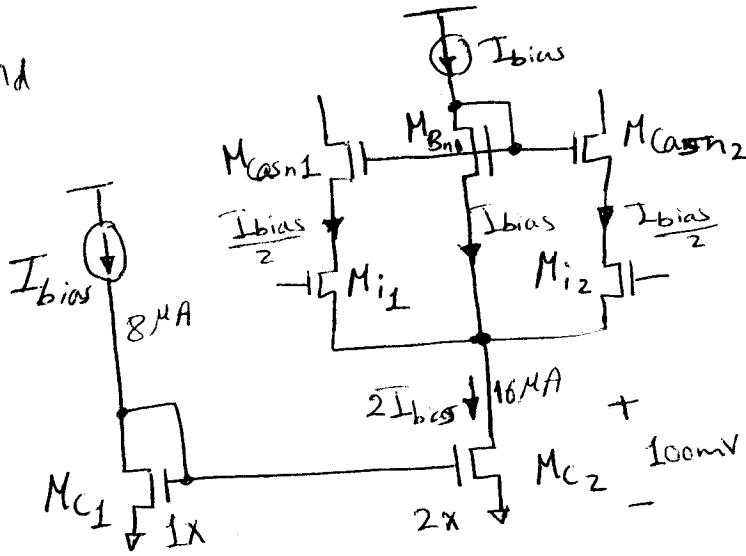
M_{i1}, M_{i2} & M_{c2} are in subthreshold

∴ for optimal biasing we want

$$V_{g_{M_{Bn_1}}} = 0.2 + V_{gs_{casn_2}}$$

$$= 0.1 + V_{gs_{MBn_1}}$$

$\therefore I_{bias} = 8\,\mu A \Rightarrow I_{M_{Bn_1}} = 8\,\mu A$



$I_{casn_{1,2}} = 4\,\mu A$

we can make $\left(\frac{W}{L}\right)_{M_{casn_1}} = \left(\frac{W}{L}\right)_{M_{casn_2}} = \frac{10\,\mu m}{0.36\,\mu m}$ Leading to current density of 4×10^{-7} A/μm & $V_{gs_{casn_{1,2}}} = 420\,mV$

This means $V_{gs_{M_{Bn_1}}} = 520\,mV$ & $I_{M_{Bn_1}} = 8\,\mu A$

For $V_{gs} = 520mV$, the required current density = 3 μA/μm (figs

$$\therefore \left(\frac{W}{L}\right)_{M_{Bn_1}} = \frac{8/3}{0.36} \approx \frac{2.67\,\mu m}{0.36\,\mu m}$$

For NMOS Devices

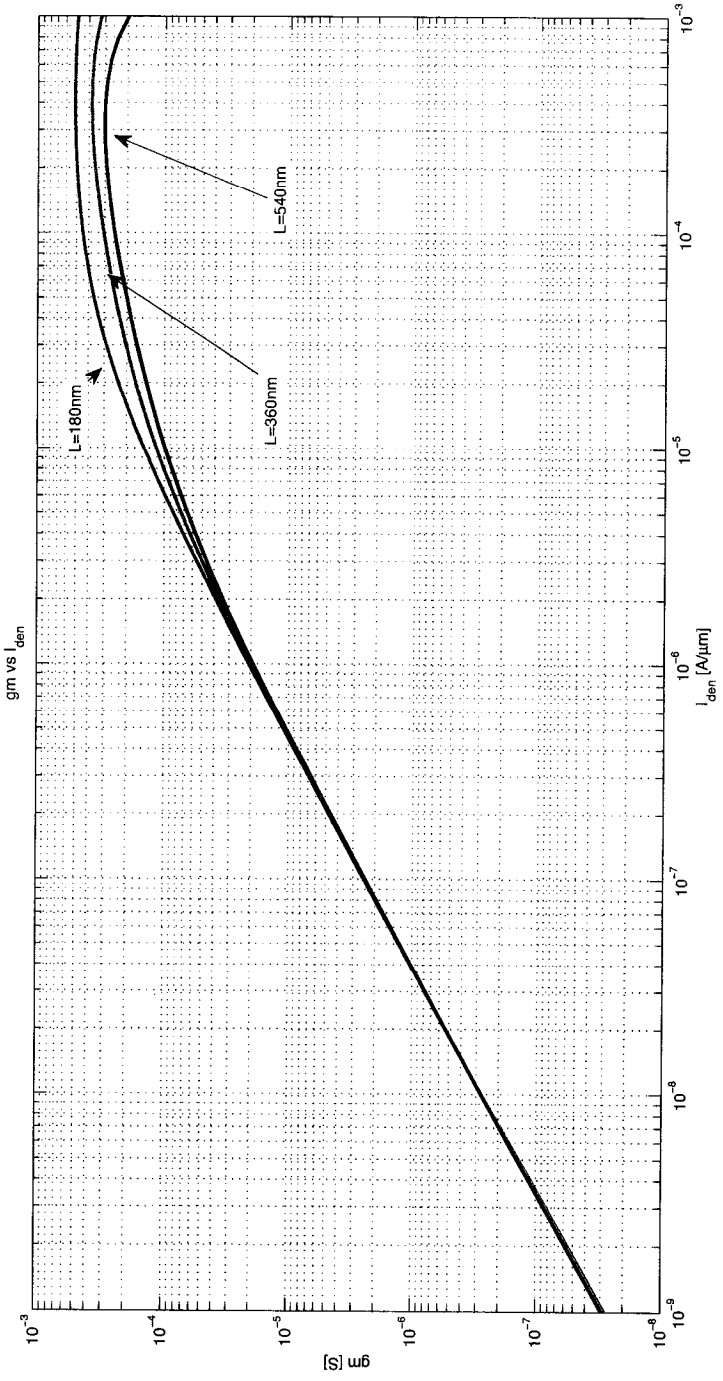


Figure 2: NMOS: g_m vs. $I_{ds}/\mu m$

For PMOS Devices:

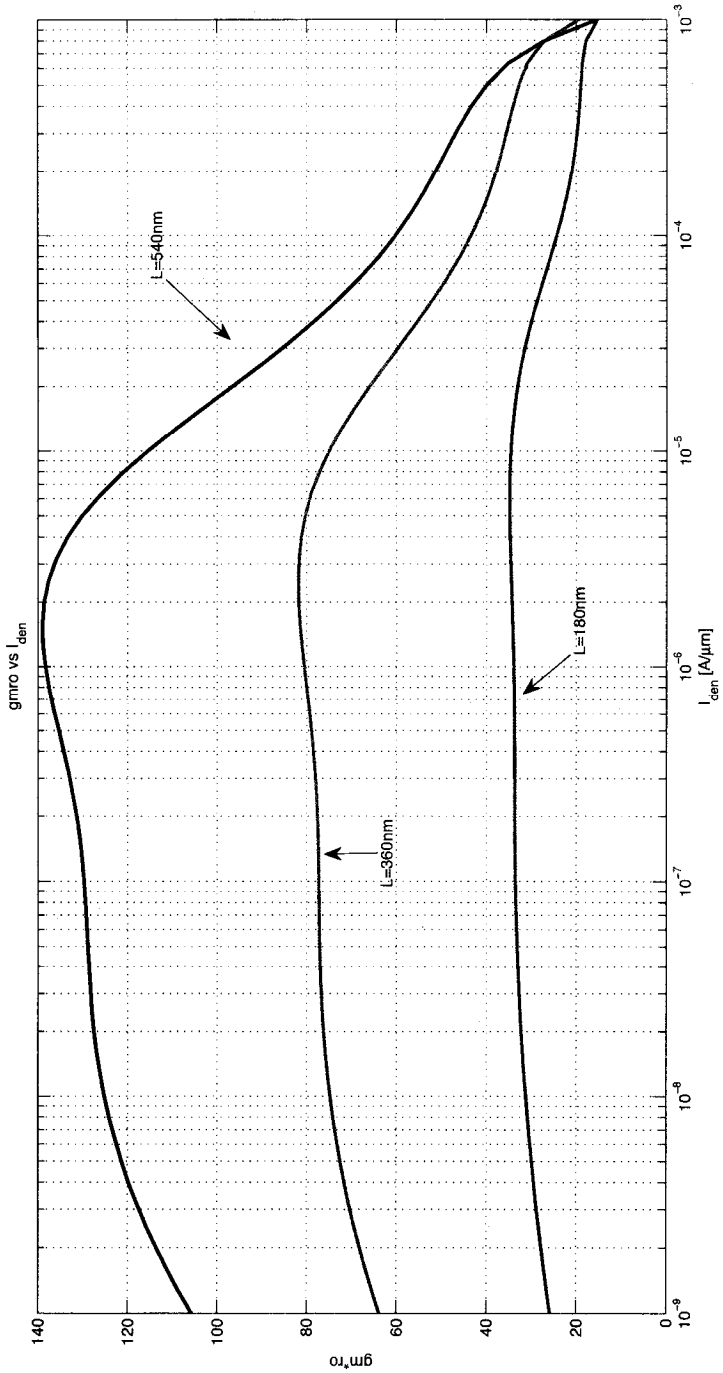


Figure 3: NMOS: $g_m r_o$ vs. $I_{ds}/\mu m$

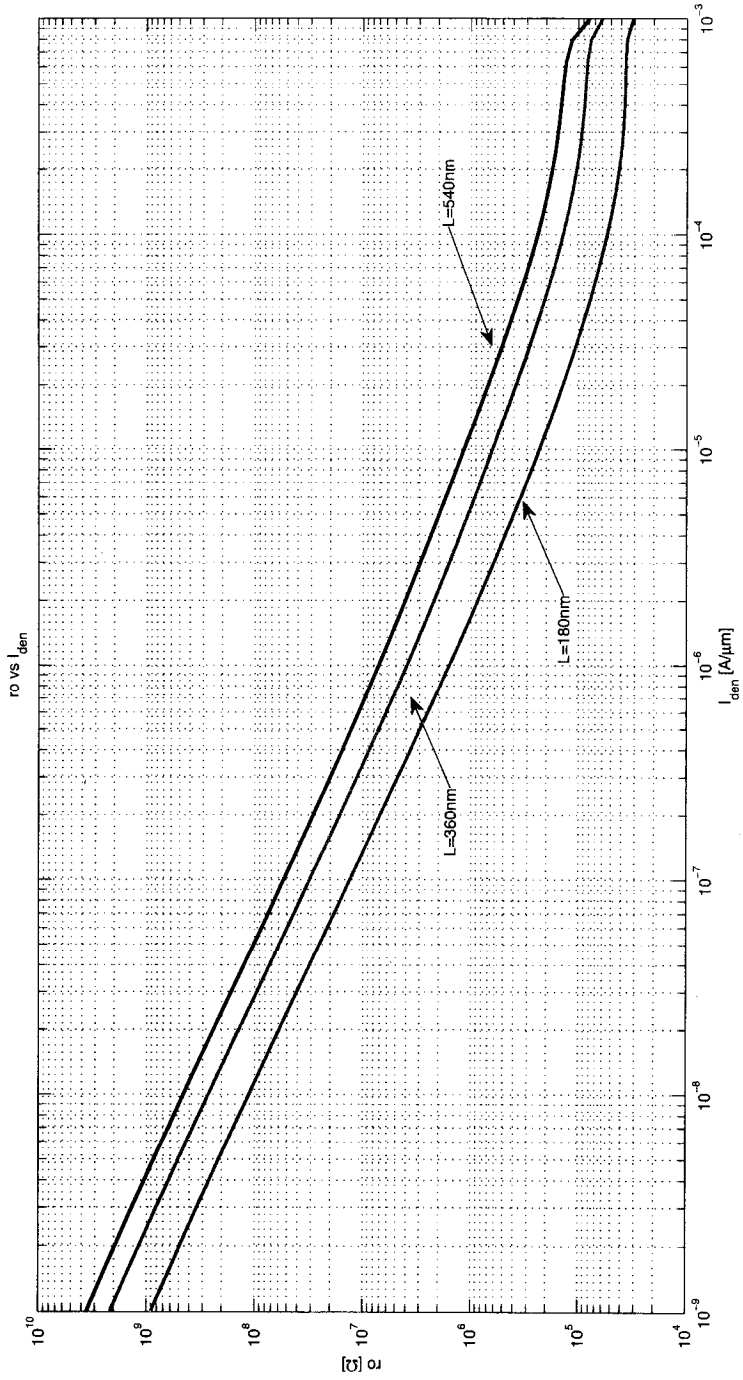


Figure 4: NMOS: r_o vs. $I_{ds}/\mu m$

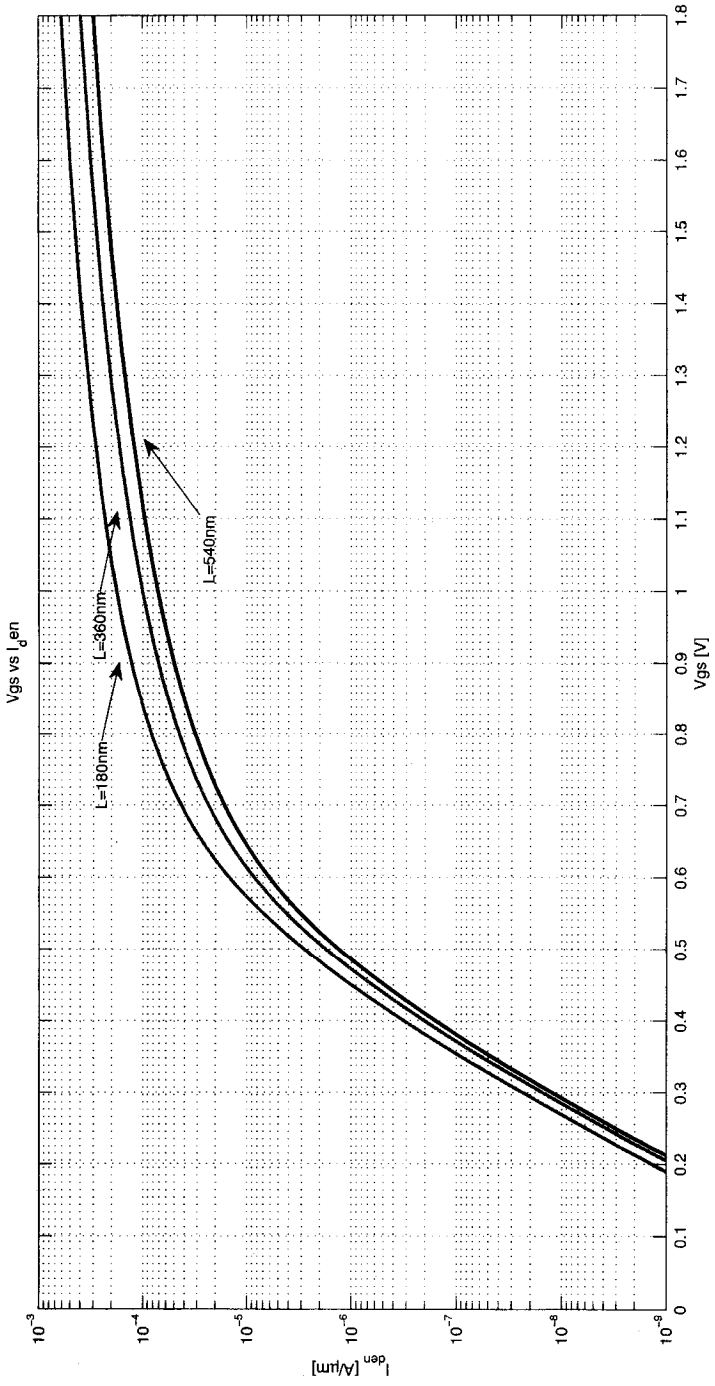


Figure 5: NMOS: $I_{ds}/\mu m$ vs. V_{gs}

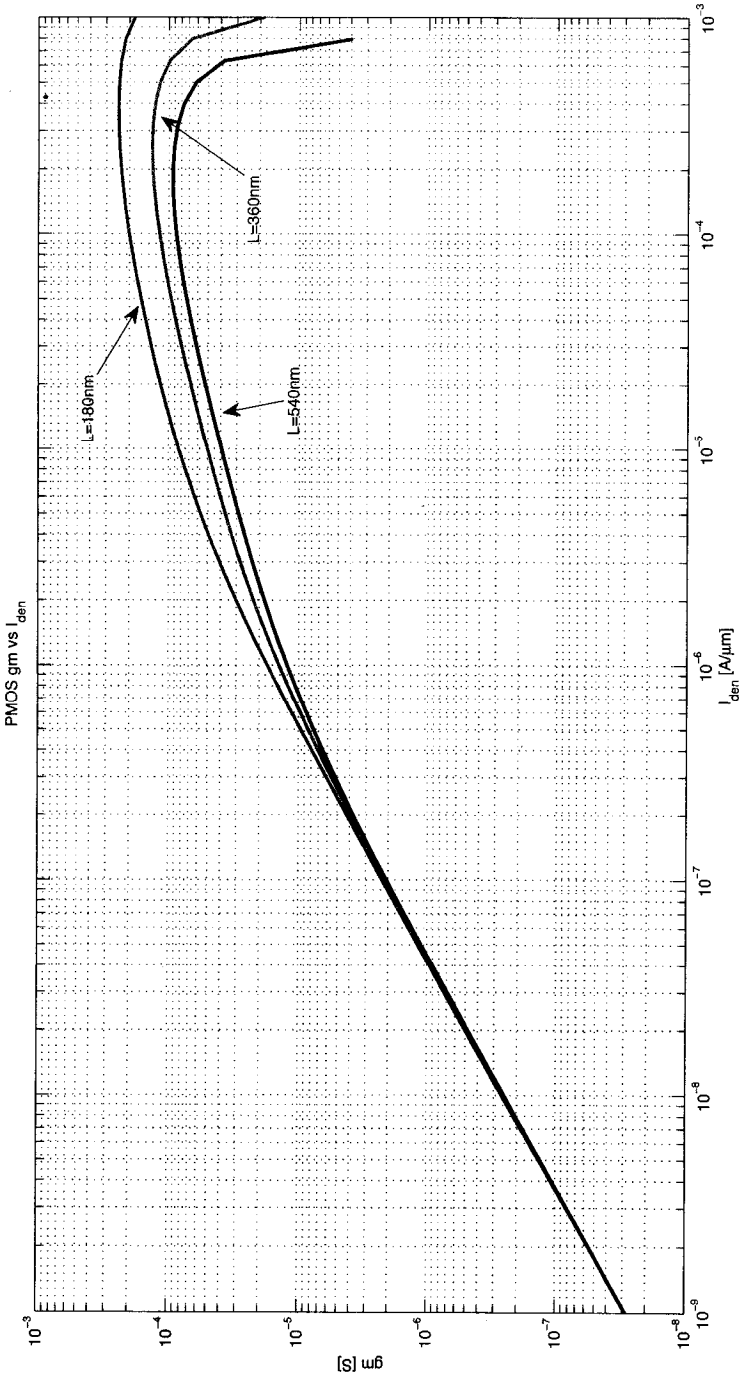


Figure 6: PMOS: g_m vs. $I_{ds}/\mu m$

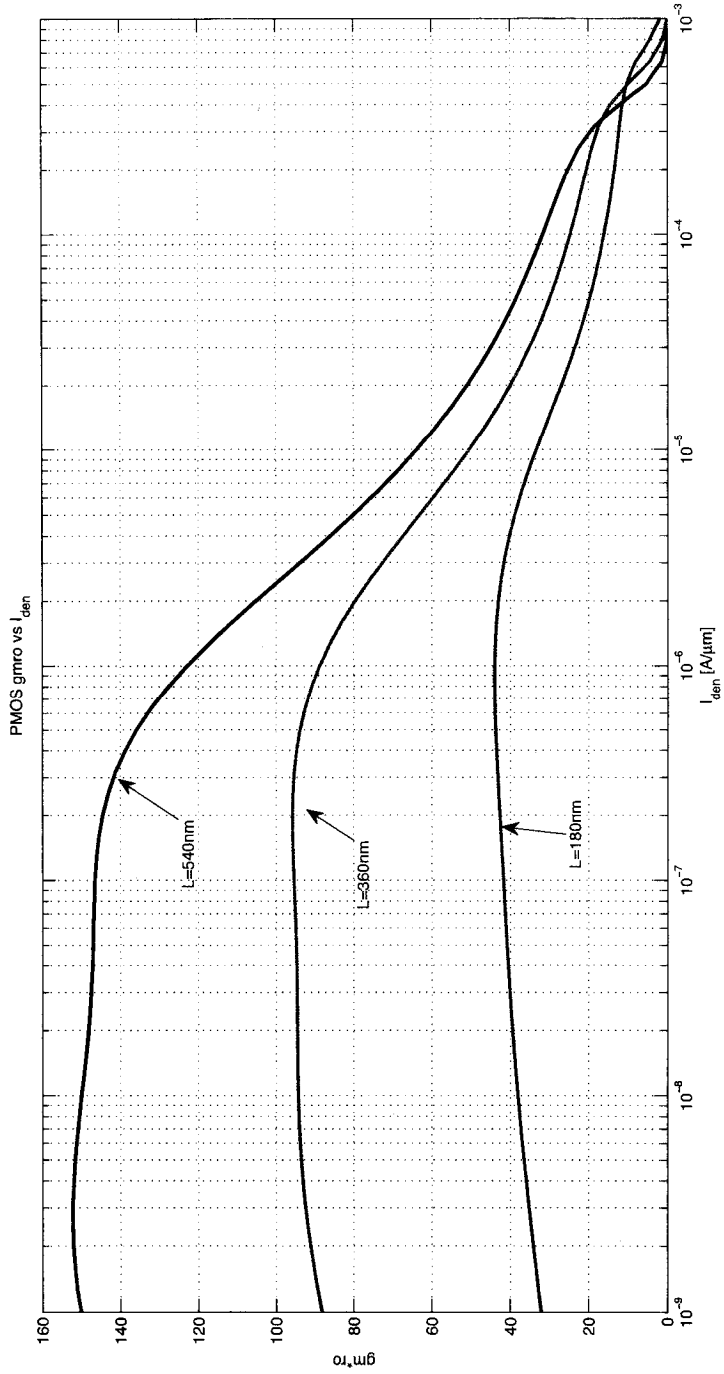


Figure 7: PMOS: $g_m r_o$ vs. $I_{ds}/\mu m$

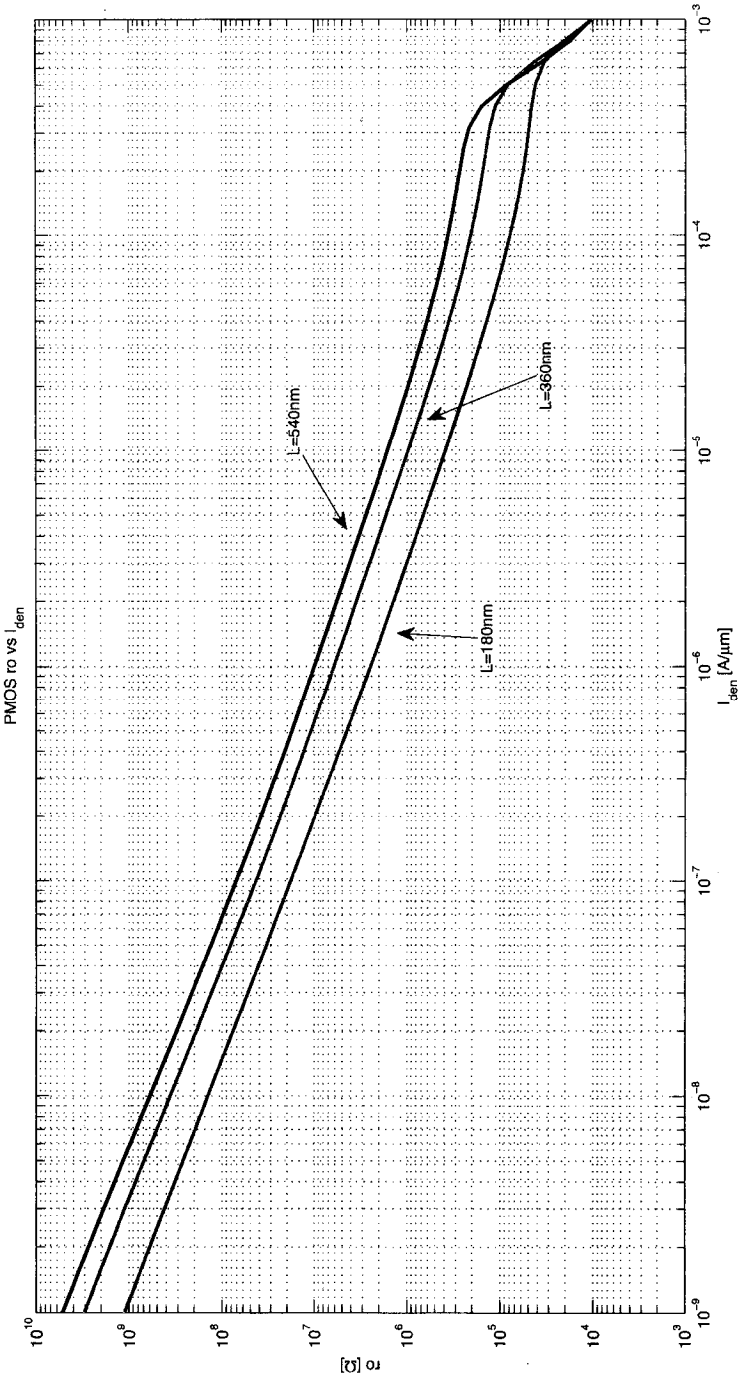


Figure 8: PMOS: r_o vs. $I_{ds}/\mu m$

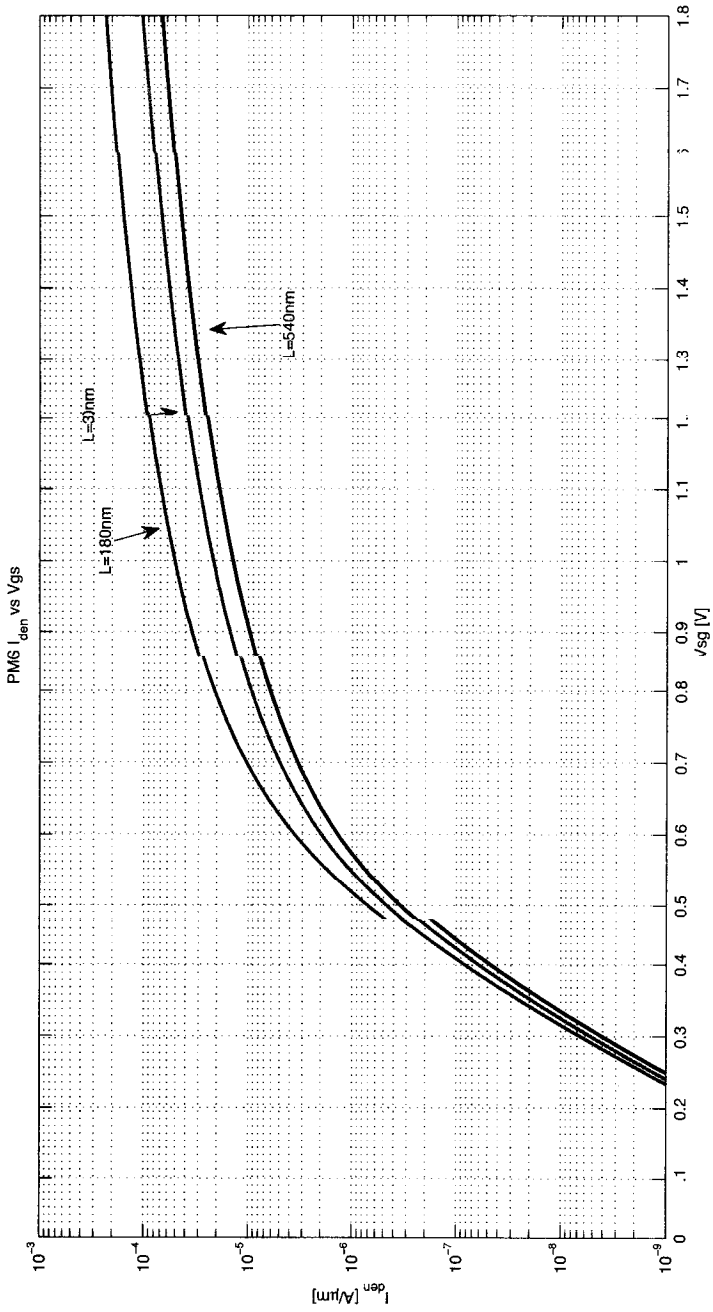


Figure 9: PMOS $I_{ds}/\mu m$ vs. V_{gs}