University of California, Santa Barbara

Department of Electrical & Computer Engineering

ECE 137B

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A high-gan, low-noise fully differential operational transconductance amplifier

Due June 1, 2010

As transistor channel lengths start to decrease, it becomes harder to design analog circuits in theses processes. Nevertheless, designing high performance analog circuits is necessary for high performance A/D, D/A and filters. This design project will highlight some of the obstacles that you might face as an analog designer.The goal of this lab is the design of a high-gain, high-bandwidth low noise operational amplifier. Your prelabs must be done individually and your labs maybe done in teams of 2 if you prefer.

The following constraints must be met.

1. The bias current for your amplifier *must* be derived from a bias generator.
2. The open-loop gain of your amplifier must be $\geq 80dB$
3. The unity gain frequency of your design must be $\geq 10MHz$ for a 1pF load to ground on each output.
4. An input common-mode range of $\geq \pm 150mV$ at a supply voltage of 1.5V
5. The circuit must operate reliably (i.e meet all specs) in a supply range of $1.5V \leq V_{dd} \leq 1.8V$.
6. Power dissipation $\leq 500\mu W$ with a 1.8V power supply including the bias network.
7. A CMFB Circuit is expected for this fully differential design
8. An output swing of 1.5V for a 1.8V supply
9. Worst Case Systematic offset of 1mV
10. Settling time of $\leq 120ns$ to settle with 0.1% of the final value
11. A Common mode rejection ratio (CMRR) $\geq 70dB$ at an input common-mode equal to $\frac{V_{dd}}{2}$
12. A phase-margin of $\geq 50^{\circ}$, additionally you may not use compensation capacitors greater than 5pF.

13. Power-Supply Rejection Ration (PSRR+,PSSR-) $\geq 70dB$ at 100kHz. The PSRR+ refers to the a voltage applied on VDD and PSSR- to an ac votage applied between the negative rail and gnd. For this you will have to tie all the NMOS nodes normally at GND to a pin.

14. A dynamic range $\geq 83dB$ at a supply voltage of 1.8V.
    Dynamic range is given by $DR = \frac{V_{\text{output swing}}}{\text{Input Referred Noise}}$ For a 1.8V supply with an output swing of 1.5V this translates to $\cong 100\mu V$ of input referred noise of in-band noise given by $\left(\sqrt{\frac{V_{noise}^2}{Hz} \times \text{Unity gain bandwidth}}\right)$ when the amplifier is in unity gain configuration driving a 1pF load.

15. The circuit must be minimally sensitive (i.e. meet all specifications) to process variation.

Some additional things you should consider

1. You will be graded on the overall size of your circuit
2. Using widths $> 100\mu m$ or lengths $> 1.8\mu m$ will result in points being deducted.

1 Prelab 1: Due April 23, 2010

The first step in any analog design is to characterize the design parameters so that you can perfrom hand calculation of your intended design. In modern processes there are many second-order effects and instead of using simplified MOS equations design curves are often preferred. For example, instead of using a square law equation that is only approximately valid, a transconductance/unit width(g_m/W) curve (where W is in μm) for various current densities($A/\mu m$) is often preferred. An example curve is given in figure 1

From this curve, one can determine the g_m of the device for a given current density.

1. In cadence, design a simulation so that you can plot the gm vs ids curve for the NMOS and PMOS device in your process. You should also plot the currents for various lengths as in the figure 1. You can use the parametric sweep function in analog artist to aid you in this task. Export your results to MATLAB as a CSV file so that you can determine the equation that best fits the curve for each length. You might have noticed in figure 1 that the curve is linear in the beginning and starts to compress toward the end. The two regions correspond to the subthreshold or weak-inversion and strong inversion regions of the transistor. You may split the curve

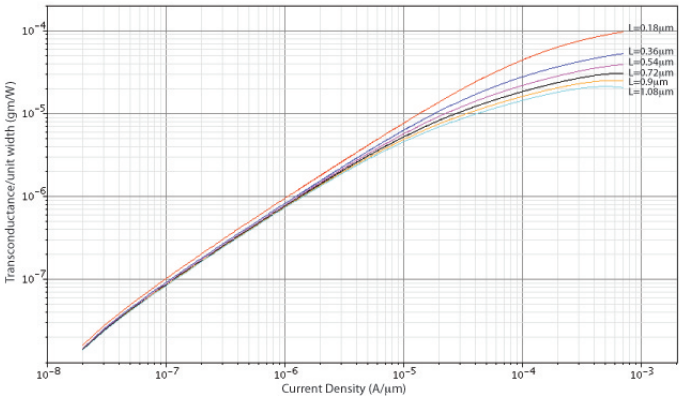

Figure 1: Example gm vs Ids curve for various lengths for a NMOS transistor in 0.18um process

into multiple parts so that you get better fits. What are the equations for g_m in the two regions? Does it agree with what you know about the transistor?

2. Devise a simulation so that you can plot r_o/W of the device for various current densities and also for various lengths.

3. Devise a simulation to calculate the device capacitance of both the PMOS and NMOS per unit width for the various lengths as in the earlier case.

4. Given a capacitive load of 1pF , design an NMOS common-source amplifier with an ideal current source load that has a bandwidth of 10MHz and a gain of 20. Show your calculations that you used to determine the length and width of your NMOS amplifier. Also create a symbol for your amplifier.

5. Now cascade the two amplifiers in series and then load it with a 1pF load, determine the gain and bandwidth of your amplifier. Hand-calculate the poles of the system from your knowledge of the transistor parameters. Do you expect the amplifier to be stable? If so why and if not why not?

6. Export the data into MATLAB and using the tutorial convert it into an lti-model. Where are the poles of your amplifier? Do these results agree?

7. Since you have to design an amplifier with 80dB of gain, How would you split the gain in two stages? It is advisable to have a high-gain first stage and low-gain second stage (also your second stage cannot have a cascode due to the swing requirement which further limits its gain). One way to pick the gain is to get the maximum possible gain from a common source which will be your second stage and then allocate the rest to your first stage. What is the current you will use for the common source, noting

that you need a r_o so that the bandwidth of the common-source stage driving a 1pF load is at least 10MHz?

2 Lab 1: Due April 30, 2010

In this lab you will design a supply-independent current source that can be used in the design of your op-amp. The current bias network must meet the following criteria.

1. No resistor value greater than 10K may be used.
2. The bias network must have a PSRR better than 60dB in the bandwidth range of 10KHz.
3. The circuit must be minimally sensitive ($\leq$ 1% current variation) to process variation.
4. The circuit must operate reliably in a supply range of $1.5V \leq V_{dd} \leq 1.8V$.
5. Power dissipation $\leq 50\mu W$ with a 1.5V power supply
6. The bias network must contain a start-up network
7. The current density matching in all branches of your circuit must be better than 1%

Using the parameters above you will design a current bias network. A few points to note:

1. The power dissipation specification can be translated to a branch current specification by dividing it by the power supply.
2. To ensure that the bandwidth specifications are met you must be able to design your common-source amplifier using this current source. This does not mean that the current bias network must supply this value but that the current can be obtained by multiplying the bias network current value by an integer.
3. High accuracy in current densities translates to a high output impedance specification for current sources/current mirrors.
4. High PSRR translates to having a high loop gain in the feedback loop of your current bias network.

Turn in the following

1. The topology of your current bias network with the sizes of all devices, including your calculations and how you arrived at those device sizes.
2. A plot of the currents in your bias network, showing the matching accuracy as a function of V_{dd}
3. A bode plot of the gain of the current bias network w.r.t the power supply, showing a -60dB gain in the 10kHz bandwidth.
4. The total power consumed by your network (power supply current $\times$ power supply)

3 Prelab 2: Due May 7, 2010

Now that we have the current bias network the next task is to design the first-stage of the op-amp.

1. Using the gain allocation design a differential amplifier that meets this gain. Note this is a fully differential design.
2. one of the things you should keep in mind is that in a DC coupled design the quiescent operating point of your differential amplifier must be such that it can effectively bias your second stage. If your common source stage is a NMOS device then the output of your amplifier will have to be approximately around NMOS bias voltage form your current source.
3. Calculate the input referred noise of this amplifier (both 1/f and thermal (or shot depending on your region of operation) noise
4. Given the size of your common source stage and knowledge of device capacitances and output resistance of your amplifier, calculate the pole of your amplifier.

4 Lab 2: Due May 14, 2010

In this lab you will implement the first stage of your op-amp

1. Plot the ***DC*** transfer curve of your opamp
2. Plot the AC transfer curve of your op-amp, do the poles lie where you predicted them to be?
3. Plot the noise power spectral density of your amplifier, how does this compare to your theoretical calculation.

5 Prelab 3: Due May 21

In this prelab you will hand calculate the design of your second stage and also design your common-mode feedback loop.

1. Given the gain allocation, the current, the bandwidth and the swing requirements, design an amplifier that will serve as your second stage.
2. Given your entire amplifier topology design a CMFB such that the output is at mid-rail.

6 Lab 3: Due May 30

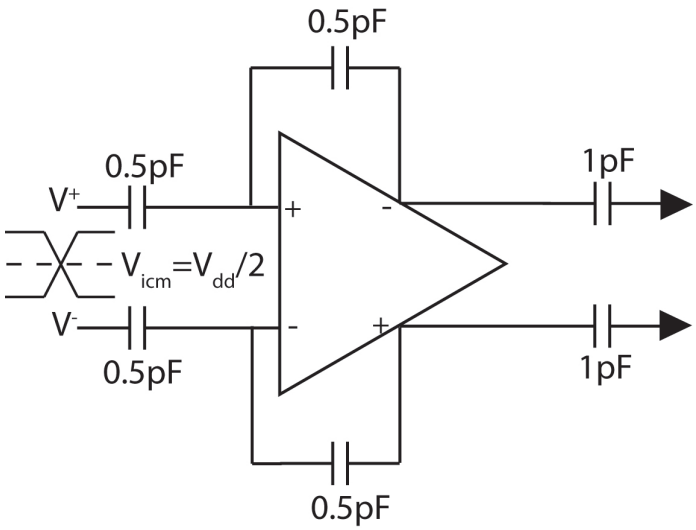

Figure 2: Configuration for testing step response

1. Design your second stage according to your prior calculations for bandwidth and swing with a load of 1pF
2. Plot the DC and AC response of your amplifier, Does this agree with your hand calculations
3. DC couple both your stages and plot the DC and AC responses. Do they agree with what you would expect from theory?
4. Export your AC response into matlab and convert it into an LTI model. In matlab compensate your amplifier by introducing the appropriate poles and zeroes. Plot the response of your theoretically compensated amplifier

5. Using your matlab design as a guide compensate your design and plot the AC response of your compensated design
6. Plot the step response of your amplifier for a 100mV step for both rising and falling steps with your op-amp in unity gain configuration, see figure 2.
7. Plot the AC response of your common-mode gain
8. Plot the AC response of your power-supply gain both from V_{dd} and V_{ss}
9. Plot the noise PSD of your op-amp
10. Turn in a table with the expected specifications and values of your design.