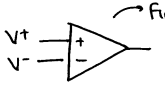
Notes 04/19/2010

Last Class → MOS Capacitance

OP-AMP DESIGN



→ First stage is a differential pair

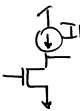
Op-amp datasheets include:
- open loop gain
- bandwidth
- phase margin

Open loop gains are anywhere from 80dB-120dB

- Think about what kind of op-amp you want to design.

① MOS Amps → capacitive loads, input is practically infinite impedance
② BJT Amps → resistive loads

Example: 80dB gain ① Can this be accomplished in one stage?



$gain = -g_m r_o$ $\quad g_m = \frac{2I_d}{V_{ov}} = \sqrt{2I_d k}$

$V_{ov} = V_{gs} - V_t$ $\quad I_d = \frac{k}{2} V_{ov}^2$

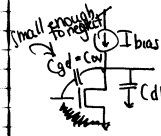
$V_{ov} = \sqrt{\frac{2I_d}{k}}$ $\quad k = \mu_n C_{ox} \frac{W}{L}$

$r_o = \frac{1}{\lambda I_d}$ $\quad gain = -\frac{\sqrt{2I_d k}}{\lambda I_d} \rightarrow gain \propto \frac{1}{\sqrt{I_d}}$

as $I_d \uparrow$, gain ↓ – to get maximum gain (small bias current)

However, bandwidth is effected

- only ignore C_{gd} if device is small and frequency of operation is low

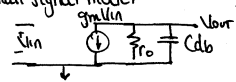


- one pole, $\tau = r_o C_{db}$

$H(s) = \frac{g_m r_o}{1 + s r_o C_{db}}$ $\quad \therefore H(s) = \frac{A_o}{1 + s\tau}$

Load entirely due to C_{db}

Small-signal model



$H(s) = \frac{-g_m r_o}{1 + s r_o C_{gb}}$ gain $\propto \frac{1}{\sqrt{I_d}}$

- Lower I_d, increase gain, lower bandwidth

Typical $V_{ov} \sim 200mV$ $I_d = 100\mu A$

$g_m = \frac{2 \cdot 100\mu A}{200mV} = \underline{1mS}$ to get 80dB: $r_o = \frac{A_o}{g_m} = \frac{10^4}{10^{-3}} = \underline{10M\Omega}$

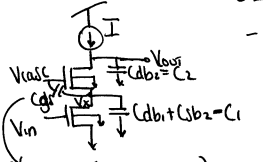
typically λ ranges from $0.1 \rightarrow 0.01$ $\lambda = 0.1$

$r_o = \frac{1}{\lambda I_d} = \underline{100k\Omega}$ → off by factor of 100 to get 80dB

$A_o = \frac{1}{\lambda}\sqrt{\frac{2k}{I}}$ } pick I, λ & k are given → get a set gain for a given process

Other options?

Cascode → increasing output impedance
- add second stage without adding another pole close to original
- second pole is far away

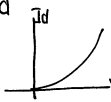


$\frac{2}{3} W L C_{ox}$ (in saturation)

(C_{gs} is not there in low frequency b/c if $V_{bias}\uparrow$ $V_x\uparrow$, eliminating effect of capacitance

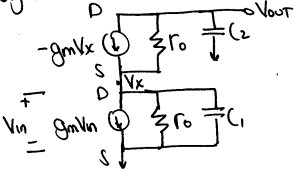
as $V_{in}\uparrow$, transistor wants to increase current but cannot due to fixed I so $V_d \downarrow$ instead

Transistor Curves:

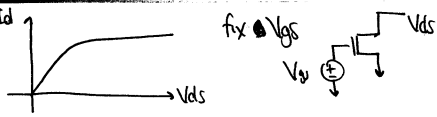


(fix Vds)

Small-signal model:



Remember: r_o has no meaning in DC condition



r_o is necessary for the transistor to satisfy physical constraints, without r_o, gain would be infinite

Back to small-signal cascode:

$$\frac{V_x}{V_{in}} = -g_{m1} r_{o1} \qquad \frac{V_{out}}{V_x} = g_{m2}(r_{o2} \parallel r_{o1})$$

$$\boxed{\frac{V_{out}}{V_{in}} = -g_{m1} g_{m2} r_{o1}(r_{o2} \parallel r_{o1})}$$

Adding caps: C in parallel with device r_o

C_2 will be the dominant pole b/c the impedance is higher at that point

$$\tau_1 = g_{m2} r_{o1} r_{o2} C_2 \qquad \tau_2 = r_{o1} C_1$$

} if same size device $C_1 \approx 2C_2$

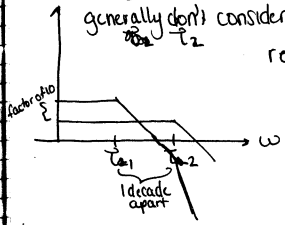
τ_1 bigger by factor of 2 $\quad \tau_1 = \frac{g_{m2} r_{o2}}{2} \tau_2$

~~poles are generally good~~ - in addition, usually drives another cap which make τ_1 even slower, more dominant

Example: gain of 10 → 20dB

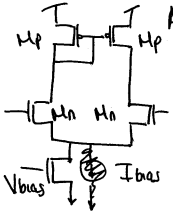
generally don't consider τ_2

resort to 2 stages for 80dB gain



80dB - Two stages (Second stage, highest swing possible)

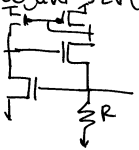
First stage



$A_v = g_{mn}(r_{op} \| r_{on})$

① Pick bias current (using power constraints)

Ex. $100\,\mu W \rightarrow 2V\ (V_{dd}) \Rightarrow I_b = 50\,\mu A$



pick R

$V_t = 0.5V$

$V_{ov} = 200mV$

$R = \frac{0.5 + 0.2}{50\,\mu A}$

$R = \frac{7}{5}(10^4)\,\Omega$

$R \approx 14k\,\Omega$

② Sizing pmos devices (using swing requirements)

Set V_{gs} of pmos to point at which output swings

Notes 04-21-2010

Exam Monday, April 26th (Chapter 1-6 (Razavi)
Review Session Friday

Amplifier Design

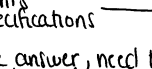
Constraints or Specifications ⟶ Design

- no unique answer, need to consider circuit complexity and application of circuit

Tradeoffs to consider → Power ↑ Bandwidth ↑
- with Vdd fixed → Power ↑, Current ↑, BW ↑
- Charging capacitors faster and the rate of change depends on $\frac{dV}{dt} = \frac{I}{C}$

Precision ↑ Bandwidth ↓

- precision in terms of the amplitude of a follower
  Ex. unity gain amplifier



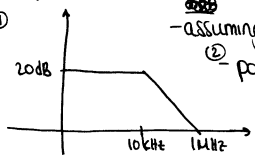
$\epsilon = \frac{1}{A_0}$ Vout can never reach Vin exactly

- to get a smaller error, Ao must be very large

- larger gain implies smaller bandwidth: must charge cap to higher value which takes longer → single pole example

- To achieve both required a second pole (second stage)
  ↳ high gain & BW

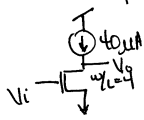
Example: Ao = 100 BW = 100 kHz Power = 100 μW Vdd = 2.5V



- assuming gain is achieved in one stage

② - power → $I = P/Vdd = \frac{100\,\mu W}{2.5V} = 40\,\mu A$

③ Decide on a topology:



Consider transistor parameters (set for a particular device): $\frac{\mu_n C_{ox}}{2} = 25\mu A/V^2$

$V_T = 0.5V \quad \lambda = 0.1$

④ Determine transistor gain

$r_o = \frac{1}{\lambda I_d} \longrightarrow A_v = -g_m r_o \qquad g_m = \frac{2I_d}{V_{ov}} = \sqrt{2I_d k}$

$V_{ov} = \sqrt{\frac{I_d}{k}}$

$A_v = \sqrt{2I_d k} \cdot \frac{1}{\lambda I_d}$

$= \frac{1}{\lambda}\sqrt{\frac{k}{I_d}} = 100$

⑤ Determine size (W/L)

$\frac{1}{0.1}\sqrt{\frac{k}{I_d}} = 100 \rightarrow \sqrt{\frac{k}{I_d}} = 10 \rightarrow \frac{k}{I_d} = 100$

$k = 20\mu A(100) \rightarrow k = 10\mu A(100) \quad k = \frac{\mu_n C_{ox}}{2}(10)$

$2\frac{\mu_n C_{ox}}{2}(10) = 10\mu A(100) \rightarrow 4\mu_n C_{ox}\left(\frac{W}{L}\right) = 10\mu A(100)$

$4(25\mu A/V^2)\left(\frac{W}{L}\right) = 10\mu A(100) \rightarrow \boxed{\left(\frac{W}{L}\right) = 4}$

- Be careful with λ. It is specified for a given length.
If length is 1μm, width is 4μm

$\boxed{L = 1\mu m, \; W = 4\mu m}$

⑥ Determine V_{gs}

Process = 0.5μm (λ specified for 1μm)

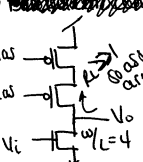
$V_{ov} = \sqrt{\frac{I_d}{k}} = \sqrt{\frac{1}{100}} = 0.1$

$V_{ov} = V_{gs} - V_T = 100mV$ (↳ 500mV)

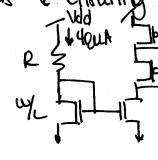
$\boxed{V_{gs} = 600mV}$

Note: Processes are typically design for fastest digital systems, as an analog designer, length must be increased

⑦ [redacted]



⑧ Ensuring 40μA of current



- you can choose this W/L to be 4
then you can calculate R from required current

Ok →

- In general, want smaller values of R b/c they are hard to manufacture
  On the order of 10-100kΩ, so pick R = 25kΩ for example

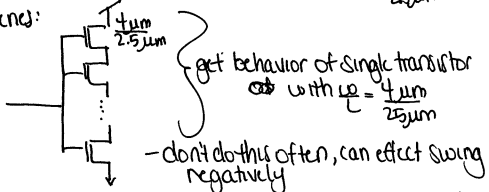
  $I_R = V = 25k\Omega(40\mu A) = 1V$

  $(2.5-1) = 1.5V = V_{gs}$ instead → $V_{ov} = 1.0V$

  $\frac{W}{L} = \frac{2I_d}{\mu_n C_{ox} V_{ov}^2} = \frac{40\mu A}{250\mu A/V^2 (1V)} = 4/25$

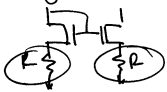
Problems with L >> W, may want to readjust resistor value to get better ratio

- If you want to make a transistor with these specs: use $\frac{4\mu m}{25\mu m}$
could place 10 in series:



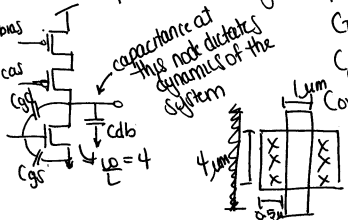
- don't do this often, can effect swing negatively

Another option is to refer V_{gs} to another voltage instead of ground but you bring problems with matching



- Pick pmos size as W/L = 4 b/c we are not considering swing yet

⑧ Considering 3-dB point
where is the pole → Identify all caps



$C_{DB} = 2ff + 5ff = 7ff$

$C_{GD} = C_{ov}(W) = 0.8ff$

$C_{out} \equiv 4ff + 0.8ff + 7.8ff$ $\quad r_o = \frac{1}{\lambda I_d} = \frac{1}{0.1(40\mu A)} \approx 250k\Omega$

$\omega_o = \frac{1}{r_o C_{out}} = \frac{1}{7.8ff(250k\Omega)} \approx 512.8 Mrad/s$

$f_o = \frac{512.8 Mrad/s}{2\pi} \approx 81.6MHz$ → frequency is off from design specs.

① Didn't take capacitance of pmos into effect

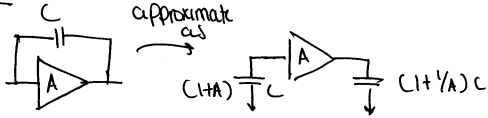
② Cov shows up as two capacitors

as freq ↑ more signal is shorted through C_{gd} which eliminates your 180° phase shift

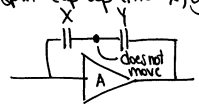
-gives a RHP zero because of 180° rotation

Instead of $\frac{s+a}{s+b}$ you get $\frac{s-a}{s+b}$ (kills phase)

Miller Effect



Proof: split cap up into X, Y



Superposition

$= \frac{V_{out}x}{X+Y} + \frac{V_{out}y}{X+Y} = 0$

$\frac{V_{out}x}{X+Y} + \frac{AV_{in}y}{X+Y} = 0$

$V_{in}x = -AV_{in}y$

$x = -Ay$

$V_{out} = AV_{in}$

$\frac{Y}{X+Y} = C$

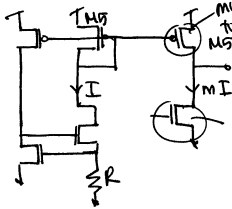
$y = \frac{C}{A}(A+1)$

$X = (A+1)C$

Notes 04/08/2010

Differential Amplifier Design

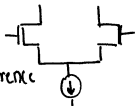
Last Time:



Differential

- Robust to noise due to high CMRR

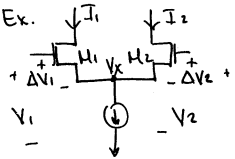
Benefits:



- Allows you to take a difference voltage

(Subtracts two voltages referenced to ground through a common node point)

Ex.



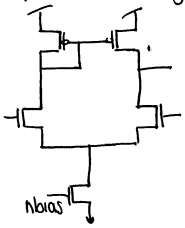
$V_1 - \Delta V_1 + \Delta V_2 - V_2 = 0$

Make $\mu_1 = \mu_2$ (carry the same current and have the same parameters)
$\therefore V_{ov}$ for each is equal

So $\Delta V_1 = \Delta V_2 \rightarrow V_1 - V_2 = 0$

- In addition, currents are proportional to the voltage subtraction (as long as inputs are differential)
  i.e. $\Delta V_1 \uparrow$ the same as $\Delta V_2 \downarrow$ in order to treat V_x as a small signal ground "virtual ground"

- Simplest version - single-ended



$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_{bias}}$

- two parameters to control g_m
  (1) W/L (2) I_{bias}

- In CS design, the above parameters are not independent

$V_{gs} = V_{in}$ $V_{ov} = V_{in} - V_T$

$g_m = \frac{2 I_d}{V_{in} - V_T}$ But, $I_d = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_T)^2$

- choosing I_d implies W/L

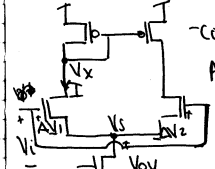
Difference w/ diff. pair: the source is not pinned to ground

- Independently control V_{GS} & I_D, choose I_D for a particular Fosc and W/L for desired g_m.
- Gives an extra degree of freedom: input voltage decoupled from V_{GS}

What do you design for? (Specific actions)
① Gain
② Bandwidth
③ Power
⑥ Swing
} explicitly specified

④ Input Common Mode
⑤ Output Quiescent Voltage
} implicitly specified

- Input Common Mode range (range of bias voltages possible for input) so that the amp still works



- Connect inputs to put in common mode

Apply $V_i = V_{dd}$, will it work?

V_x stays constant b/c I remains the same due to common mode operation

- To prove amp is operational → must prove all transistors are in saturation
  i.e. $V_{DS} > V_{ov} > V_{GS} - V_T$

Does V_{ov} change? → No, I remains the same, V_S increases with increase on input instead

$\vec{I} = \sigma \vec{E}$ (current depends on electric field)

- In transistor: ~~higher voltage acts as drain~~, lower voltage acts as source, higher voltage will act as drain

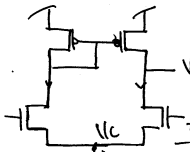
- How low can you go? → ensure bottom transistor remains in saturation V_S cannot go lower than V_{ov} of bottom transistor

then V_i must include V_{ov} of input nmos

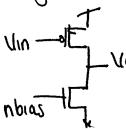
$V_i - \Delta V_i - \Delta V_2 = 0$ $\quad V_i = \Delta V_i + \Delta V_2$ $\quad V_i = V_{GSi} + V_{ov}$

$V_{GSi} = V_T + V_{ov}$

Output Quiescent Voltage

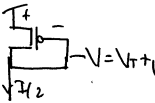


- want Vout to sit at $V_{DD}/2$ (if supply is $V_{DD} \to 0$) or 0 for (supply $\pm V_{DD}$)
- under the assumption that $V_{in,cm} = @ V_{dd}/2$ (for $V_{dd} \to 0$) or @ 0 (for $\pm V_{dd}$)
- Enforcing $V_{dd}/2$ at output by sizing



where will Vout end up?

- If currents are the same:



$V_{dd} - (V_T + \sqrt{I / \mu_p C_{ox} \cdot W/L}) = V_{dd}/2$

$\mu_p \frac{C_{ox}}{2} \frac{W}{L} (V_{gs} - |V_{tp}|)^2 = I/2$ - pick W/L to get $V_{dd}/2$

- In reality, Vout will settle close to design spec b/c current does change slightly.

Swing (how high can Vout go b/f devices go out of saturation)

- worry about pmos on the up swing ($V_{dd} - V_{ov(pmos)}$) - upper limit
- worry about nmos on the down swing & [illegible]

$V_{out} - V_{ovi} - V_c = 0 \quad V_c = V_i - (V_T + V_{ovi})$

$V_{out} - V_{ovi} - V_i + V_T + V_{ovi} = 0 \rightarrow V_{out} = (V_i - V_T)$ - lower limit

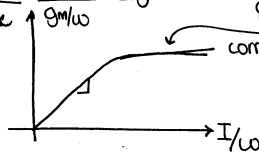
- Physically cannot have Vout go lower than Vc because the source & drain will flip and current will go the other way

Power → bias current

Gain → fix I → get r_o from g_m (using graphs or eqns)

Notes 05-05-10

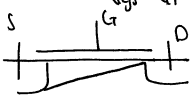
Revisit Device Physics



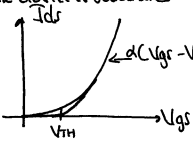
$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$ → equation is valid in saturation and that the transistor is in strong inversion

corresponds to

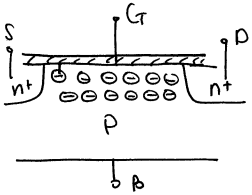
$V_{gs} = V_T$



Assume device is saturated



- Real devices cannot switch abruptly



- Electrons can still diffuse from source to drain even when transistor is supposedly "off"
- Behaves like a bjt when $V_{gs} < V_T$
- Current has an exponential relationship in this regime

Derivation:

Start with diffusion current, relationship between current density and diffusion - Fick's First Law:

$\vec{\Phi}$ = $-D \frac{dC}{dx}$ → Flux $\qquad \vec{J} = qD_n \frac{dn(x)}{dx}$

Boltzmann distribution: relates potential energy to concentration

$n = n_0 \exp\left[\frac{qE}{KT}\right]$ - At any point on channel, potential called surface potential ϕ_s.

$= n_0 \exp\left[\frac{q\phi_s}{KT}\right] = \frac{n_i^2}{N_A} \exp\left[\frac{q\phi_s}{KT}\right]$

$n_0 = \frac{n_i^2}{N_A}$ } $n_0 p_0 = n_i^2$ in thermal equilibrium

$p_0 \cong N_A$

$n = \frac{n_i^2}{N_A} \exp\left[\frac{q\phi}{kT}\right]$ Total concentration:

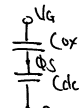
$= \frac{n_i^2}{N_A} \int_0^\infty \exp\left[\frac{q\phi}{kT}\right] dx$ (assume thickness = t of electron $\phi = \phi_s$ in that region)

$= \frac{n_i^2}{N_A} t \exp\left[\frac{q\phi_s}{kT}\right] = Q/\omega$

$J = qD_n \frac{dn}{dx}$ $\frac{I}{\omega t} = qD_n \frac{dn}{dx}$

$I = q\omega t D_n \frac{dn}{dx}$

$\frac{d\phi_s}{dV_{gb}} = \frac{C_{ox}}{C_{ox}+C_{dep}}$



$\int d\phi_s = \frac{C_{ox}}{C_{ox}+C_{dep}} dV_{gb}$

$n = 1 + \frac{C_{dep}}{C_{ox}}$ when $V_{gs} = V_{TH}$, $\phi_s = 2\phi_f$

$\phi_s = \frac{C_{ox}}{C_{ox}+C_{dep}} V_{gb} + k = \frac{V_{gb}}{n} + k$ $\phi_s = \frac{(V_{gb}-V_T)}{n} + 2\phi_f$

$\therefore \phi_s = \frac{(V_{gb}-V_T)}{n} + 2\phi_f$

$I = q\omega t D_n \left[n_o(s) - n(d)\right]$ $n_o(s) = \frac{n_i^2}{N_A} \exp\left[\cdots\right]$

assume source tied to body $= \frac{n_i^2}{N_A} \exp\left[\frac{q(V_{gs}-V_T)}{nkT}\right] \exp\left[\frac{q\phi_s}{kT}\right]$

$n_o(s) = \frac{n_i^2}{N_A} \exp\left[\frac{q(V_{gs}-V_T)}{nkT}\right] \exp\left[\frac{q2\phi_f}{kT}\right]$

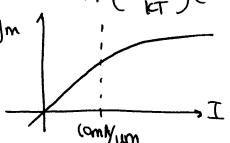
$n(d) = \frac{n_i^2}{N_A} \exp\left[\frac{q(V_{gd}-V_T)}{kT}\right] \exp\left[\frac{q2\phi_f}{kT}\right]$

$I = \boxed{q\omega t D_n \left\{\frac{n_i^2}{N_A} \exp\left[\frac{q2\phi_f}{kT}\right]\right\}} \exp\left[\frac{q(V_{gs}-V_T)}{nkT}\right] \left\{\left(1-\exp^{\frac{-qV_{ds}}{kT}}\right)\right\}$

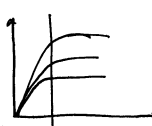
I_o ← pull into I_o

$I = I_o \exp\left(\frac{qV_{gs}}{nkT}\right)\left(1-\exp\left(\frac{-qV_{ds}}{kT}\right)\right)$ → Subthreshold MOSFET

BJT: $I = I_o \exp\left(\frac{qV_{be}}{kT}\right)\left(1-\exp\left(\frac{-qV_{ce}}{kT}\right)\right)$



if $V_{ds} \gg kT/q$ → $\exp\left(\frac{-qV_{ds}}{kT}\right)$ drops out



$I = I_0 \exp\frac{qV_{gs}}{kT}$

In subthreshold:

Saturation eqn: $I = I_0 \exp\left(\frac{qV_{gs}}{kT}\right)$

$\frac{\partial I}{\partial V_{gs}} = \frac{I_0 q}{nkT}\exp\left(\frac{qV_{gs}}{kT}\right) = \frac{I}{n\left(\frac{kT}{q}\right)}$

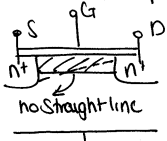
→ $\frac{2kT}{q}$ – device saturated

$g_m = \frac{I}{n V_{TH}}$

– as channels get shorter, subthreshold current increases (leakage current even when device is supposed to be off)

- For analog design → more headroom (no more $V_{gs}-V_t$ limitation)
now it is $\frac{2kT}{q}$
- In addition, gain is constant w/ current.

Body effect (occurs when source and body are not tied to the same potential)



$V_{TH} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$ (Qdep/Cox)

V_{GB} V_{FB} ϕ_S ϕ_S

$\phi_S = 2\phi_F$ when $V_{SB} \to V_t$

need to refer to source

~~$V_{GB} \to V_{GS}$~~ ~~$V_{GB} \to V_{SB}$~~ ~~$V_{GB} \to V_{SB}$~~

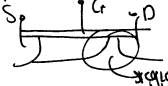
$V_{FB} \to V_{GS} - V_{SB}$

$V_{GB} + V_{SB} = V_{FB} + V_{SB} + \phi_S + \frac{Q_{dep}}{C_{ox}}$

$V_t = \boxed{V_{FB} + 2\phi_F} + V_{SB} + \gamma\sqrt{2\phi_F + V_{SB}} + \boxed{\gamma\sqrt{2\phi_F}} - \gamma\sqrt{2\phi_F}$

$V_t = \underbrace{V_{TH0}}_{V_{FB}+2\phi_F} + V_{SB} + \gamma\sqrt{2\phi_F + V_{SB}} + \gamma\sqrt{2\phi_F}$ — new threshold due to body effect

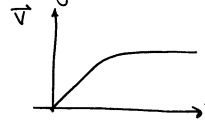
- If two transistors are stacked:



V_t is different

Velocity Saturation

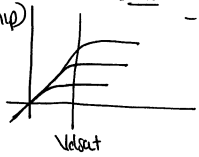
$\vec{v} = \mu\vec{E}$ → when field is small this is valid, relationship is linear



- As field increases, collision time changes so velocity saturates
- Results in premature saturation at V_{dsat}

$I \propto V_{dsat}$ (linear relationship)

- Similar to degenerative effect of source resistor



- velocity cannot increase any further

Notes 05-10-10

Last Class: Device Physics - short-channel effects (subthreshold)

This Class: How to perform graphical design (short-channel devices)

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 \left[\frac{1}{1 + \frac{V_{gs} - V_T}{E_{sat} L}}\right]$$

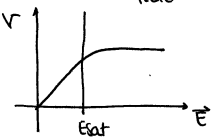
E_{sat} → saturating electric field

If $V_{gs} - V_T \gg 1$ → linear

If $V_{gs} - V_T \ll 1$ → Square-law device

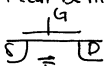
$\vec{v} = \mu \vec{E}$ only valid in drift physics

$v(E) = \frac{\mu \vec{E}}{1 + E/E_{sat}}$



negative feedback

So it can be modeled as source degeneration



also applying field

Mobility: μ_{eff}

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_{scatter}}$$

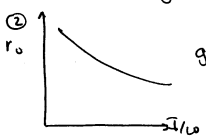
- mobility must be adjusted due to surface scattering

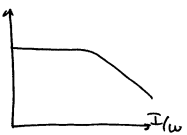
- Lesson: formula helps understanding but is inaccurate for calculations

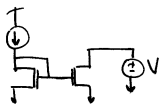
- How do you design around this problem?

Graphical design: g_m vs. current density ① / r_o vs. current density ② / $g_m r_o$ vs. current density ③

device must be in saturation

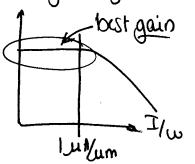






Example: 10μA per branch (single-stage)

Gain: $g_m r_o$



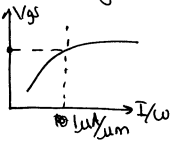
Speed → smaller device to carry same current

- pick a number as high as you can for required current

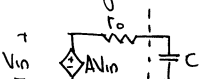
- To ensure device operates at chosen point you must enforce the voltage condition as well
  - V_{gs} must be same as necessary for the g_m vs I/w

$w = 10\mu m$ to get $10\mu A$ $\quad L = 0.18\mu m$

Plot V_{gs} vs I/w →



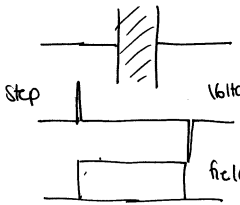
- Calculating bandwidth (pole determined by single time constant)



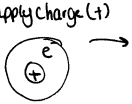
- Should lie at $\frac{1}{r_o C}$ ← loss of ½ gain at

- as frequency increases, you lose energy through the capacitor and gain drops!

Capacitance: two plates with an insulator



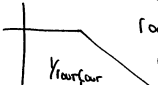
Insulator: apply charge (+)



no longer spherical

- takes a finite time for field to ripple through so it slows down

- potentials must have caps associated with them

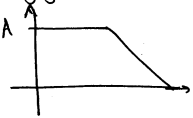


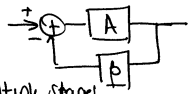
$r_{out} = r_{op} \| r_{on}$

$C_{out} = C_{db_n} + C_{db_p}$

- Still must take load cap into account as well

- Datasheets usually refer to unity gain bandwidth
- unity gain and 3-db gain is related by open-loop gain
  - to increase gain, you decrease bandwidth
  - move up and down curve using feedback





$\frac{A}{1+A\beta}$

-typically 30-50dB in single device

80dB → 10^4 gain through multiple stages

Ex. 2 stages (not unconditionally stable)

$= (250)(40)$ (poles are at different locations b/c gains are different)

① ②

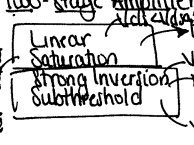
Higher gain → higher r_o → lower pole location (for same cap)

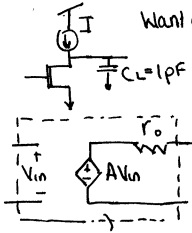
-With pole locations at same point in feedback you will automatically get ringing. due to 180° phase shift

Notes 05-12-2010

Last Class: Graphical Design

Two-Stage Amplifier Design





Want a bandwidth = 1MHz.
How do you pick current I?

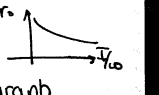
pole = $\frac{1}{r_o(C_L + C_{db} + C_{current\ source})}$

C_{out}

pole = $\frac{1}{r_o C_{out}} = \omega = 2\pi f$

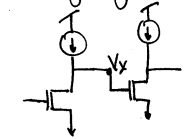
-use value of BW to find r_o

$r_o = \frac{1}{2\pi (1MHz) C_{out}}$



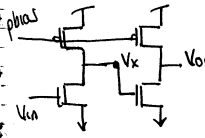
-Once you get r_o, you can find current from r_o vs. I/ω graph

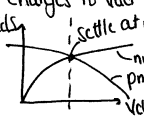
Want higher gain? → Two stages



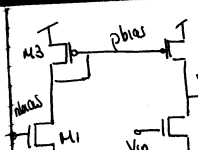
- If DC-coupled, you must ensure V_x is sitting at the right place to provide the desired current
- Where will V_x settle?

Vdd or GND? → No, because one of the devices must be off to allow point to go to Vdd or GND
- pmos supplies current until ~~there~~ V_x charges to Vdd then shuts off. Reverse for GND





- Similar to load line analysis

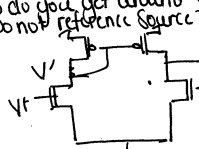


$\left(\frac{W}{L}\right)_{M1} = X \left(\frac{W}{L}\right)_{M2}$

$\left(\frac{W}{L}\right)_{M3} = X \left(\frac{W}{L}\right)_{M4}$

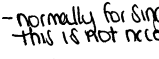
If @ DC
Vin = nbias then Vo' = pbias

How do you get around input bias requirement?
Do not reference source to ground → differential stage

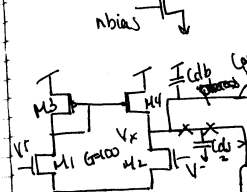


$V_{OUT} = V'$ @ DC

- pick a transistor size to get desired V' value
- normally for single stage set at Vdd/2, but this is not necessary for two-stage



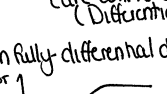
(Using smaller out of first stage)



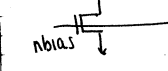
V_X too high for nmos, huge gate overdrive
Instead put output to pmos

- Once the loop is closed, we dont care where output settles (Differential-Single ended)

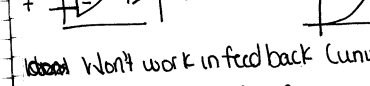
- With fully differential design,



open loop gain, pick point from graph



Won't work in feedback (unity gain). Why?



$A_1 = ?$ $\tau_1 = ?$
$A_2 = ?$ $\tau_2 = ?$

$A_1 = 100 = g_{m_{1,2}}(r_{op} \| r_{on})$

$\tau_1 = (r_{op} \| r_{on})(C_{db4} + C_{db2} + (g_{m5}$

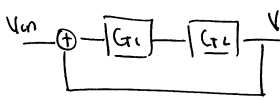
$A_2 = g_{m_5}(r_{op} \| r_{on})$

$\tau_2 = (r_{o5} \| r_{o4})(C_{db5} + C_{db6} + (L)$

- faster pole: lower gain } with the
- slower pole: higher gain } same load

$G_T = g_m r_o \quad g_m = \sqrt{2 I_{ds} \mu_n C_{ox} W/L} \quad r_o = \frac{1}{\lambda I_{ds}}$

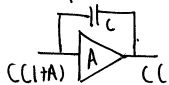
$G_T = \frac{\sqrt{2 \mu_n C_{ox} W/L}}{\lambda \sqrt{I_{ds}}}$ } CS has higher current



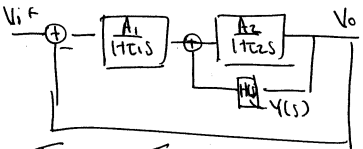
$\frac{G_1 G_2}{1 + G_1 G_2} = \frac{V_{out}}{V_{in}}$ } in unity gain feedback

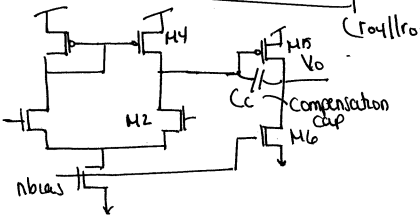
$\frac{V_{out}}{V_{in}} = \frac{A_0 A_1}{(1+\tau_1 s)(1+\tau_2 s) + A_0 A_1}$ → if complex, then amplifier rings

How do you move pole locations?
Want to ensure poles are sufficiently far apart before trying to compensate



- load previous pole by ~AC to move back first pole exactly like minor loop compensation





$(r_{o4} \| r_{o2})(g_{m5}(r_{o5} \| r_{o6}))(Cc)$
A

- Capacitors are bidirectional - so you also get a zero as well