Compensation

Reduced Gain

New gain = (A0 - H1) dB
New unity gain = uc
Reduced gain \Rightarrow lower DC gain \& lower bandwidth

Want PM of 50°

\[ \text{phase margin} \]

Vin

- \[ \frac{1}{\alpha R} + \frac{1}{R_f} + \frac{1}{\beta R_f} \]

\[ \frac{V_{in} - V_{out}}{V_{out}} \]

\[ \frac{V_{in} - V_{out}}{\frac{1}{\alpha R} + \frac{1}{R_f} + \frac{1}{\beta R_f}} = V_{in} + V_{out} \]

\[ \frac{V_{in} - V_{out}}{A_0(s)} \left( \frac{1}{\alpha R} + \frac{1}{R_f} + \frac{1}{\beta R_f} \right) = V_{in} + V_{out} \]

- Amount of input applied is smaller than original \Rightarrow reducing original gain

\[ (V_{in} - V_{out}) \left( \frac{1}{\alpha R} + \frac{1}{R_f} + \frac{1}{\beta R_f} \right) = \frac{V_{in}}{\alpha R} + \frac{V_{out}}{\beta R_f} \]

\[ V_{in} \left( \frac{1}{\alpha R} + \frac{1}{R_f} + \frac{1}{\beta R_f} \right) = V_{out} \left( \frac{A_0(s)}{\alpha R} \right) \left( \frac{1}{\alpha R} + \frac{1}{R_f} + \frac{1}{\beta R_f} \right) + \frac{1}{\beta R_f} \]

- Is there a way to compensate without killing the gain?
  (Keep unity gain frequency at \( \omega_c \))

Pole followed by a zero

\[ \frac{R_f + \frac{1}{\omega C}}{R_f + R_c + \frac{1}{\omega C}} \]

Ex.

\[ V_{in} \]

\[ \frac{1}{R_2} \]

\[ - \frac{1}{C} \]

\[ V_{out} \]

\[ \frac{1 + \frac{sRLC}{1 + \frac{sRLC}{L + \frac{RfR_c}{L + \frac{sRLC}{L + \frac{RfR_c}{L + \frac{sRLC}{L}}}}}}}{L + \frac{RfR_c}{L + \frac{sRLC}{L + \frac{RfR_c}{L + \frac{sRLC}{L}}}}} \]
Generic TF: \[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{R_3}{\omega^2 + 1}}{\omega^3 + 1}
\]

Phase

\[-\frac{\omega^2 - 1}{\omega^3 + 1}\]

Original system \(\phi\)

- Compensation called \(\text{LAG compensation}\)
- Can live with reduced bandwidth in certain applications

Example:

\[
\begin{align*}
V_{\text{in}} & \rightarrow A(s) \rightarrow V_{\text{out}} \\
R_f & \rightarrow R_f \\
R_3 & \rightarrow R_3 \parallel R_2 + \frac{1}{sC}
\end{align*}
\]

\[
R_3 = \frac{1 + sR_2R_3C}{l + s(R_2 + R_3)C}
\]

\[
V_{\text{out}} = \frac{Z_{hf}}{R_3} = \frac{1 + sR_2R_3C}{l + s(R_2 + R_3)C}
\]

If \(R_2 = 0\) \(\rightarrow\) proportional integral controller (P.I. controller)

Another option? \(\) Kill gain, keep bandwidth

System phase

\[\sin\left(\frac{\omega_0}{\omega - 1}\right)\]

- Added \(\phi\) at crossover to get desired phase margin
- Still want to keep original unity gain frequency \(\omega_0\)

- Instead add zero first, pole second
Generic TF = \frac{1}{\alpha} \left[\frac{\alpha s + 1}{ts + 1}\right]

Example network:

\[ \frac{R_1(\frac{V_{in}}{1 + R_1 C})}{R_1 + R_2} \]

\[ V_{out} = \frac{R_2}{R_{in} + R_2 + R_{1}C} \]

\[ V_{out} = \frac{R_2}{R_{in} + R_2 + R_{1}C} \cdot \frac{R_1(1 + R_1 C)}{R_{in} + R_2 + R_{1}C} \]

if \( R = 0 \) - proportional derivative controller (PD-controller) + parallel combination = smaller

Compensation is called LEAD compensation

Op Amp Example

How do you stabilize the plant itself?

\[ V_{out} = \frac{G_1(s)}{1 + G_1(s) G_2(s) H(s)} \]

\[ V_{out} = \frac{G_1(s) G_2(s)}{1 + G_1(s) G_2(s) H(s)} \]
\[ V_{in} \quad \begin{array}{cc} & (\text{G1}(s)) \quad \text{Receives to} \quad \frac{\text{G1}(s)}{1 + \text{G2}(s) \cdot \text{H}(s)} \\
\quad \text{H}(s) \quad \text{H}(s) \quad \text{H}(s) \end{array} \]

Rewritten as
\[ V_{in} \quad \begin{array}{cc} & (\text{G1}(s)) \quad \text{G2}(s) \quad \text{V}_{out} \\
\quad \text{H}(s) \quad \text{H}(s) \quad \text{H}(s) \end{array} \]

Now, rewrite
\[ \text{H}(s) \quad \text{reduction} \quad V_{out} = \frac{\text{G1}(s) \cdot \text{G2}(s)}{1 + \text{G2}(s) \cdot \text{H}(s) + \text{G1}(s) \cdot \text{G2}(s) \cdot \text{H}(s)} \]

Bode plot perspective:

\[ \text{G1}(s) \quad \text{G2}(s) \]

\[ \text{G1}(s) = \frac{A_1}{\omega_n \cdot s + 1} \]

As
Consider \( G_2(s) \) in feedback (unity gain).

- Instead of unity gain at all frequencies, we want unity gain at high frequencies only.

- Extending low but lowered gain.

Real example:

![Circuit Diagram]

Adding cap for minor loop compensation.

\[
\frac{G_\text{overall}}{\text{Gain} \approx \frac{1}{s+1}}
\]
Compensation:
- **LAG - P.I** → high DC gain, lower bandwidth
- **LEAD - P.D** → high + high bandwidth
- **REDUCED GAIN** → proportional (low gain, low bw)

**Minor Loop**

**Dominant Pole**

Ex. Series-Shunt

Ex. Voltage-Voltage (Op-Amp)

Ex. Voltage-Current
Simpler Choice: cascode

Ex. Current - Current

Ex. Current - Voltage

- Host circuits respond in voltage rather than current

- Device always picks free variable to respond with. If current is fixed with a current source, transistor will respond in voltage and vice versa.

- Resistor is between current and voltage source, so it will respond with both current and voltage. Softer gain

Capacitance:

- When referring to a layout, design this length is

Analog Design

3-5x L drawn | L drawn

Digital

Left = L drawn - 2Ld
Review of Inversion / Accumulation Concepts

- Just by applying a potential change material from p-type to n-type.

- In inversion, you will only see the oxide capacitance.
  \[ C_{ox} = \frac{wL}{t_{ox}} \]

In Linear:
- \[ C_{gs} = \frac{1}{2} C_{ox} wL \] (partition half to each junction)
- \[ C_{gd} = \frac{1}{2} C_{ox} wL \]

In Saturation (channel pinched off):
- \[ C_{gs} = \frac{2}{3} C_{ox} wL \]
- \[ C_{gd} = \frac{1}{3} C_{ox} wL + C_{ov} \]
- \[ C_{gs} = \frac{2}{3} C_{ox} wL + C_{ov} \]
- \[ C_{gs} = \frac{1}{3} C_{ox} wL + C_{ov} \]

- Still must include C_{ov} → overlap capacitance.
  (Actually \[ C_{gd} = C_{ov} \] or \[ \frac{1}{2} C_{ox} wL + C_{ov} \])

Also have diodes between source & bulk & drain & bulk.

Small-signal model:
\[ C_{gs} \quad C_{gd} \quad C_{db} \quad C_{gs} \quad C_{gd} \quad C_{db} \]