MC1496, MC1496B

Balanced Modulators/ Demodulators

These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See ON Semiconductor Application Note AN531 for additional design information.

Features

• Excellent Carrier Suppression −65 dB typ @ 0.5 MHz
  −50 dB typ @ 10 MHz

• Adjustable Gain and Signal Handling

• Balanced Inputs and Outputs

• High Common Mode Rejection −85 dB typical

• This Device Contains 8 Active Transistors.

• Pb−Free Package May be Available.* The G−Suffix Denotes a Pb−Free Lead Finish

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 12 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
Figure 1. Suppressed Carrier Output Waveform

Figure 2. Suppressed Carrier Spectrum

Figure 3. Amplitude Modulation Output Waveform

Figure 4. Amplitude–Modulation Spectrum
### MAXIMUM RATINGS \((T_A = 25^\circ C, \text{ unless otherwise noted.})\)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applied Voltage ((V6\text{--}V8, V10\text{--}V1, V12\text{--}V8, V8\text{--}V1, V10\text{--}V4, V6\text{--}V10, V2\text{--}V5, V3\text{--}V5))</td>
<td>(\Delta V)</td>
<td>30</td>
<td>Vdc</td>
</tr>
<tr>
<td>Differential Input Signal ((V8 - V10, V4 - V1))</td>
<td>(+5.0 + (5 + 15R_E))</td>
<td>Vdc</td>
<td></td>
</tr>
<tr>
<td>Maximum Bias Current (I_5)</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction--to--Air</td>
<td>(R_{\text{θJA}})</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>Plastic Dual In-Line Package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature Range (MC1496)</td>
<td>(T_A)</td>
<td>0 to +70</td>
<td>°C</td>
</tr>
<tr>
<td>(MC1496B)</td>
<td></td>
<td>−40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range (T_{\text{stg}})</td>
<td></td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTE:** ESD data available upon request.

### ELECTRICAL CHARACTERISTICS \((V_{CC} = 12\, Vdc, V_{EE} = −8.0\, Vdc, I_5 = 1.0\, mA_{dc}, R_L = 3.9\, k\, \Omega, R_E = 1.0\, k\, \Omega, T_A = T_{\text{low}} \text{ to } T_{\text{high}}, \text{ all input and output characteristics are single--ended, unless otherwise noted.})\) \(\text{(Note 1)}\)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Fig.</th>
<th>Note</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Feedthrough (V_C = 60, mVrms) sine wave and offset adjusted to zero</td>
<td>5</td>
<td>1</td>
<td>(V_{\text{CFT}})</td>
<td>−</td>
<td>40</td>
<td>−</td>
<td>µVrms</td>
</tr>
<tr>
<td>(I_C = 1.0, kHz)</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>140</td>
<td>−</td>
<td>mVrms</td>
</tr>
<tr>
<td>(I_C = 10, kHz)</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>0.04</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>(V_C = 300, mVpp) square wave: offset adjusted to zero</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>20</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>(I_C = 1.0, kHz)</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>20</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>(I_C = 10, kHz)</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>20</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>Carrier Suppression (I_S = 10, kHz, 300, mVrms)</td>
<td>5</td>
<td>2</td>
<td>(V_{\text{CS}})</td>
<td>40</td>
<td>65</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td>(I_C = 500, kHz, 60, mVrms) sine wave</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>50</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>(I_C = 10, MHz, 60, mVrms) sine wave</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>50</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>Transadmittance Bandwidth (Magnitude) ((R_L = 50, \Omega))</td>
<td>8</td>
<td>8</td>
<td>(B_{\text{W3dB}})</td>
<td>300</td>
<td>−</td>
<td>−</td>
<td>MHz</td>
</tr>
<tr>
<td>Carrier Input Port, (V_C = 60, mVrms) sine wave</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>80</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>(I_S = 1.0, kHz, 300, mVrms) sine wave</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>80</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>Signal Input Port, (V_S = 300, mVrms) sine wave</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>80</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>(</td>
<td>V_{\text{C}}</td>
<td>= 0.5, Vdc)</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>80</td>
</tr>
<tr>
<td>Signal Gain ((V_S = 100, mVrms, f = 1.0, kHz;</td>
<td>10</td>
<td>3</td>
<td>(A_{\text{VS}})</td>
<td>2.5</td>
<td>3.5</td>
<td>−</td>
<td>V/V</td>
</tr>
<tr>
<td>(</td>
<td>V_{\text{C}}</td>
<td>= 0.5, Vdc)</td>
<td></td>
<td></td>
<td></td>
<td>−</td>
<td>2.5</td>
</tr>
<tr>
<td>Single--Ended Input Impedance, Signal Port, (f = 5.0, MHz)</td>
<td>6</td>
<td>−</td>
<td>(r_{\text{ip}})</td>
<td>−</td>
<td>200</td>
<td>−</td>
<td>kΩ</td>
</tr>
<tr>
<td>Parallel Input Resistance</td>
<td></td>
<td></td>
<td>(c_{\text{ip}})</td>
<td>−</td>
<td>2.0</td>
<td>−</td>
<td>pF</td>
</tr>
<tr>
<td>Single--Ended Output Impedance, (f = 10, MHz)</td>
<td>6</td>
<td>−</td>
<td>(r_{\text{op}})</td>
<td>−</td>
<td>40</td>
<td>−</td>
<td>kΩ</td>
</tr>
<tr>
<td>Parallel Output Resistance</td>
<td></td>
<td></td>
<td>(c_{\text{oo}})</td>
<td>−</td>
<td>5.0</td>
<td>−</td>
<td>pF</td>
</tr>
<tr>
<td>Input Bias Current (I_{bS} = \frac{I_1 + I_4}{2}; I_{bC} = \frac{I_8 + I_{10}}{2})</td>
<td>7</td>
<td>−</td>
<td>(I_{bS})</td>
<td>−</td>
<td>12</td>
<td>30</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{bC})</td>
<td></td>
<td></td>
<td>(I_{bC})</td>
<td>−</td>
<td>12</td>
<td>30</td>
<td>µA</td>
</tr>
<tr>
<td>Input Offset Current (I_{oS} = I_1 - I_4; I_{oC} = I_8 - I_{10})</td>
<td>7</td>
<td>−</td>
<td>(I_{oS})</td>
<td>−</td>
<td>0.7</td>
<td>7.0</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{oC})</td>
<td></td>
<td></td>
<td>(I_{oC})</td>
<td>−</td>
<td>0.7</td>
<td>7.0</td>
<td>µA</td>
</tr>
<tr>
<td>Average Temperature Coefficient of Input Offset Current ((T_A = −55^\circ C \text{ to } +125^\circ C))</td>
<td>7</td>
<td>−</td>
<td>(</td>
<td>T_{\text{C}<em>{\text{I}</em>{\text{O}}}}</td>
<td>)</td>
<td>−</td>
<td>2.0</td>
</tr>
<tr>
<td>Output Offset Current ((I_6 - I_9))</td>
<td>7</td>
<td>−</td>
<td>(</td>
<td>I_{\text{OO}}</td>
<td>)</td>
<td>−</td>
<td>14</td>
</tr>
<tr>
<td>Average Temperature Coefficient of Output Offset Current ((T_A = −55^\circ C \text{ to } +125^\circ C))</td>
<td>7</td>
<td>−</td>
<td>(</td>
<td>T_{\text{C}<em>{\text{I}</em>{\text{O}}}}</td>
<td>)</td>
<td>−</td>
<td>90</td>
</tr>
<tr>
<td>Common--Mode Input Swing, Signal Port, (I_S = 1.0, kHz)</td>
<td>9</td>
<td>4</td>
<td>(CMV)</td>
<td>−</td>
<td>5.0</td>
<td>−</td>
<td>Vpp</td>
</tr>
<tr>
<td>Common--Mode Gain, Signal Port, (I_S = 1.0, kHz)</td>
<td>9</td>
<td>−</td>
<td>(ACM)</td>
<td>−</td>
<td>−85</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td>Common--Mode Quiescent Output Voltage ((Pin 6 \text{ or } Pin 9))</td>
<td>10</td>
<td>−</td>
<td>(V_{\text{out}})</td>
<td>−</td>
<td>8.0</td>
<td>−</td>
<td>Vpp</td>
</tr>
<tr>
<td>Differential Output Voltage Swing Capability</td>
<td>10</td>
<td>−</td>
<td>(V_{\text{out}})</td>
<td>−</td>
<td>8.0</td>
<td>−</td>
<td>Vpp</td>
</tr>
<tr>
<td>Power Supply Current (I_6 + I_{12})</td>
<td>7</td>
<td>6</td>
<td>(I_{\text{CC}})</td>
<td>−</td>
<td>2.0</td>
<td>4.0</td>
<td>mAdc</td>
</tr>
<tr>
<td>(I_{\text{EE}})</td>
<td></td>
<td></td>
<td>(I_{\text{EE}})</td>
<td>−</td>
<td>3.0</td>
<td>5.0</td>
<td></td>
</tr>
<tr>
<td>DC Power Dissipation ((I_6 + I_{12}))</td>
<td>7</td>
<td>5</td>
<td>(P_{\text{D}})</td>
<td>−</td>
<td>33</td>
<td>−</td>
<td>mW</td>
</tr>
</tbody>
</table>

1. \(T_{\text{low}} = 0^\circ C \text{ for } MC1496\)
   \(T_{\text{high}} = +70^\circ C \text{ for } MC1496\)
   \(= −40^\circ C \text{ for } MC1496B\)
   \(= +125^\circ C \text{ for } MC1496B\)
Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).
Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.
Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degrades the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.
Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal–input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input–signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.
At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single–ended) at low frequencies is defined as the voltage gain,

$$ A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \quad \text{where} \quad r_e = \frac{26 \text{ mV}}{I_5(\text{mA})} $$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors “on” and two transistors “off” (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.
Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5.

$$ V_S \leq I_5 R_E \quad \text{(Volts peak)} $$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common–mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage–current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, P_D = 2 I5 (V6 – V14) + I5 V5 – V14 where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$ I_5 = I_6 = I_{12}, $$
$$ I_B < < I_C \quad \text{for all transistors} $$
then:

$$ R_5 = \frac{V - \phi - 500 \Omega}{I_5} \quad \text{where} \quad R_5 \text{ is the resistor between Pin 5 and ground} $$
$$ \phi = 0.75 \text{ at } T_A = +25^\circ C $$

The MC1496 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common–Mode Quiescent Output Voltage

$$ V_6 = V_{12} = V_+ - I_5 R_L $$

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector–base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

30 Vdc ≥ [(V6, V12) – (V8, V10)] ≥ 2 Vdc
30 Vdc ≥ [(V8, V10) – (V1, V4)] ≥ 2.7 Vdc
30 Vdc ≥ [(V1, V4) – (V5)] ≥ 2.7 Vdc

The foregoing conditions are based on the following approximations:

$$ V_6 = V_{12}, V_8 = V_{10}, V_1 = V_4 $$

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Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

**Transadmittance Bandwidth**

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$
\gamma_{21C} = \frac{i_o (\text{each sideband})}{v_s (\text{signal})} \left| V_o = 0 \right.
$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$
\gamma_{21S} = \frac{i_o (\text{signal})}{v_s (\text{signal})} \left| V_c = 0.5 \text{ Vdc}, \ V_o = 0 \right.
$$

**Coupling and Bypass Capacitors**

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

**Output Signal**

The output signal is taken from Pins 6 and 12 either balanced or single-ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

**Negative Supply**

$V_{EE}$ should be dc only. The insertion of an RF choke in series with $V_{EE}$ can enhance the stability of the internal current sources.

**Signal Port Stability**

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.

An alternate method for low-frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

**TEST CIRCUITS**

Figure 5. Carrier Rejection and Suppression

Figure 6. Input–Output Impedance

Figure 7. Bias and Offset Currents

Figure 8. Transconductance Bandwidth
MC1496, MC1496B

Figure 9. Common Mode Gain

Figure 10. Signal Gain and Output Swing

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, \( f_C = 500 \text{ kHz} \) (sine wave), \( V_C = 60 \text{ mVrms}, f_S = 1.0 \text{ kHz}, V_S = 300 \text{ mVrms}, T_A = 25^\circ \text{C}, \) unless otherwise noted.

Figure 11. Sideband Output versus Carrier Levels

Figure 12. Signal−Port Parallel−Equivalent Input Resistance versus Frequency

Figure 13. Signal−Port Parallel−Equivalent Input Capacitance versus Frequency

Figure 14. Single−Ended Output Impedance versus Frequency

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TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500$ kHz (sine wave), $V_C = 60$ mVrms, $f_S = 1.0$ kHz, $V_S = 300$ mVrms, $T_A = 25^\circ$C, unless otherwise noted.

Figure 15. Sideband and Signal Port Transadmittances versus Frequency

Figure 16. Carrier Suppression versus Temperature

Figure 17. Signal−Port Frequency Response

Figure 18. Carrier Suppression versus Frequency

Figure 19. Carrier Feedthrough versus Frequency

Figure 20. Sideband Harmonic Suppression versus Input Signal Level
The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

**Signal Levels**

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

\[
V = (5)(R_E) \text{ volts peak.}
\]

This expression may be used to compute the minimum value of \(R_E\) for a given input voltage amplitude.
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<table>
<thead>
<tr>
<th>Carrier Input Signal (V_C)</th>
<th>Approximate Voltage Gain</th>
<th>Output Signal Frequency(s)</th>
</tr>
</thead>
</table>
| Low−level dc              | \[
\frac{R_L V_C}{2(R_E + 2r_e) \left( \frac{K T}{q} \right)}
\]                                                                 | \( f_M \)                  |
| High−level dc             | \[
\frac{R_L}{R_E + 2r_e}
\]                                                                 | \( f_M \)                  |
| Low−level ac              | \[
\frac{R_L V_C \text{ (rms)}}{2 \sqrt{2} \left( \frac{K T}{q} \right) (R_E + 2r_e)}
\]   | \( f_C \pm f_M \)          |
| High−level ac             | \[
\frac{0.637 R_L}{R_E + 2r_e}
\]                                                                 | \( f_C \pm f_M, 3f_C \pm f_M, 5f_C \pm f_M, \ldots \) |

2. Low−level Modulating Signal, \( V_M \), assumed in all cases. \( V_C \) is Carrier Input Voltage.
3. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, \( f_C + f_M \) and \( f_C - f_M \).
4. All gain expressions are for a single−ended output. For a differential output connection, multiply each expression by two.
5. \( R_L \) = Load resistance.
6. \( R_E \) = Emitter resistance between Pins 2 and 3.
7. \( r_e \) = Transistor dynamic emitter resistance, at 25°C;
8. \( K \) = Boltzmann’s Constant, \( T \) = temperature in degrees Kelvin, \( q \) = the charge on an electron.

Figure 25. Voltage Gain and Output Frequencies

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low−level modulating signal input and the following carrier input conditions:
1) Low−level dc
2) High−level dc
3) Low−level ac
4) High−level ac

These gains are summarized in Figure 25, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification. All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 \( \mu \)F capacitors on Pins 8 and 10 should be increased to 1.0 \( \mu \)F. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level...
is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

**Doubly Balanced Mixer**

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 30 shows a mixer with a broadband input and a tuned output.

**Frequency Doubler**

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

**Phase Detection and FM Detection**

The MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.
DEFINITIONS

- $f_C$: Carrier Fundamental
- $f_S$: Modulating Signal
- $f_C \pm n f_S$: Fundamental Carrier Sideband Harmonics
- $n f_C$: Carrier Harmonics
- $n f_C \pm n f_S$: Carrier Harmonic Sidebands

**Figure 30. Doubly Balanced Mixer**
(Broadband Inputs, 9.0 MHz Tuned Output)

**Figure 31. Low-Frequency Doubler**

**Figure 32. 150 to 300 MHz Doubler**

L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44–6 Toroid Core.

L1 = 1 Turn AWG No. 18 Wire, 7/32" ID

http://onsemi.com
## MC1496, MC1496B

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC1496D</td>
<td>SO−14</td>
<td>55 Units/Rail</td>
</tr>
<tr>
<td>MC1496DR2</td>
<td>SO−14</td>
<td>2500 Tape &amp; Reel</td>
</tr>
<tr>
<td>MC1496P</td>
<td>PDIP−14</td>
<td>25 Units/Rail</td>
</tr>
<tr>
<td>MC1496PG</td>
<td>PDIP−14 (Pb-Free)</td>
<td>25 Units/Rail</td>
</tr>
<tr>
<td>MC1496P1</td>
<td>PDIP−14</td>
<td>25 Units/Rail</td>
</tr>
<tr>
<td>MC1496BD</td>
<td>SO−14</td>
<td>55 Units/Rail</td>
</tr>
<tr>
<td>MC1496BDR2</td>
<td>SO−14</td>
<td>2500 Tape &amp; Reel</td>
</tr>
<tr>
<td>MC1496BP</td>
<td>PDIP−14</td>
<td>25 Units/Rail</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### MARKING DIAGRAMS

**SO−14**

- **D SUFFIX**
  - CASE 751A

  ![MARKING DIAGRAM SO−14 D SUFFIX CASE 751A](image)

- **P SUFFIX**
  - CASE 646

  ![MARKING DIAGRAM SO−14 P SUFFIX CASE 646](image)

**PDIP−14**

- **P SUFFIX**
  - CASE 646

  ![MARKING DIAGRAM PDIP−14 P SUFFIX CASE 646](image)

A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
MC1496, MC1496B

PACKAGE DIMENSIONS

SO-14
D SUFFIX
PLASTIC PACKAGE
CASE 751A-03
ISSUE F

PDIP-8
P SUFFIX
PLASTIC PACKAGE
CASE 646-06
ISSUE M

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

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