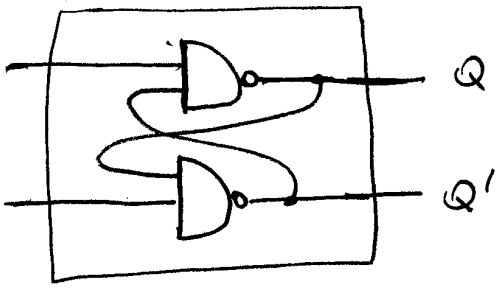
Problem 10

(15 points): In this problem, we investigate a basic latch consisting of cross-coupled NAND gates (rather than NOR gates):



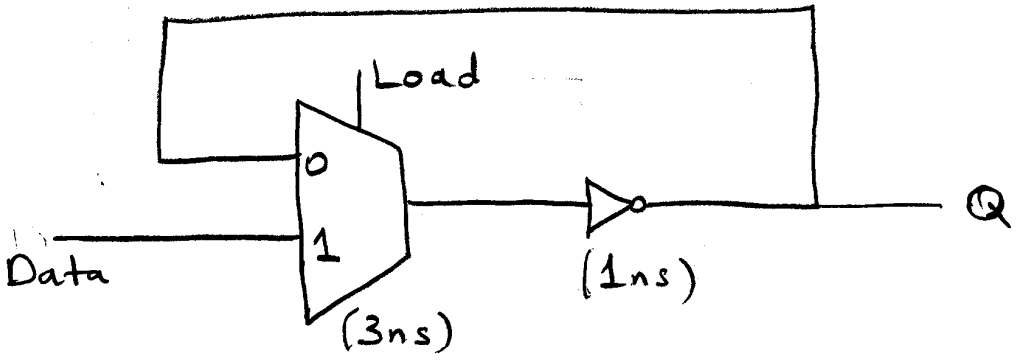
(a) Determine how the two input terminals should be labeled. In our labeling, "R" stands for "reset" and "S" stands for "set". $(R, S) = (1, 0)$ should produce $(Q, Q') = (0, 1)$, and $(R, S) = (0, 1)$ should produce $(Q, Q') = (1, 0)$. Use this labeling for the rest of the problem.

(b) For what input values (i.e. for what values of R and S) does the basic latch "hold" the values of Q and Q'?

(c) What input values of (R,S) are "forbidden"? Why are these forbidden?

Problem 11

(25 points) Some sequential circuits may exhibit "oscillatory" behavior. Examine the following circuit:

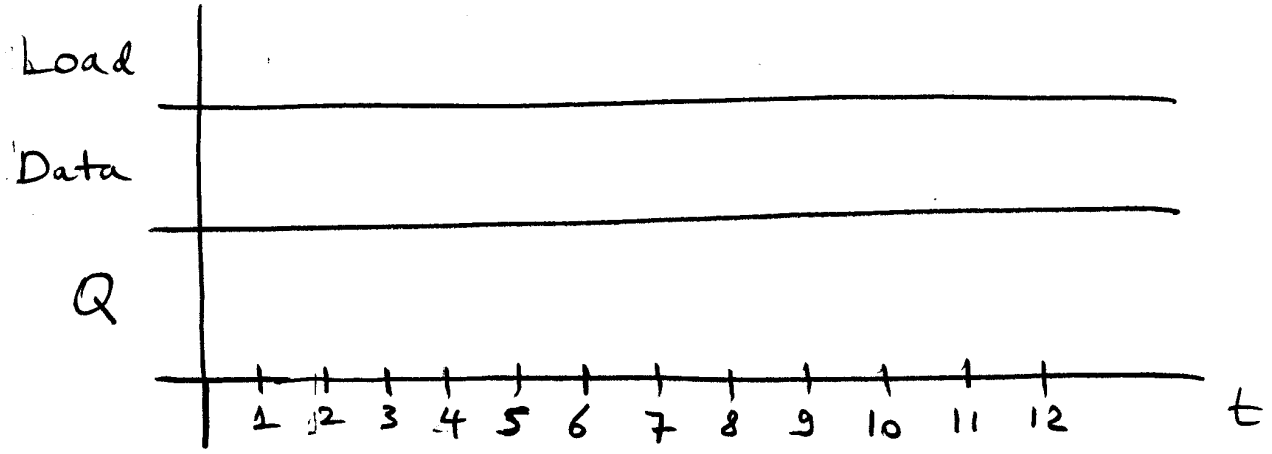


Assume that the mux has a propagation delay of 3 ns, and the inverter has a propagation delay of 1 ns.

(a) When Load = 1, does Q have a stable value?

(b) Assume that initially, Load = 1 and Data = 1

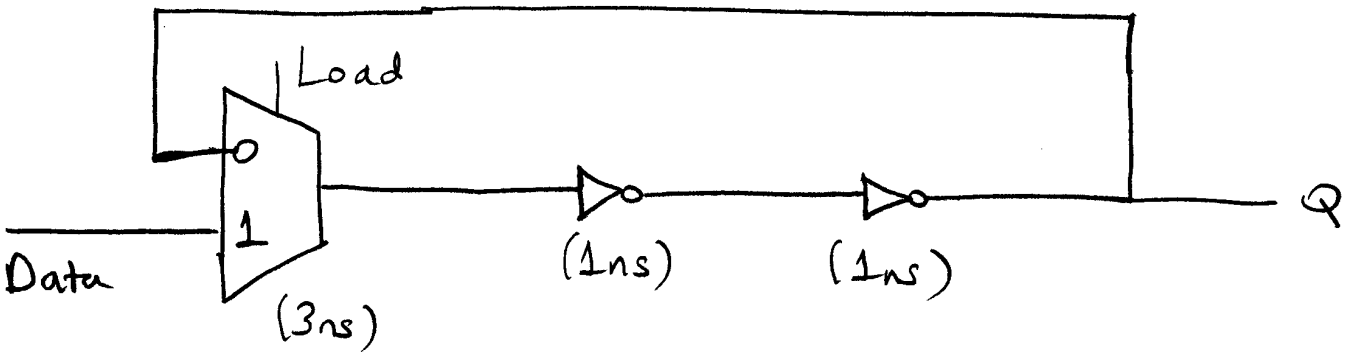
What happens when Load becomes 0 at time t=2 ns. Below, show this event and what ensues.



(c) Can this circuit be considered a "storage element" (i.e. "memory element")? Why or why not?

(d) If we did not know the propagation delay of the inverter (but knew that of the mux), could the above circuit be used to estimate the propagation delay of the inverter?

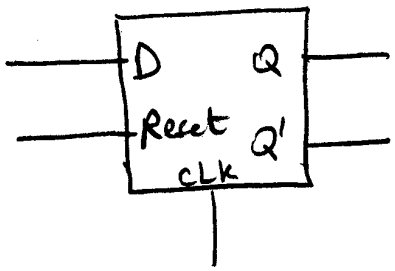
(e) Now, consider



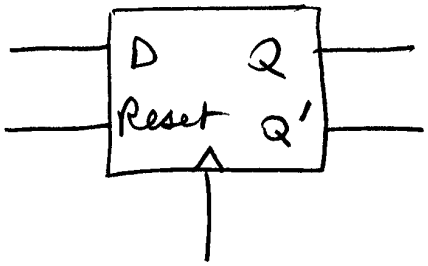
Without drawing the timing diagram, can you describe the <u>key features</u> of this circuit? (You have to determine what the key, i.e. important features are here.) How is the behavior of this circuit different from the original? Can this circuit be used as a storage element?

Problem 12

(40 points) In this problem, assume that the clocked latches and the flip-flops have ideal operation (i.e. no propogation delays, set-up and hold times). Further, assume that the clocked D-latch has asynchronous reset, and the D flip-flop has synchronous reset. The schematics for these units are shown below:

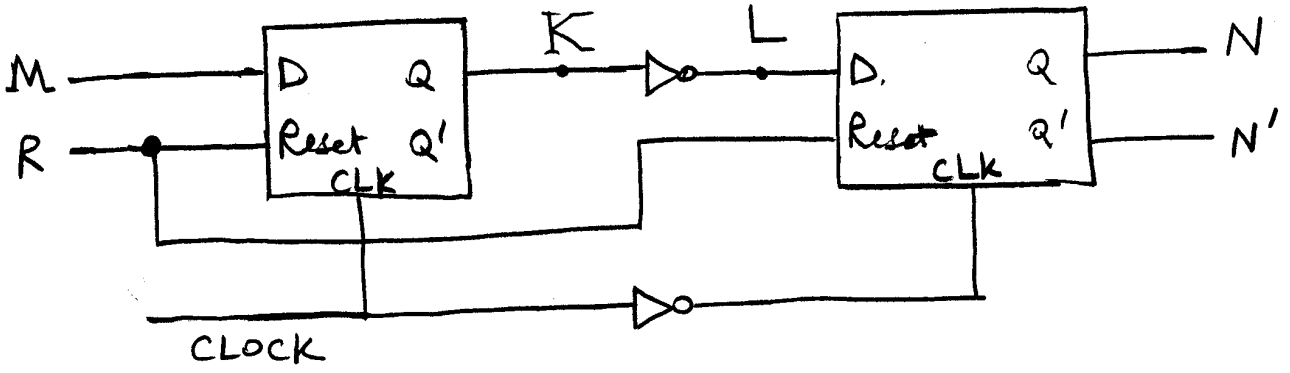


clocked D-latch



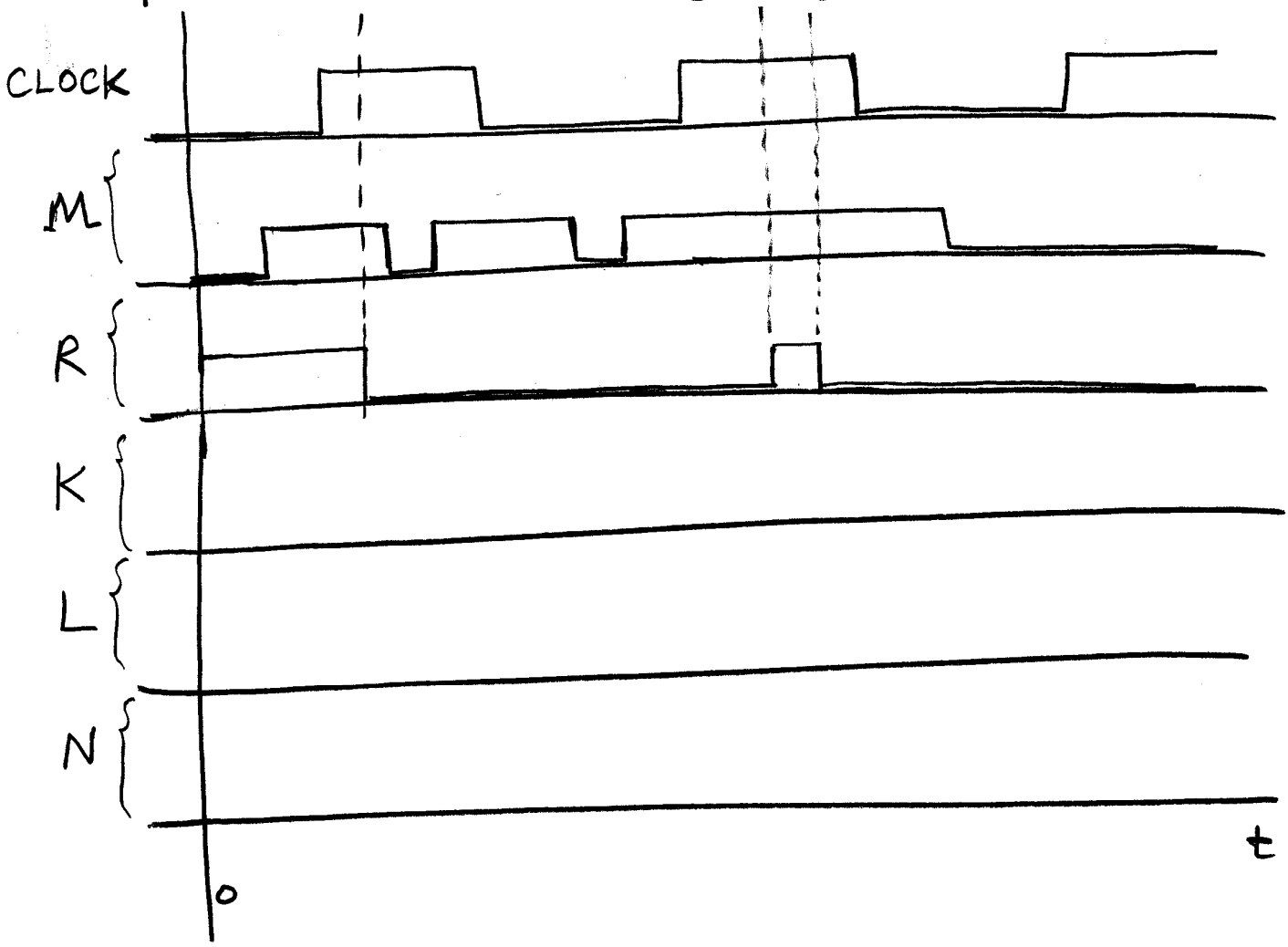
D flip-flop

(a) For the following circuit,



The inputs are M, R and CLOCK, and the outputs are N and N'. Assume zero propogation delay for each inverter shown above.

Complete the following timing diagram:



When drawing the timing diagram, assume that at $t=0$, you do <u>not</u> know the initial state of the circuit. (Denote unknown values by a large X on the diagram.)

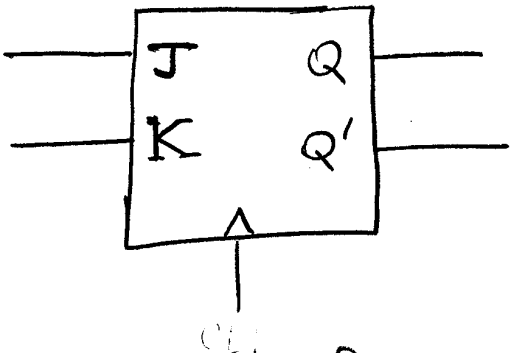
(b) Now, we replace <u>each</u> clocked D latch in part(a) by a D flip-flop. Draw the resulting schematic. (There will be 2 D flip-flops.) Draw the timing diagram for K, L, N given the same CLOCK, M, R as in part (a).

(c) What differences do you observe between the outputs N in (a) and (b)?

(d) Can you think of any uses for the circuit in part(a)? In part (b)? Can you describe in words what each one does?

Problem 13

(15 points) We introduce the JK flip-flop:

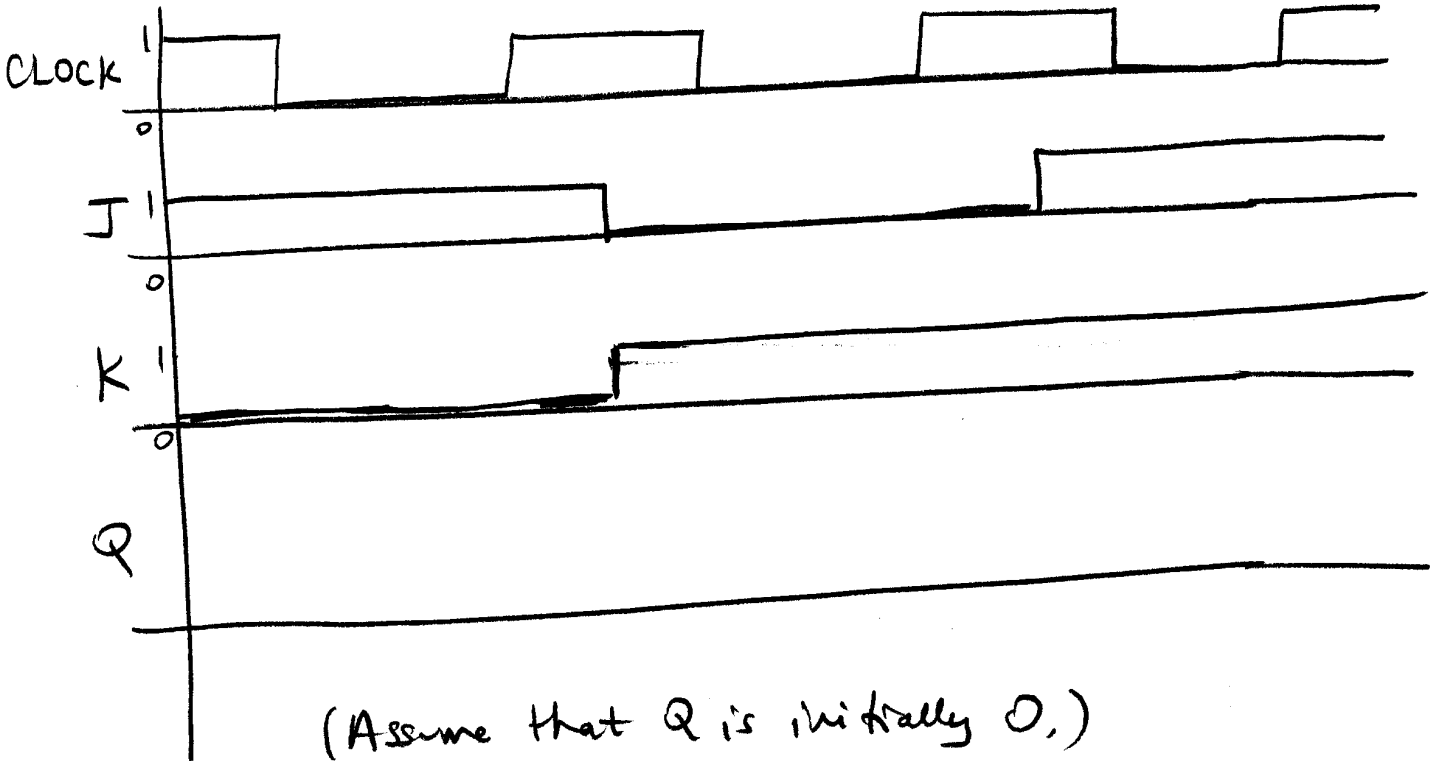


(This schematic is for the positive-edge triggered JK flip-flop. There is also a negative-edge-triggered version)

The operation is as follows: If $J=1$ and $K=0$, the flip-flop output is set to $Q=1$ (at the active clock edge). If $K=1$ and $J=0$, the flip-flop output is reset to $Q=0$ (at the active clock edge), If $J=1$ and $K=1$ at the active clock edge, then Q "toggles" (i.e. if it was 0, it becomes 1; and if it was 1, it becomes 0). If $J=0$ and $K=0$, then the flip-flop holds Q's value.

(a) Based on the above information, write down the state table, and then the next-state equation for the JK flip-flop.

(b) Fill in the timing diagram for a positive-edge triggered JK flip-flop.



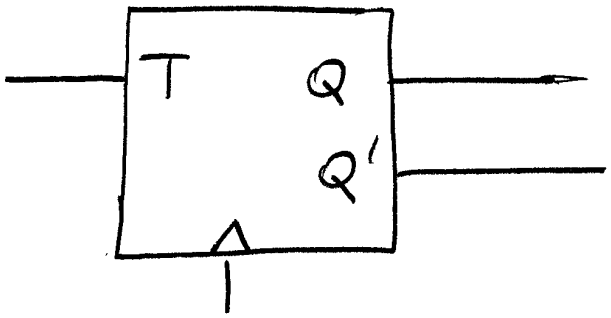
(Assume that Q is initially 0.)

(c) Construct a D flip-flop using only JK flip-flops as memory elements. (If needed, you can use external combinational logic.)

(Show the schematic.)

Problem 14

(20 points) We introduce the T flip-flop. In this name, "T" stands for "toggle".

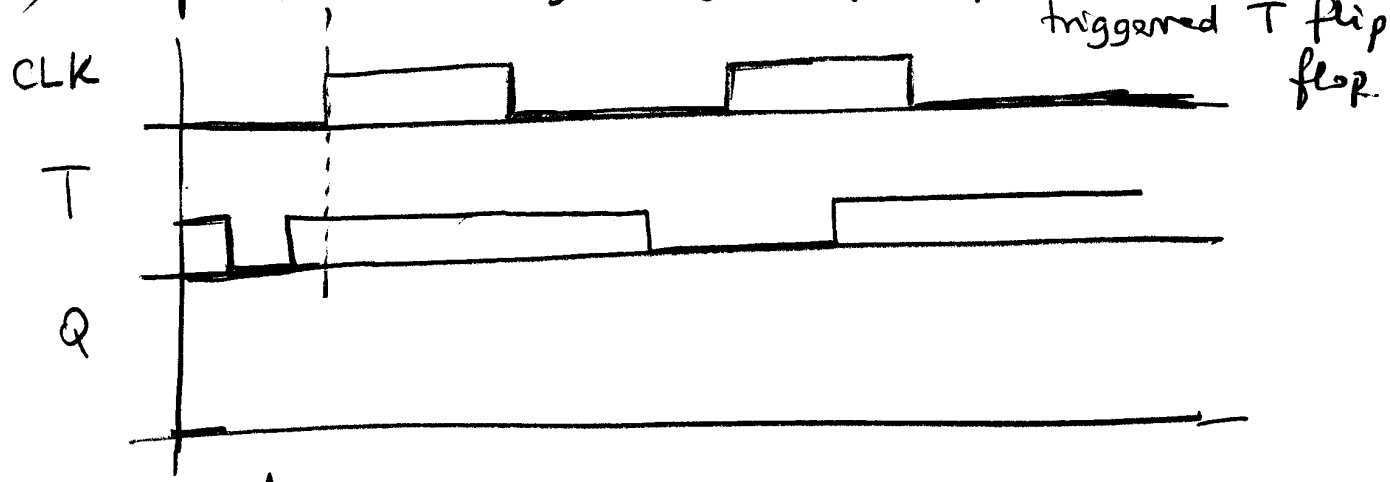


(This is a positive edge-triggered T flip-flop.)

The operation is as follows: At the active edge of the clock, if T=1, then Q "toggles"; if T=0 instead, it holds Q.

(a) Write down the state table and the next-state equation for the T flip-flop.

(b) Complete the timing diagram for a positive edge triggered T flip flop.



Assume Q=0 initially.

(c) Construct a T flip-flop

(c1) using only D flip-flops as memory elements,

(c2) using only JK flip-flops as memory elements.

(d) Where and why would you prefer a T flip-flop over a D flip-flop? Is a parallel-access shift register more easily designed using D or T flip-flops? What about a counter? Why?