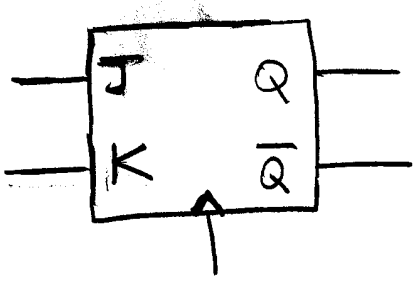
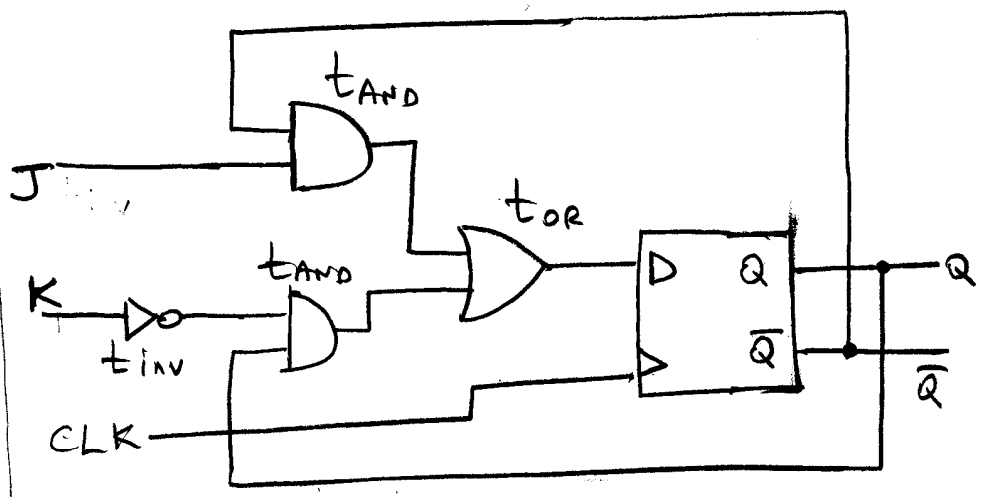
Problem 19

(25 points) Consider the following implementation of a JK flip-flop:



(interface)



(IMPLEMENTATION)

- Assume that the gates have delays as shown. Further, assume that t_{su}, t_h, and t_p (CLK-to-Q) for D flip-flop are given.
- Using the simple gate delay model, derive:

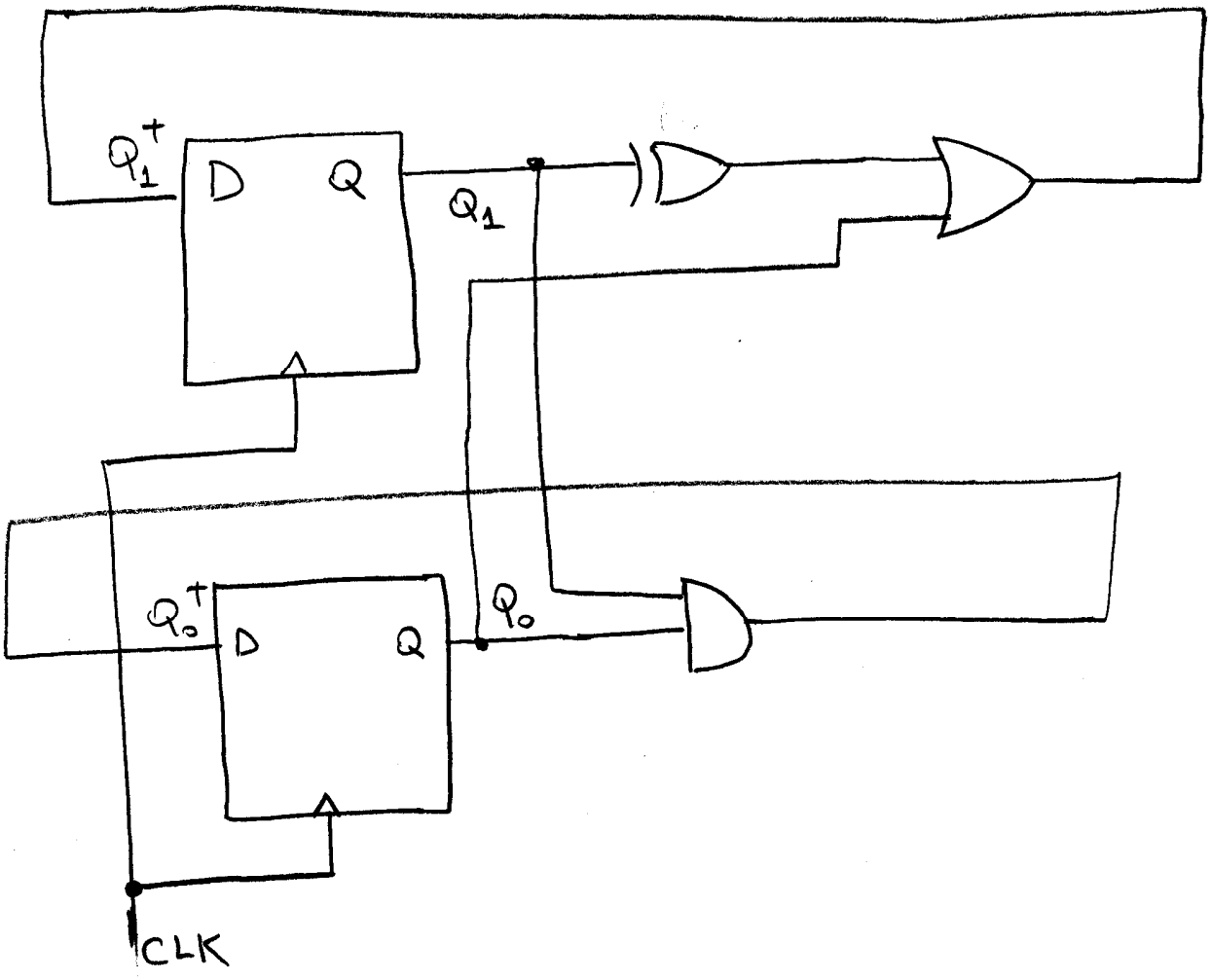
(a) the set-up time of this JK flip-flop,

(b) the hold time of this JK flip-flop,

(c) the CLK-to-Q propagation delay of this JK flip-flop.

Problem 20

(25 points) The circuit for this problem is given below:



The following parameters are given (i.e. their values are known):

t_{XOR} : delay of the XOR gate

t_{OR} : " " " OR "

t_{AND} : " " " AND "

t_h : hold time of D flip-flop.

t_{su} : set-up time of D flip-flop

t_p : the CLK-to-Q prop. delay of the D flip-flop.

Using these parameters, answer the following questions:

(a) What is the <u>maximum</u> clock frequency such that this FSM will still work correctly? (You must show your derivation, i.e. how you arrived at the answer. The answer will be in terms of the above parameters.) (10 points)

(b) For this part only, assume that (5 points)

$t_{XOR} = 1.0$ ns	$t_{su} = 1.2$ ns
$t_{OR} = 1.4$ ns	$t_p = 2.1$ ns
$t_{AND} = 2.0$ ns	$t_h = 0.3$ ns

Find the maximum clock frequency, using your expression in (a).

(c) In terms of the parameters (other than t_h), find the maximum hold time that a D flip-flop in this circuit can <u>require</u> such that the circuit will still be operational? (Hint: Trace the "fast" signals through the combinational circuit.) (10 points)