University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 152A Digital Design Principles
Course Syllabus

A. Basic Course Information

Instructor: Prof. Volkan Rodoplu
Room 4113, Engineering I
Email: vrodoplu@ece.ucsb.edu
Office Hours: TBA

Lecture Hours and Location:
5:00 PM - 6:15 PM Tuesday & Thursday LSB 1001

Course web page:
http://www.ece.ucsb.edu/courses/ECE152A/152A_F05Rodoplu

Teaching Assistants:

Sean Gordoni	sgordoni@umail.ucsb.edu
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Labs:

Code	Day	Hours	TA
11163	M	2:00 - 4:50 PM	Saeed
11171	W	8:00 - 10:50 AM	Yi-Wei
11189	T	7:00 - 9:50 PM	
11197	M	7:00 - 9:50 PM ***	

*** The Monday morning lab section has been moved to Monday night. If you cannot switch to Monday night, you are allowed to switch to other sections if there is space in the other section.

All labs are held in Engineering I, Room 1124.

Weekly Review Session:
Wednesday, 6:00 PM, location: TBA

TA Weekly Office Hours:
Will be held in Engineering I, Room 1124 (DigiLab).

See the course web page for the TA office hours. (You may go to the office hours of any TA, not just your own lab section TA.)

Textbook and References:

(Required) Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 1st edition, McGraw-Hill, 2003.

(Optional) Charles H. Roth, Jr., "Fundamentals of Logic Design", 5th Edition, Brooks/Cole, May 2003.

Grading:
35% Laboratories
[Lab 1: 5%, Lab 2: 5%, Lab 3: 5%, Lab 4: 10%, Lab 5: 10%]
10% Homework
20% Midterm Exam
35% Final Exam

Final Exam Date:

Check the course catalog for time. Place will be announced on the course web page.

Prerequisites:
Know the material in Chapters 1-5, 7-9 of Charles Roth's book "Fundamentals of Logic Design" (5^{th} edition).

B. Tentative Course Calendar and Topics:

Week of	**Review Session**	**LABORATORY**	**Tuesday Lecture**	**Thursday Lecture**
Sep.19				(Lecture 0) Organizational Lecture - DigiLab account sign-up - Review session poll - To-do list.
Sep.26	No session	Introduction to Lab Equipment and Software.	(Lecture 1) Review of Boolean algebra, map word problem to combinational logic.	(Lecture 2) Algebraic simplification theorems, Boolean functions, bubble-pushing,

			Reading: Ch. 1.1, 2.1-2.4, 3.5 Find a lab partner.	functional completeness, NAND/NOR-only circuit design. Reading: Ch. 2.5-2.8
Oct.3	Wiring principles, resistors, capacitors, fan-in, fan-out; practical lab advice; answer questions on Laboratory 1.	Lab 1 check-in (Lab 1: Basic Combinational Logic Design with Seven-Segment Display) [Lab # 1 Pre-lab due]	(Lecture 3) Muxes, half and full adder, Boolean cube, K-maps, maxterm and minterm expansions, don't cares. Reading: Ch.. 4.1-4.4, 4.8, 5.1-5.2, 6.1	(Lecture 4) Propagation delay, timing diagram, critical path, Verilog for combinational logic; interface and implementation. Reading: Ch. 2.9-2.10, 4.12, 6.2-6.4
Oct.10	Answer questions on Lab. 2; simple adders; Verilog for combinational logic design.	Lab 1 check-out; Lab 2 check-in. (Lab 2: 4-bit Adder Design: Verilog, Simulation, download to FPGA.) [Lab # 2 Pre-lab due]	(Lecture 5) Basic latch, D latch and D flip-flop (behavioral); design of registers, shift registers and counters. Reading: Ch. 7.1-7.4, 7.8-7.11 [HW # 1 due]	(Lecture 6) Timing diagrams of latches, flip-flops, shift registers, counters; T flip-flop, JK flip-flop, use of tristate buffers with memory elements.
Oct.17	FSM design example (map word problem; state diagram, state assignment, state table); answer questions on Lab. 3.	Lab 2 check-out; Lab 3 check-in (Lab 3: Counter Design) [Lab # 3: No pre-lab due]	(Lecture 7) Map word problem to FSM; state diagram, state table, state assignment; Mealy/Moore machines. Reading: Ch. 8.1-8.3 [HW # 2 due]	(Lecture 8) Timing diagrams for Mealy/Moore machines; map state diagram to flip-flop implementation. Reading: Ch. 8.1-8.3
Oct.24	No review session.	Lab 3 check-out [Only Parts 1, 2 and 3 are due] Lab 4 check-in (Lab 4: Thunderbird FSM	MIDTERM EXAM (in class)	(Lecture 9A) Verilog for sequential design; RTL and behavioral Verilog for FSMs.

		design; ModelSim simulation; download to FPGA; software/hardware interface for testing) [No pre-lab for Lab 4.]		Reading: Ch.8.4, Appendix A
Oct.31	Designing sequential systems with Verilog; examples.	Lab 4 continues [Lab 4: Part 1 is due]	(Lecture 9B) Examples of Mealy/Moore machines; mapping word problems to state diagrams.	(Lecture 10) More examples of Mealy/Moore machines, and Verilog for sequential machines.
Nov.7	General-purpose FSM design; answer questions on Lab. 5.	Lab 4 check-out; Lab 5 check-in (Lab 5: General-purpose FSM; RAM-based design.) [Lab # 4 Check-out: Parts 2, 3 and 4 due] [No Pre-lab for Lab 5]	(Lecture 11A) Timing of sequential circuits: set-up, hold times, propagation delays, minimum clock period Reading: Ch 10.3.1-10.3.2 Reading for Lab 5: Ch 8.5 (Serial Adder)	(Lecture 11B) Examples of timing problems in sequential circuit design. [HW # 3 due]
Nov.14	Carry-lookahead adder review; CMOS circuits; RAM (S-RAM, D-RAM); answer questions on Lab.5.	Lab 5 continues [Lab 5: Parts 1 and 2 due]	(Lecture 13) CMOS technology: Combinational logic, and RAM (S-RAM, D-RAM) Reading in Course Reader: Section from Randy Katz on RAM.	(Lecture 14) 2's complement arithmetic, adder/subtractor, carry look-ahead adder. Reading: Ch. 5.3-5.4 Course Reader: Section from Randy Katz on carry look-ahead adder. [HW # 4 due]
Nov.21	No review session	Lab 5 Check-out: Parts 3 and 4 due.	(Lecture 15) Area-delay analysis of adders; solving problems.	Thanksgiving Holiday (No lecture)

Nov.28	No review session	TA's will hold office hours to answer any questions.	(Lecture 16) Finish up adders; Course evaluations Review Session 1 (for Final Exam)	(Lecture 17) Review Session 2 (for Final Exam) [HW # 5 due]

C. Graded Course Work and Rules:

C. 1. Laboratory Rules and Recommendations:

Rules:

The labs will be done in teams of two people. You may not have someone else outside the course or a member of another team in class do your lab (or sections of the lab) for you. It is fine to discuss, to get help from others in class as well as other students on debugging, but once you understand the problem, you (as a team) must go ahead and carry out the solution on your own.

Usually, we will not accept any late labs. Each lab's grading is divided into demonstrable milestones. Any milestones completed before the deadline, if demonstrated and are correct, will get full credit. For some labs, we may advertise a late policy of a few days. In that case, any milestone of the lab that is late will get 50% of the credit that would be earned if that milestone had been completed on time.

There is usually a problem set due at the beginning of each lab. HAND IN A CLEAR PHOTOCOPY OF YOUR PROBLEM SET SOLUTIONS AT THE BEGINNING OF THE LAB. KEEP THE ACTUAL WRITE-UP FOR YOURSELF; YOU WILL BE USING THAT IN THE REST OF THE LAB.

If you burn a board that you have checked out from the ECE shop, you will be charged 1/2 of the cost of the board, in order to get a replacement. Follow the wiring guidelines for each lab.

Recommendations:

The strategy that we recommend for the labs is to start early and make as much progress as possible on your own as a team. Use the lab sessions very well: Ask the TA's the troubling points to remove any problems that are preventing your progress in the labs. Go to the TA's office hours held in the laboratory room for extra help. When you do the labs, try to understand fully why things are the way they are. The clarity of the top level design on any project is extremely important. Before you jump into

implementation, make sure that you have understood the problem at the highest level of abstraction correctly and designed the top level solution with the tools at this level. If you have any doubts about the project specification, it is important to clear them as high up in the design abstraction chain as possible.

C. 2. Homework Rules and Recommendations:

Rules:

Homework is due in the HOMEWORK BOX on the 5th floor of Engineering I, on the date and time shown for that homework on the course web page. Late homework gets a zero. The only exception to this is a well-documented, legitimate emergency.

You are allowed to collaborate with other students in this class on the homework assignments. You may not copy someone else's solutions, solutions from the instructor's manual or solutions from previous years. You may not have someone outside the course (e.g. a student who has taken the course before) do you homework for you. You may discuss the homework assignments and solution strategies with anyone, but the work you hand in must be your own write-up.

Recommendations:

The strategy that we recommend is to start the homework early and do as much of the homework as possible on your own. Then, get together with other students who have done the same to check your answers with each other's, discuss the points on which you disagree, find correct solutions and then write up the corrected solution yourself.

C. 3. Exam Rules and Recommendations:

Rules:

The exam rules apply to all of the exams. At the end of the exam, we will tell you to stop writing and raise your exam booklet high. If you continue writing, we will deduct roughly 5% per minute from your exam score. Wait in your seat until we announce that ALL of the exams in the exam room have been collected.

If you finish your exam early, you may hand in your exam and then leave the exam room until 10 minutes before the exam is over. Once you hand in your exam, you may not get it back to make further changes. After we enter the last 10 minutes of the exam, even if you finish early, you need to wait in your seat for time to be called.

If you arrive late for an exam, you will not be given extra time at the end of the exam.

If you need any special accommodations for the exam room, you need to talk to me in advance and as soon as you become aware of such special needs.

You must write the exam on your own. Receiving or giving help during the exam is prohibited. All exams will be in class and will be closed book. You may not bring any devices to the exam on which equations can be stored or any wireless devices that can retrieve such data. On some exams, we may allow you to use calculators only for computational purposes.

If we cannot read your answer, we cannot give you any credit. If you have very bad handwriting, please see me at the beginning of the quarter.

If you do not show up for an exam, you receive a zero for that exam. The only exception to this rule is an emergency that is well-documented. As soon as you become aware of such an emergency, you need to contact me so that I can find a reasonable solution.

You must write your name on the sheet that contains the exam questions and hand in this sheet along with your exam. We will return the exam questions along with graded exams.

It is usually impossible to take the midterm or final exams earlier or later. However, in case of emergencies, we may give you an early or late exam. We cannot give guarantees on how much more difficult the make-up exam will be and will not make adjustments to the score according to the level of difficulty of the make-up exam.

Recommendations:
The strategy that we recommend for the exams is (1) clear up your confusions way before the exam by going to the office hours of the professor and the TA's, (2) have a clear understanding of the digital design chain, i.e. how high-level abstractions are successively mapped down to low layers.

A common pitfall in studying for exams is to "go over" the lecture and homework material by flipping pages and recognizing correct solutions. This will usually not prepare you well for exams in this course. You need to take new problems (from your textbook, previous year's exams that we hand out, or from other textbooks or sources) and actively solve new problems. If you had difficulty with a homework problem, don't look at any solutions or textbooks; instead try solving the problem again from scratch and figure out where you are having difficulty.

The exams will cover all of the lecture notes, reading, laboratories and discussions that far. The final exam will be comprehensive. All of the exams are design-oriented. On exams, you will typically be given a word problem and asked to produce a design that solves the problem. It is very important to internalize the design process and get the system timing right on these problems. A superficial understanding of the material will not suffice.

D. Policy on Student Misconduct:

We will be vigilant to detect student misconduct and to investigate any reported cases. In this course, copying someone else's solutions, copying solutions from the instructor's manual, copying solutions from previous years' labs and student folders, using books in a closed-book exam, copying from someone else during an exam, are first-degree offenses. If we find any evidence of these or other offenses, we will refer the case immediately to the committee on student misconduct.

E. Mapping to Letter Grades:

The letter grade that you receive in this course will reflect your level of understanding of the material and the level of design skills you have developed in this course.

The following is an estimate of how the letter grades will be assigned. (Some of these points, for example, how much of the homework you can do by yourself, is for your self-assessment. As we said, it is fine to get together with others after you have given your best effort at the homework yourself. But high homework scores due to collaboration with others should not delude you into thinking that you know the material.)

A+: Extraordinary performance, 95-100% on almost everything; can typically do 100% of the homework by him/herself.

A: Student has excellent understanding and mastery of the material. Typically, this student can do 90-100% of the homework correctly by him/herself; exam performance reflects solid understanding of the design process, with at most a few minor design flaws; can get the timing right on almost all designs; typically, lab scores are 90-100%.

A-: Typically, can do 80-90% of the homework correctly by him/herself; exam performance shows at most one main design flaw and a few minor ones; can get timing right on most designs; lab scores are typically 90-100%.

B+: Typically, can do 70-80% of the homework correctly by him/herself; exam performance shows a couple of main design flaws (per exam); lab scores are typically 80-90%.

B: A rough measure is that this student can still be hired as a digital designer; can do 70-80% of the homework correctly by him/herself; exam performance shows about three main design flaws (per exam); lab scores are typically 75-85%.

B-: Student is below the requirements for what we would consider adequate level of understanding for digital design work in industry; can do 60-70% of the homework correctly by him/herself; exam performance shows more than a few design flaws (per exam); lab scores are typically 60-75%.

C: Student lacks a good understanding of digital design; can do 50-65% of the homework by him/herself; exam performance shows a superficial understanding of digital design; lab scores are typically 50-60%.

D: Can typically do 45-60% of the homework by him/herself; exam performance shows a shaky understanding of digital design; lab scores are typically 45-55%.

F: Can typically do 0-45% of the homework by him/herself; exam performance is completely inadequate; did not get even the main messages of the course; lab scores are typically 0-45%.