ECE 152A Lecture # 0

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Useful Course Information

- Professor: Volkan Rodoplu (vrodoplu@ece.ucsb.edu)
- Lectures: TR 5:00-6:15 PM, LSB 1001
- Course web page: http://www.ece.ucsb.edu/courses/ECE152A/152A_F05Rodoplu
  - Read course web page regularly for announcements

Teaching Assistants

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What is ECE 152A?

- Junior-level course on digital design principles
- Prerequisites: Basic knowledge of digital design (K-maps, Boolean minimization, combinational logic problems)
- Basic course components: Lecture, laboratory, homework
- Leads to courses: ECE 154 (computer architecture), ECE 152B (digital design methodologies), ECE 124 (VLSI design)

What will I learn in this course?

- Very useful and fundamental hardware design skills that you can use in industry internships:
  - Sequential design (e.g. designing a simple controller)
  - Experience with an FPGA (Field-Programmable Gate Array) board (XSA50)
  - **Verilog**: a hardware description language that is used throughout industry for digital design.
  - Structures like ADDERS that go into the ALU in the CPU of a processor.

Applicable to Design Paradigms

- The skills that you develop in this course are also useful for all these digital design paradigms:
  - Customized, highly hand-optimized design of microprocessors (such as Intel's).
  - DSPs (Digital Signal Processors) such as the TI (Texas Instruments) DSP chips and co-processors (but also need ECE 153 and ECE 154).
  - ASIC (Application Specific Integrated Circuit) design (cell phone components; wireless LAN chips).

Course Organization

- Weekly lectures
- Laboratory: Very significant component of the course.
  - Weekly laboratory sections.
  - Labs are synchronized with the lectures.
  - Work in teams of 2 people.
- Homework
- Exams

Outline of Course Calendar

- Weeks 1-2: Review of combinational logic, K-maps; Verilog for combo design
- Weeks 3-5: Sequential logic, counters, FSMs; Verilog for sequential design
- Week 6: FSM optimization, timing
- Week 7: Adders; CMOS; RAM
- Week 8: Datapath and control
- Weeks 9-10: Course review; review sessions
  - **See detailed course calendar in syllabus**

Textbooks

- (Required) Brown & Vranesic, *Fundamentals of Digital Logic with Verilog Design*
  - Very well-written book that actually explains the Verilog language while developing the digital design principles
- (Required) Course Reader available at the UCSB bookstore
- (Optional) Charles Roth, *Fundamentals of Logic Design*
  - ECE 15A textbook

Assignments

- **Reading assignments**:
  - In course calendar in syllabus (for each lecture)
- **Pre-lab (or Lab problem set):**
  - Photocopy due at beginning of certain labs (you keep the real one)
  - Noted in course calendar; deadlines shown on the course web page
- **Homework:**
  - Due in HOMEWORK BOX, 5th Floor, Engineering I
  - Due dates on course web page and in course calendar in syllabus
- **Laboratories**
  - Due dates are on course web page

ALL HOMEWORKS and ALL LABS have already been posted on the course web page.

Announcements

- Move Monday morning section to Monday night: 7:00 – 9:50 PM
  - Can all Monday morning students switch to ANY other section?
- Weekly review sessions are planned to take place Wednesday nights, starting next week (check course web page)
  - Aim: to answer questions about lectures and homework (and about laboratory if needed).
- To access SOLUTIONS on the course web page: username:____, password:_____