## **Troubleshooting ModelSim:**

- Start Project Navigator, open your verilog files. Copy and paste this verilog code as text in separate file and save it in a different folder than your lab2 folder.
- Now, Close project navigator.
- Delete all the files from Lab2 folder including imported libraries.
- Now, start project navigator and File -> New Project
- Click on the browse button and select your lab 2 directory.
- Type in a Project Name and click Next. Select xc2s50 for your Device value. Make sure the Generated Simulation Language is Verilog, not VHDL.
- To add your verilog code, from the left panel, right-click on xc2s50-6tq144, and select new source.
- Choose Verilog Module from the list, and type in a file name. (If you have saved your verilog in a text file, then copy-paste your code from that.)
- To test your verilog code, save your work, (remember it is necessary to save your work) and click on create new source.
- Select Test Bench Waveform from the list, and type in a file name. In the Combinatorial Timing box, input 2 for both Check outputs and Assign inputs. Click OK. Input your test patterns here, and save your file.
- Now, click on your .tbw file in left panel and then in the bottom-left panel, select ModelSim Simulator and then double click on simulate behavior model.
- The wave-default window will show the results of your values. (click on "Zoom full" button, not "zoom 2x", to see your waveform)
- If there is an error in your input pattern, it will show a number in the left panel of the wave window.
- (If ModelSim didn't show anything, then you need to import libraries. Import libraries one by one as specified in the document on the course page. If it shows "Vcom failed" error. Click on cancel and try to import other remaining libraries.Whenever there is an error, click on cancel. At the end, close ModelSim and start it again from Project navigator as shown above.)
- After you are through with your simulation, proceed with creating "implementation constraints file" as given at the back of your lab-2 handout and your implementation.

## If anybody has problems, please let us know.