ECE 152A-Fall 2008

University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 152A Digital Design Principles
Course Syllabus

A. Basic Course Information

Instructor: Prof. Volkan Rodoplu
Room 4113, Engineering I
Email: vrodoplu@ece.ucsb.edu
Office Hours: TBA

Lecture Hours and Location:
3:30 PM - 4:45 PM Monday & Wednesday
Location: (!) Theater Dance (TD) 2600
(This is next to the Humanities Building.)

Course web page:
http://www.ece.ucsb.edu/courses/ECE152A/152A_F08Rodoplu

Teaching Assistants:

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Labs:

All labs are held in Harold Frank Hall, Room 1124.

TA Weekly Office Hours:
Will be held in Engineering I, Room 1124 (DigiLab).

See the course web page for the TA office hours. (You may go to the office hours of ANY TA. That is, you are not limited to those of your own lab section TA.)

Textbook and References:

(Optional) Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 1st edition, McGraw-Hill, 2003.

(Optional) Charles H. Roth, Jr., "Fundamentals of Logic Design", 5th Edition, Brooks/Cole, May 2003.

Grading:

35% Laboratories
[Lab 1: 5%, Lab 2: 5%, Lab 3: 5%, Lab 4: 10%, Lab 5: 10%]
10% Homework
20% Midterm Exam
35% Final Exam

Final Exam Date:

Check the course catalog for time. Place will be announced on the course web page.

Prerequisites:

Know the material in Chapters 1-5 of Charles Roth's book "Fundamentals of Logic Design" (5^{th} edition).

B. Tentative Course Calendar and Topics:

Week of	**LABORATORY**	**Monday Lecture**	**Wednesday Lecture**
Sept.29	Go to your lab section; laboratory orientation, laboratory board and wiring basics, and DigiLab account set-up; Find a lab partner.	(Lecture 0.1) Organizational Lecture - DigiLab account sign-up - To-do list.	(Lecture 0.2) PRE-TEST (30 minutes) To test your knowledge from prerequisite course. (Please study K-maps, minimum SOP's.)
Oct. 6	Lab 1 check-in (Lab 1: Basic Combinational Logic Design with Seven-Segment Display)	(Lecture 1) Review of Boolean algebra, map word problem to combinational logic. Optional Reading: B&V: Ch. 1.1, 2.1-2.4, 3.5	(Lecture 2) Algebraic simplification theorems, Boolean functions, bubble-pushing, functional completeness, NAND/NOR-only circuit design. Optional Reading: B&V: Ch. 2.5-2.8
Oct. 13	Lab 1 continues [Lab # 1 Pre-lab due]	(Lecture 3) Muxes, half and full adder, Boolean cube, K-maps, maxterm and minterm expansions, don't cares. Optional Reading:	(Lecture 4) Propagation delay, timing diagram, critical path, Verilog for combinational logic; interface and implementation. Optional Reading:

		B&V: Ch.. 4.1-4.4, 4.8, 5.1-5.2, 6.1	B&V: Ch. 2.9-2.10, 4.12, 6.2-6.4 [HW # 1 due this Friday]
Oct. 20	Lab 1 check-out; Lab 2 check-in. (Lab 2: 4-bit Adder Design: Verilog, Simulation, download to FPGA.) [Lab # 2 Pre-lab due]	(Lecture 5) Basic latch, D latch and D flip-flop (behavioral); design of registers, shift registers and counters. Optional Reading: B&V: Ch. 7.1-7.4, 7.8-7.11	(Lecture 6) Timing diagrams of latches, flip-flops, shift registers, counters; T flip-flop, JK flip-flop, use of tristate buffers with memory elements. [HW # 2 due this Friday]
Oct. 27	Lab 2 check-out; Lab 3 check-in (Lab 3: Counter Design) [Lab # 3: No pre-lab due]	MIDTERM REVIEW	MIDTERM EXAM(in class)
Nov. 3	Lab 3 check-out Lab 4 check-in (Lab 4: Thunderbird FSM design; ModelSim simulation; download to FPGA; software/hardware interface for testing) [For Lab 4: Read the entire lab handout before coming to the lab.]	(Lecture 7) Map word problem to FSM; state diagram, state table, state assignment; Mealy/Moore machines. Optional Reading: B&V: Ch. 8.1-8.3	(Lecture 8) Timing diagrams for Mealy/Moore machines; map state diagram to flip-flop implementation. Optional Reading: B&V: Ch. 8.1-8.3
Nov. 10	Lab 4 continues [Lab 4: Part 1 is due]	(Lecture 9A) Verilog for sequential design; RTL and behavioral Verilog for FSMs. Optional Reading: B&V: Ch.8.4, Appendix A	(Lecture 9B) Examples of Mealy/Moore machines; mapping word problems to state diagrams.
Nov.	Lab 4 check-out;	(Lecture 11A)	(Lecture 11B)

17	Lab 5 check-in (Lab 5: General-purpose FSM; RAM-based design.) [Lab # 4 Check-out: Parts 2, 3 and 4 due] [For Lab 5: Read Ch 8.5 (Serial Adder) in textbook]	Timing of sequential circuits: set-up, hold times, propagation delays, minimum clock period Optional Reading: B&V: Ch 10.3.1-10.3.2	Examples of timing problems in sequential circuit design. [HW # 3 due this Friday]
Nov. 24	Lab 5 continues [Lab 5: Parts 1 and 2 due] (Note: for those whose lab sections are on Thursday, Parts 1 and Parts are due on Wednesday in the class)	(Lecture 13) CMOS technology: Combinational logic, and RAM (S-RAM, D-RAM)	(Lecture 14) 2's complement arithmetic, adder/subtractor, carry look-ahead adder. Optional Reading: B&V: Ch. 5.3-5.4 [HW # 4 due this Wednesday]
Dec. 1	Lab 5 Check-out: Parts 3 and 4 due.	(Lecture 15) Area-delay analysis of adders; solving problems.	(Lecture 16) Course evaluations; Review Session (for Final Exam) [HW # 5 due this Friday]

C. Graded Course Work and Rules:

C. 1. Laboratory Rules and Recommendations:

Rules:

The labs will be done in teams of two people. You may not have someone else outside the course or a member of another team in class do your lab (or sections of the lab) for you. It is fine to discuss, to get help from others in class as well as other students on debugging, but once you understand the problem, you (as a team) must go ahead and carry out the solution on your own.

Usually, we will not accept any late labs. Each lab's grading is divided into demonstrable milestones. Any milestones completed before the deadline, if demonstrated and are correct, will get full credit. For some labs, we may advertise a late policy of a few days. In that case, any milestone of the lab

that is late will get 50% of the credit that would be earned if that milestone had been completed on time.

There is usually a problem set due at the beginning of each lab. HAND IN A CLEAR PHOTOCOPY OF YOUR PROBLEM SET SOLUTIONS AT THE BEGINNING OF THE LAB. KEEP THE ACTUAL WRITE-UP FOR YOURSELF; YOU WILL BE USING THAT IN THE REST OF THE LAB.

If you burn a board that you have checked out from the ECE shop, you will be charged 1/2 of the cost of the board, in order to get a replacement. Follow the wiring guidelines for each lab.

Recommendations:
The strategy that we recommend for the labs is to start early and make as much progress as possible on your own as a team. Use the lab sessions very well: Ask the TA's the troubling points to remove any problems that are preventing your progress in the labs. Go to the TA's office hours held in the laboratory room for extra help. When you do the labs, try to understand fully why things are the way they are. The clarity of the top level design on any project is extremely important. Before you jump into implementation, make sure that you have understood the problem at the highest level of abstraction correctly and designed the top level solution with the tools at this level. If you have any doubts about the project specification, it is important to clear them as high up in the design abstraction chain as possible.

C. 2. Homework Rules and Recommendations:

Rules:
Homework is due in the HOMEWORK BOX on the 3rd floor of Harold Frank Hall, on the date and time shown for that homework on the course web page. Late homework gets a zero. The only exception to this is a well-documented, legitimate emergency.

You are allowed to collaborate with other students in this class on the homework assignments. You may not copy someone else's solutions, solutions from the instructor's manual or solutions from previous years. You may not have someone outside the course (e.g. a student who has taken the course before) do you homework for you. You may discuss the homework assignments and solution strategies with anyone, but the work you hand in must be your own write-up.

Recommendations:
The strategy that we recommend is to start the homework early and do as much of the homework as possible on your own. Then, get together with other students who have done the same to check your answers with each

other's, discuss the points on which you disagree, find correct solutions and then write up the corrected solution yourself.

C. 3. Exam Rules and Recommendations:

Rules:

The exam rules apply to all of the exams. At the end of the exam, we will tell you to stop writing and raise your exam booklet high. If you continue writing, we will deduct roughly 5% per minute from your exam score. Wait in your seat until we announce that ALL of the exams in the exam room have been collected.

If you finish your exam early, you may hand in your exam and then leave the exam room until 10 minutes before the exam is over. Once you hand in your exam, you may not get it back to make further changes. After we enter the last 10 minutes of the exam, even if you finish early, you need to wait in your seat for time to be called.

If you arrive late for an exam, you will not be given extra time at the end of the exam.

If you need any special accommodations for the exam room, you need to talk to me in advance and as soon as you become aware of such special needs.

You must write the exam on your own. Receiving or giving help during the exam is prohibited. All exams will be in class and will be closed book. You may not bring any devices to the exam on which equations can be stored or any wireless devices that can retrieve such data. On some exams, we may allow you to use calculators only for computational purposes.

If we cannot read your answer, we cannot give you any credit. If you have very bad handwriting, please see me at the beginning of the quarter.

If you do not show up for an exam, you receive a zero for that exam. The only exception to this rule is an emergency that is well-documented. As soon as you become aware of such an emergency, you need to contact me so that I can find a reasonable solution.

You must write your name on the sheet that contains the exam questions and hand in this sheet along with your exam. We will return the exam questions along with graded exams.

It is usually impossible to take the midterm or final exams earlier or later. However, in case of emergencies, we may give you an early or late exam. We cannot give guarantees on how much more difficult the make-up exam

will be and will not make adjustments to the score according to the level of difficulty of the make-up exam.

Recommendations:
The strategy that we recommend for the exams is (1) clear up your confusions way before the exam by going to the office hours of the professor and the TA's, (2) have a clear understanding of the digital design chain, i.e. how high-level abstractions are successively mapped down to low layers.

A common pitfall in studying for exams is to "go over" the lecture and homework material by flipping pages and recognizing correct solutions. This will usually not prepare you well for exams in this course. You need to take new problems (from your textbook, previous year's exams that we hand out, or from other textbooks or sources) and actively solve new problems. If you had difficulty with a homework problem, don't look at any solutions or textbooks; instead try solving the problem again from scratch and figure out where you are having difficulty.

The exams will cover all of the lecture notes, reading, laboratories and discussions that far. The final exam will be comprehensive. All of the exams are design-oriented. On exams, you will typically be given a word problem and asked to produce a design that solves the problem. It is very important to internalize the design process and get the system timing right on these problems. A superficial understanding of the material will not suffice.

D. Policy on Student Misconduct:

We will be vigilant to detect student misconduct and to investigate any reported cases. In this course, copying someone else's solutions, copying solutions from the instructor's manual, copying solutions from previous years' labs and student folders, using books in a closed-book exam, copying from someone else during an exam, are first-degree offenses. If we find any evidence of these or other offenses, we will refer the case immediately to the committee on student misconduct.