2 Hardware Notes

This chapter introduces you to the different components used in this labororatory to build digital systems.

2.1 Resistors

Each resistor is labeled with 3 or 4 color bands designating its resistance. This section explains the color code used to indicate the resistance value.

The first 3 bands specify the resistance value. Refer to table 2.1 (a) for the colors and their numeric value. The first two color bands indicate the first two significant digits of the resistance. The third band is a multiplier, i.e. it indicates the magnitude in powers of 10. The fourth band is called tolerance band and specifies the tolerance or precision of the indicated value.

color	value
black	0
brown	1
red	2
orange	3
yellow	4
green	5
blue	6
violet	7
gray	8
white	9

(a)

color	value
none	20%
silver	10%
none	5%

(b)

Table 2.1: Color code table: (a) Resistance value, (b) tolerance.

Here an example: an orange, red, brown, gold resistor has R=320 Ω with 5% tolerance. A yellow, violet, red, silver resistor is 4700 Ω (4.7 kΩ) with 10% tolerance.

2.2 Capacitors

Capacitors can be non-polarized or polarized devices. Usually, small capacitors like ceramic capacitors do not have polarity while larger electrolytic capacitors are polarized. Such capacitors will have the polarity marked — be sure to connect them properly. Improperly connected electrolytic capacitors could leak and release carcinogenic fumes.

Larger capacitors have the capacitance printed on the casing (in μF). Smaller mylar capacitors are labeled with a 3-digit number followed by a "K". Similar to resistors, the first two digits are the first two significant digits of the capacitance value. The third digit is a multiplier; it indicates the magnitude, i.e. how many zeros to add to the first two digits. The result is the capacitance in pF. For example, a capacitor labeled 104K is 10 0000 pF or 0.1 mF.

For ceramic capacitors, there is no standard fixed method of telling the capacitance. Usually, the number printed on the capacitor is the number in pF of capacitance.

2.3 Integrated Circuits

You will be using integrated circuits (ICs) in this laboratory to build the experiments. ICs come in different packages, but in the laboratory we will exclusively use the plastic dual in-line pin package (DIP).

In this class, you will use transistor-transistor logic (TTL) almost exclusively. Your chip numbers will be in the 74XXX range, e.g. 7400, 7404 etc. However, the label on the chip surface is a combination the manufacturer code, chip family and chip number, e.g. SN7400 or SN74LS00.

How do you determine the orientation, i.e. pin 1, on a DIP package? The text on the chip's surface is not always printed right side up. There are two common ways to mark pin 1:

- a little dimple on the package over pin 1.
- an indentation at one end of the chip. Pin 1 is the bottom left pin when the chip is oriented with this indentation to the left side. Pin numbers are counted counterclockwise from pin 1.

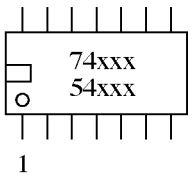


Figure 2.1: Location of pin 1 on a DIP chip.

Besides the inputs and outputs depending on the functionality, all integrated circuits have two pins for the supply voltage (V_{cc}) and ground (GND). Most chips adhere to the following convention:

- The last pin on the lower side (right bottom corner) is usually GND.
- The pin in the top left corner is usually V_{cc}, i.e. 5 V.

Before you use a chip, read the chip pinout and description. You can find the pinouts of the commonly used chips at the back of this manual, or refer to section 2.4 for online reference.

Some input pins (e.g. reset, enable) affect the overall functionality of a chip. **Even if you do not use these inputs, you will need to hardwire them to either "00" or"1", see section 2.6**. However, inputs not associated with the part of the chip that you are using (e.g. inputs to another inverter or AND gate on the same chip) can be left unconnected.

2.4 Data Sheets & Chip Manuals

Almost every workstation in the digilab should be equipped with a chip manual that contains functional descriptions and pinouts of the ICs that you will use in your circuits. However, during recent years some of them have been "lost".

The data sheets of the commonly used chips are included at the end of this manual. As an alternative, you can access specifications and descriptions online:

- **www.ti.com**: Products → Digital Logic → Product Tree,
  or directly at focus.ti.com/docs/logic/logichomepage.jhtml. In this laboratory we use transistor-transistor logic (TTL), so you will want to refer to your chips in that section. Over the years, Texas Instruments introduced advanced TTL logic families like the different Schottky logic families (S, LS, AS, ALS).
- The "Chip Directory" (Chipdir), an internet directory that contains pinouts for many old chips you cannot find on TI's web site. Two mirror sites are
  - www.xs4all.nl/~ganswijk/chipdir/
  - www.embeddedlinks.com/chipdir/

  If these are offline, you can search for another mirror with Google or any other major search engine.

2.5 TTL Logic Levels

Digital logic has two discrete values — "0" or "1". These digital values are represented by analog voltages, e.g. in TTL a "0" is 0 V and a "1" is 5 V. What about intermediate voltages, e.g. is 2.5 V a "0" or a "1"?

The TTL logic levels are defined as voltage ranges: an **input voltage** between 2.0 V and 5.0 V is considered to be a logic "1" and a voltage between 0 V and 0.8 V is considered a logic "0". Voltages between 0.8 V and 2.0 V are **not** defined and can either be a "0" or "1". The designer cannot accurately predict the chip's response to a voltage level in this range.

Output logic levels have the following voltage ranges: a "0" will fall between 0 V and 0.4 V (0.5 V for some chips) and a "1" will be in the range of 2.4 V – 5.0 V. Note that if you measure an intermediate output voltage like 0.7 V, there is something wrong in your circuit — even though this is a valid input voltage!

This situation arises most frequently when you have one of the following problems:

- **Missing ground connections**: you do not have one common ground for your whole circuit.
- **Bus contention**: several members on a common bus try to drive the bus to different logic levels.
- **Chip fanout**: Each output can only drive a limited number of inputs! As a rule of thumb, a TTL output can drive 8 TTL inputs.

2.6 Logic "0", "1" on TTL inputs

TTL chips have a relatively low input impedance. Therefore you cannot wire 5 V directly to an input, because you risk burning it out. To limit the current into a TTL chip, **tie the input high with a 4.7 kΩ pull-up resistor**.

When an input is not connected to anything (floating input), an interesting physical phenomenon occurs with TTL logic: you might expect the input to take on a low logic level — it does not. Unconnected TTL inputs usually float to a high logic level. However, **do not assume that this will be the case!** Unusual power loads on a TTL chip can cause an unconnected input to register as a logic low. **To assure a logic "0", tie the input to ground.**

2.7 Tri-State Outputs

When you connect several components on one common bus, only one component can drive the bus at any given time. Typically, a bus carries data between different devices in the system. Some devices on the bus can write (output) data and other devices can read that data. Suppose two devices are writing to the bus simultaneously, one with a "0" output and one with a "1" output. Effectively you have a shortcut in your circuit that will result in chips burning out. The voltage level on the bus will be some intermediate value that is neither high nor low, since the values tend to cancel each other out.

To avoid this situation, some chips come equipped with a special output characteristic know as "*HI-Z*" or "*tri-state*". In that state, a chip is not actively driving a voltage level onto the bus. Its output voltage takes on the level provided by another chip driving the bus.

Note that at most one device can be writing to the bus at any given time! However, it is possible that no device drives the bus, thus leaving the voltage level undefined.

2.8 Open-Collector Outputs

The output stage of a regular TTL chip is a transistor connected as inverting amplifier. If the input signal is "1", the transistor is on and the output signal voltage is approximately 0 V because of the voltage drop across the resistor (figure 2.2 (a)). If the input signal is

"0", the transistor is off and the output signal is around 5 V (actually a bit less due to internal losses).

An open-collector chip does not have the 5 kΩ collector resistor between 5 V and the transistor (figure 2.2 (b)). If the input is "1", the output goes to 0 V; but if the input is "0", the output has no internal voltage source to make the output voltage 5 V. An external 5 kΩ pull-up resistor is needed to connect the output to the 5 V voltage source (figure 2.3).

Why would we want to use this type of chip? Notice that if there are two open-collector circuits with a common pull-up resistor, then if either input signal is "1", the output goes low. We have just invented a NOR gate! This is a simple way of ANDing or ORing signals without adding another chip to the circuit. This technique is called a "wired-and" or "wired-or" gate.

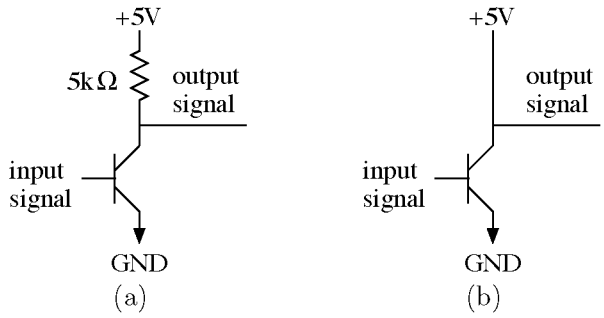


Figure 2.2: TTL outputs: (a) regular and (b) open-collector.

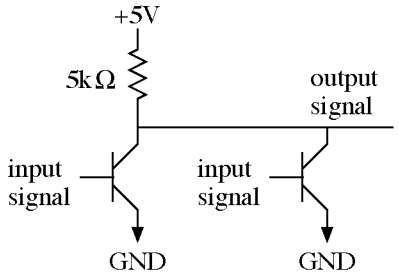


Figure 2.3: Common pull-up resistor on open-collector outputs.

2.9 Latches vs. Flip-Flops

A lot of confusion surrounds the terms "latch" and "flip-flop", especially since many textbooks use these words interchangeably.

A latch is an asynchronous, level-sensitive storage device that, when enabled, transparently passes the data on the input through to the output. When the enable is released, the input value is "latched", i.e. the chip outputs holds on to the last value no matter what appears on the input.

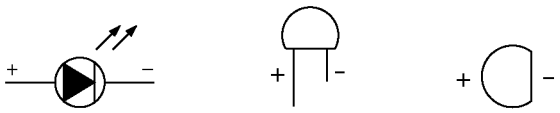
Contrary to the latch, a flip-flop is a synchronous, edge-sensitive device. The data at the input is only passed to the output at the rising edge of the enable (referred to as clock for flip-flops). A flip-flop can be made from two cascaded latches with the second latch enable being the inverted clock.

Flip-flops are commonly used in designs that require data to flow in a synchronized manner through the system, e.g. in a state machine. The flow of data is precisely synchronized to a common clock.

2.10 LEDs

Light emitting diodes (LEDs) can be used in digital systems to indicate logic levels. The basic idea is that one side of the LED is connected to power and the other side is connected to a driver. However, with LEDs there are a few things you need to remember. First, LEDs are diodes and therefore have voltage polarity, i.e. they only work one way in the circuit. If they are put in backwards, they will not work.

Figure 2.4 (a) shows the schematic symbol for an LED. The arrow in the center of the diagram points in the direction of positive current flow, or from larger positive voltage toward a lower voltage. Unfortunately, LEDs do not have this arrow marked on them. On new LEDs, the shorter lead is the negative lead (figure 2.4 (b)). Be careful with this identification though — the leads could have been clipped short and may not properly indicate the negative lead. If you examine an LED closely, you will find that it has a slightly flat edge near one of the leads. This edge indicates the negative side of the LED.



(a) (b) (c)

Figure 2.4: Light emitting diode (LED): (a) schematic symbol; (b), (c) polarity identification.

Another important thing about LEDs is that they can only sustain a limited current — about 30 mA. If the LED draws more than 30 mA, it will burn out and cease to function. Also, LEDs drop a specific voltage when lit — about 1 V. If you put a bare LED into a 5 V circuit, it is going to draw a lot of current and burn out. Therefore you need to limit the current using a series resistor.

The value of this resistor can be determined with the equation $V = RI$. The LED drops 1 V, so the resistor must drop 4 V. We can allow 30 mA, so we need a 133 Ω resistor. In this lab, we will use **330 Ω resistors** for an added safety margin.

When using LEDs to display data, be sure to use drivers. Below are three appropriate techniques to buffer an LED. Figure 2.5 (a) shows the setup for active high signals: the inverter inverts a high signal — making it low — and completes the path to light the LED. Note that the chip acts as a ground connection for the LED. With an active low signal use figure 2.5 (b). Figure 2.5 (c) shows

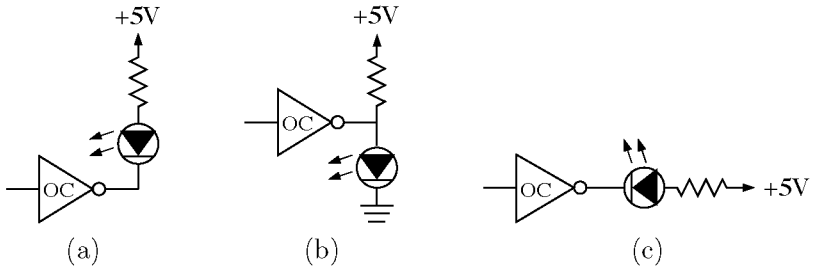


Figure 2.5: Driving an LED with an inverter. Open-collector inverters (e.g. 7405): (a) series switching, (b) shunt switching. Regular inverter (e.g. 7404) setup (c).

2.11 7-Segment Displays

Seven-segment displays consist of 7 LEDs in a package arranged in a special pattern. Lighting various LEDs allows different numbers to be displayed. Each LED can be controlled individually, but typically a BCD to 7-segment decoder/driver is used.

There are two display types: common-anode and common-cathode. Common-anode displays should be driven by the active-low outputs of the 7446 or 7447 decoders; they have identical pinouts, so you can interchange them. The 7448 and 7449 drivers feature active-high outputs for driving common-cathode LEDs. Pins 13 and 14 should be connected to the supply voltage V_{cc} for the common anode display and connected to ground for the common cathode display.

Do not forget 330 Ω limiting resistors in series with all LED segments!

2.12 Schmitt Trigger

The Schmitt Trigger (schematic symbol figure 2.7 (a)) is an ordinary gate with a small amount of internal feedback. It is not yet a flip-flop but has some flip-flop characteristics superimposed on normal gate behavior.

Figure 2.7 (b) depicts the voltage behavior of a Schmitt trigger. For $V_{in} = 0$ V, the output is high as in a normal inverter (point A). As V_{in} is increased from 0 V towards Y V, at Y V the output suddenly switches to a low value (point B→C). The output remains low as long as V_{in} stays above X V (points D, E). When it reaches the lower voltage threshold X V, V_{out} switches to a high value (point F).

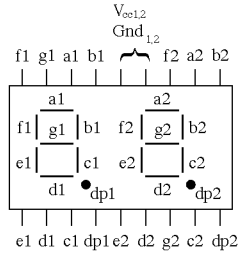


Figure 2.6: Pinout of the 7-segment LED display. Pins 13, 14 are $V_{cc1,2}$ for common anode and $Gnd_{1,2}$ for common cathode displays.

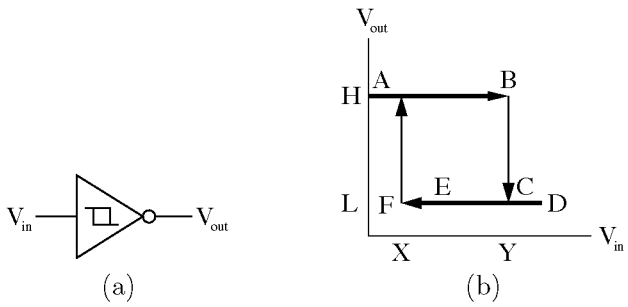


Figure 2.7: Schmitt trigger: (a) logic symbol and (b) voltage hysteresis behavior.

This behavior is called hysteresis and is measured by the difference between the X and Y voltages. The Schmitt trigger circuit symbol is a standard gate symbol with a hysteresis curve drawn inside the gate symbol (figure 2.7 (a)). For a TTL Schmitt trigger, typical values for X and Y are X = 0.8 V and Y = 1.6 V.

The Schmitt Trigger is extremely useful for waveform smoothing and noise removal in digital systems. Consider the noisy waveform in figure 2.8. V_{in} must rise to Y V before the Schmitt trigger will switch. The hysteresis rejects the noise fluctuations in the signal and a clean switch occurs in the output V_{out}.

2.13 Schmitt Trigger Oscillator

A 7414 Schmitt trigger can be used in conjunction with a single resistor and capacitor to build a simple astable multivibrator as shown in figure 2.9 (a).

The capacitor C continually charges and discharges between the hysteresis points. When the capacitor charges to the upper threshold, the output will switch to low. This will discharge the capacitor until the lower threshold is reached, which causes the output to go high. The cycle repeats indefinitely.

The resistor R_1 in must not draw excessive current from the output and its value

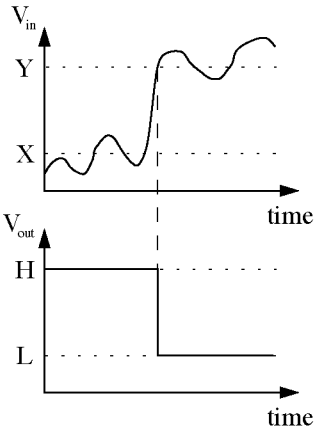


Figure 2.8: Noise removal with a Schmitt trigger.

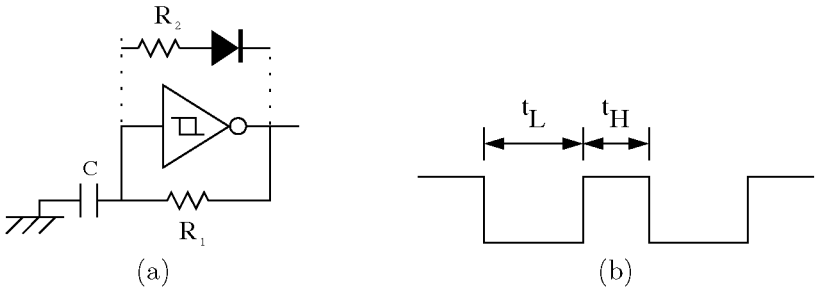


Figure 2.9: Astable multivibrator using a 7414 Schmitt trigger: (a) hardware setup, (b) output waveform.

must be high enough to prevent loading of subsequent stages. A resistance of $R_1 = 390\,\Omega$ provides a fan-out of two. With that resistance value, the expressions for output pulse width (figure 2.9 (b)) are as follows:

$$t_H = 0.14C \qquad t_L = 0.34C$$

t_L, t_H are the time durations when the output is low respectively high. The frequency of the astable is

$$f = (2.02 * 10^{-3})/C,$$

Note that there is no general frequency equation as a function of R_1 and C because the internals of the 7414 must be considered. As indicated by the expressions for t_L and t_H, the output of the astable is low approximately 70% of the time. A duty cycle of

about 50% can be obtained by adding a second resistor R_1 and a diode as indicated by the dashed lines in figure 2.9 (b).

With $R_1 = 390\,\Omega$ and $R_2 = 140\,\Omega$, the output frequency becomes

$$f = (3.3 * 10^{-3})/C,$$

2.14 Breadboarding: Wiring Guidelines

You will build your circuit on a solderless breadboard. You can directly plug your chips into the breadboard; internal connections allow you do interface to the chips. In addition, busses are available to distribute the power supply voltage and ground around the breadboard.

Some practical suggestions for using the breadboard are given below:

1. **Chip orientation**: orient all chips in the same direction. It makes it easy to glance over the whole board and identify correct pin numbers.
2. **Breadboard +5 V and ground**. The breadboard comes with designated busses for +5 V and ground, marked red and blue. Wire all these busses together and connect them to the power supply.
3. **Chip +5 V and ground connections**: wire those connections on each IC first. Take them from the nearest dedicated breadboard bus. Improper connections are the cause of many circuit malfunctions. If a circuit does not operate correctly, think about first checking the power supply connections. Do this by measuring, not by sight! Sometimes it's as simple as a broken or not completely connected wire
4. **Color coding**: use color coded wires to help indicate the function. As a minimum, use red for +5 V and black or blue for ground connections. Mark busses with one color and common control signals with another etc.
5. **Spacing**: when an IC is placed on the breadboard, there are a few remaining holes for wire connections on each pin. Keeping the two holes immediately next to the IC empty keeps your design visibly structured and organized. It also helps understanding more complicated designs because you can better read the signal flow or measure it with the oscilloscope. In addition, it becomes easier to replace faulty ICs without having to remove any wires.
6. **Floating inputs**: an unconnected TTL input usually floats high to a positive logic-1 condition, but do not count on it. Inputs are susceptible to noise and ringing. Therefore, all unused inputs should be tied to their respective level (see section 2.6.
7. **Wires**: One common problem is that the wires do not actually make "electrical contact" with the socket even though they may visually seem to. Insert the wires deeply into the sockets!