```
module testbench;
   //vars
   reg dimclock, lights, clock, left,right,brake,reset, hazards;
   wire [5:0] tail_lights;

   initial begin
       clock<=0;
       dimclock<=0;
       lights<=0;
       left<=0;
       right<=0;
       hazards <= 0;
       brake<=0;
       #20 reset<=1;               // L->left, R->right, B->brake, H->hazards
       #11 reset<=0;               // LRBH = 4'b0000
       #10 left<=1;                // LRBH = 4'b1000, left turn without brake
       #50 left<=0; right<=1;      // LRBH = 4'b0100, right turn without brake
       #50 hazards <=1;            // LRBH = 4'b0101, hazards overwrites right turn
       #50 hazards <= 0;           // LRBH = 4'b0100
       #10 brake<=1;               // LRBH = 4'b0110, right turn + brake
       #50 left<=0; right <=0;     // LRBH = 4'b0010, only brake
       #50 left <= 1;              // LRBH = 4'b1010, left turn + brake
       #50 hazards <= 1;           // LRBH = 4'b1011, (left turn + brake) overwrites hazards
       #20 left<=0;                // LRBH = 4'b0011, brake overwrites hazards
       #50 brake<= 0; hazards<=0; left<=1; right<=1; // LRBH = 4'b1100, hazards with left and ri
       #50 reset <=1;               // test reset
       #10 lights<=1;               // test lights.
       #50 lights<=0;

   end

   always begin
       #5 clock<= !clock;
   end
   always begin
       #1 dimclock <= !dimclock;
   end

   thunderbird exp(dimclock, lights, tail_lights, clock, left, right, brake, hazards, reset);

endmodule
```