

EXAMPLE FINAL EXAM

INSTRUCTIONS

1. This exam is **open** book and **open** notes.
2. It consists of 4 problems and is worth a maximum of 100 points. The problems are not of equal difficulty, so use discretion in allocating your time. Answer all questions in any order.
3. Show your answers in the spaces and additional pages provided, and use the back side of the exam pages if you need additional work space. **Show your reasoning and the essential steps clearly and concisely.**

Last Name, First Name: _____

1. MULTIPLEXERS AND DECODERS (25 points)

Consider the following function:

$$f(x_1, x_2, x_3, x_4) = \sum m(0, 4, 6, 7, 8, 11, 12, 14, 15) \quad (1)$$

- (a) Find the minimum sum-of-products (SOP) implementation for f using a Karnaugh map.
- (b) Use Shannon's expansion theorem to rewrite the result in part (a) by expanding it in terms of x_3 . Sketch a circuit diagram that implements f using a 2:1 multiplexer.
- (c) Starting with the result in part (b), use Shannon's expansion theorem to further expand f in terms of x_4 . Sketch a circuit diagram that implements f using a 4:1 multiplexer.
- (d) Show how to implement a 4:16 decoder with inputs $\{x_1, x_2, x_3, x_4\}$ using two 3:8 decoders. Then, use this decoder along with six two-input OR gates and one three-input OR gate to implement f in part (a).

Solution:

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2. STATE MINIMIZATION AND MACHINE CONVERSION (30 points)

Consider the following next-state table for a Mealy machine with input x and output z :

present state	$x = 0$	$x = 1$
A	$E, 0$	$D, 0$
B	$A, 1$	$F, 0$
C	$C, 0$	$A, 1$
D	$B, 0$	$A, 0$
E	$D, 1$	$C, 0$
F	$C, 0$	$D, 1$
G	$H, 1$	$G, 1$
H	$C, 1$	$B, 1$

- (a) Use partitioning to generate a reduced state machine. (Hint: The minimal Mealy machine has five states. Use $\{A', B', C', D', E'\}$ to label the reduced set of states.)
- (b) Use an implication table to obtain the same set of reduced states. Clearly indicate your steps. Give the state table for the reduced Mealy machine.
- (c) Convert the reduced Mealy machine to the corresponding Moore machine. When you split a state into two states, label them numerically, for example, $B' \rightarrow \{B1', B2'\}$. Sketch the Moore state diagram. (Hint: The minimal Moore machine has eight states.)

Solution:

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3. SEQUENCE DETECTOR (30 points)

Design a finite-state machine (FSM) with input x and output y that can recognize a sequence of four ones. It should be capable of recognizing overlapping patterns of four ones; thus, for input 01011111010, the output of the machine is 000000111000.

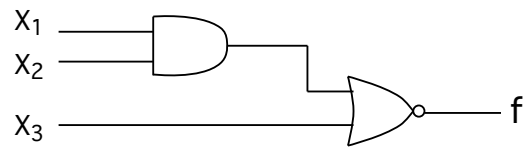
- (a) Sketch a Moore state diagram for this FSM and construct the corresponding state table. (Hint: There are five states in a minimal realization.)
- (b) Convert the Moore state table to a Mealy state table, and reduce the number of states to four using row matching. Sketch the corresponding Mealy state diagram.
- (c) Using consecutive bits for the state assignment (i.e., 00, 01, 10, 11), derive the logic for generating the next state and the output from the present state and the input. Use Q_1 and Q_2 to denote the most-significant bit and least-significant bit, respectively, of the present state.
- (d) Implement the Mealy sequence detector using JK flip-flops and sketch the circuit.

Solution:

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4. CMOS AND VERILOG (15 points)

Consider the following circuit:



- (a) Sketch a CMOS circuit implementation of this function using a pull-up/pull-down network.
- (b) Using an **always** block and **case** statements, write a Verilog module that implements this circuit.

Solution:

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