Department of Electrical & Computer Engineering
University of California, Santa Barbara

ECE 152A
Summer 2011
Shynk
H.O. #10

# EXAMPLE MIDTERM EXAM

## INSTRUCTIONS

1. This exam is **open book and open notes**.
2. It consists of 4 problems and is worth a maximum of 100 points. The problems are not of equal difficulty, so use discretion in allocating your time. Answer all questions in any order.
3. Show your answers in the spaces and additional pages provided, and use the back side of the exam pages if you need additional work space. **Show your reasoning and the essential steps clearly and concisely.**

**Last Name, First Name:** _____

## 1. COMBINATIONAL CIRCUIT (30 points)

Consider the following function:

$$f(A, B, C, D) = \sum m(0, 1, 2, 7, 8, 9, 10, 15) \tag{1}$$

**(a)** Find the minimum sum-of-products (SOP) implementation for $f$ using a Karnaugh map. Specify (i) the number of implicants, (ii) the number of prime implicants, and (iii) the number of essential prime implicants. Determine if the minimum cover you obtain is unique.

**(b)** Using the same Karnaugh map, (i) express the function $f$ using the product-of-sums (POS) notation $\prod M(\cdot)$, (ii) find the minimum POS implementation, and (iii) use Boolean algebra to verify that your result is equivalent to that derived in part (a).

**(c)** Sketch a pull-up/pull-down CMOS circuit that implements $f$. Assume that inverters have already generated the voltages for the complemented inputs. (Hint: the minimum number of transistors is 12.)

**Solution:**

**2. HALF ADDER (30 points)**

Suppose we want to design a logic circuit to implement a half adder for ternary numbers, i.e., with values $\{0, 1, 2\}$. Let $A$ and $B$ represent the two ternary numbers to be added. Since there are three levels, two bits are needed; thus, define $A = a_1a_0$ and $B = b_1b_0$. Let $S$ be the sum of $A$ and $B$, and since it also can take on three values, define $S = s_1s_0$. The carry $C$ can take on only two values, $\{0, 1\}$, so it requires only one bit.

**(a)** Complete the following table for ternary addition (specify the remaining five rows to the right of the table):

| $AB$ | $S$ | $C$ |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 1 | 1 |
| 02 | 2 | 0 |
| 10 | 1 | 0 |
| etc. | | |

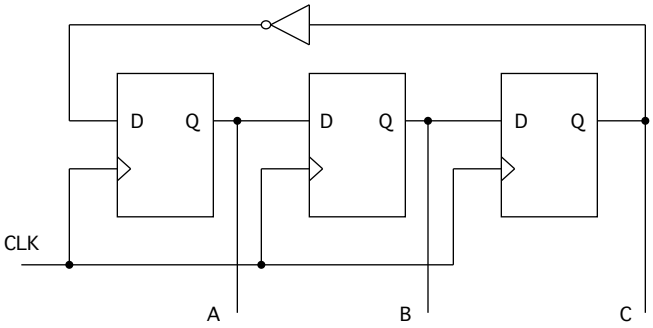
**(b)** Use the following mapping between ternary and binary numbers: $(0)_3 \rightarrow (00)_2$, $(1)_3 \rightarrow (01)_2$, $(2)_3 \rightarrow (10)_2$. With these definitions and your table in part (a), find a minimum sum-of-products (SOP) implementation for generating the carry bit $C$ and the two bits of the sum $S = s_1s_0$. (Hints: You will need three maps, each with four input variables $a_1, a_0, b_1, b_0$. Exploit the fact that $(11)_2$ cannot occur.)

**(c)** Using gate level primitives, write a module in Verilog to implement this half-adder. Determine if there are any terms common to the expressions for $S$ and $C$, resulting in primitives that can be shared.

**Solution:**

**3. FINITE STATE MACHINE (30 points)**

Consider the following finite-state machine (FSM):




**(a)** Assuming that the circuit is in the initial state $ABC = 000$, sketch a state diagram, and then provide the state table for this FSM. Find expressions for the next states $A^+$, $B^+$, and $C^+$ from Karnaugh maps.

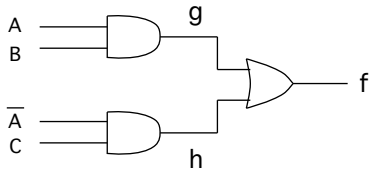
**(b)** Suppose now that we want to use T-type flip-flops instead of the D-type flip-flops. Find expressions for the inputs $T_A$, $T_B$, and $T_C$.

**(c)** Sketch a circuit for your result in part (b). (You may use logic gates other than AND and OR for a simpler implementation.)

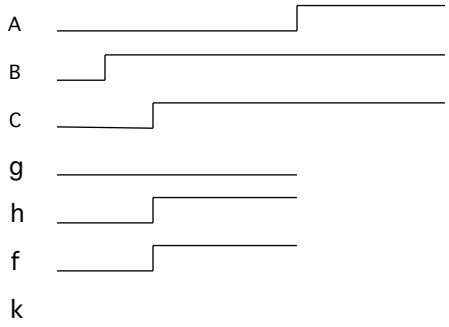
**Solution:**

**3. PROPAGATION DELAY (10 points)**

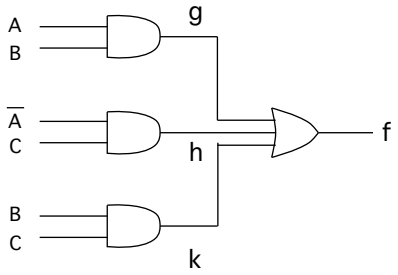
In this circuit, assume that $f$ and $h$ change instantaneously, but $g$ has a small propagation delay.




**(a)** Complete the following timing diagram, demonstrating that the delay causes the output to behave in an unexpected manner.




**(b)** The following circuit prevents the unexpected behavior. Show this by sketching $k$ on the timing diagram. Assume that $k$ changes instantaneously.




**(c)** Verify that this circuit is logically identical to the first circuit.

**Solution:**