Name:____
Perm #:_______________________________________

Lab Section TA:_________________________________

ECE 152A-Fall 2004

Prof. Volkan Rodoplu

MIDTERM EXAMINATION

INSTRUCTIONS:

1. READ THIS PAGE THOROUGHLY WHEN YOU RECEIVE IT, BUT DO NOT START TURNING TO THE OTHER PAGES UNTIL YOU ARE INSTRUCTED TO DO SO.

2. WHENEVER INDICATED, YOU MUST WRITE YOUR ANSWERS ON THE ANSWER LINES PROVIDED IN CERTAIN PROBLEMS. NO PARTIAL CREDIT WILL BE GIVEN ON THESE PROBLEMS. (We will check only the answer on that line.)

3. On other problems, PARTIAL CREDIT will be given only to true statements that make progress towards the correct answer. Partial credit may be given to correct reasoning in developing structures such as K-maps and truth tables in which the variables are clearly labeled. NO partial credit will be given for incorrect statements or statements to which no truth value can be assigned (such as a bunch of numbers or algebraic expressions). NO partial credit will be given for statements that use symbols that the problem statement or you have not defined. NO credit will be given for any work that is not clearly labeled with the part and problem number to which this work provides an answer.

4. All the exam rules in the course syllabus apply to this exam.

5. You may remove the staple from the exam pages, if is more convenient. We will provide a stapler at the end of the exam.

6. There are 12 pages in this exam. When you are instructed to start, first check that you have all the pages.

7. There is a total of 90 points on this exam.

8. You may use the back of the pages for extra work. However, these will be graded only if you clearly indicate so AND label it with the part and problem number.

PROBLEMS:

Problem # 1 [35 points]

The circuit shown in Figure 1 is called a "2-input permutation network". It has three 1-bit inputs a, b, c and two 1-bit outputs x and y. The inputs a and b are referred to as "data inputs" and c is called a "control input". This circuit is capable of producing all possible permutations of the data inputs as outputs. The desired permutation is specified by the control input. If c = 0, then x = a and y = b, and if c =1 then x = b and y = a.

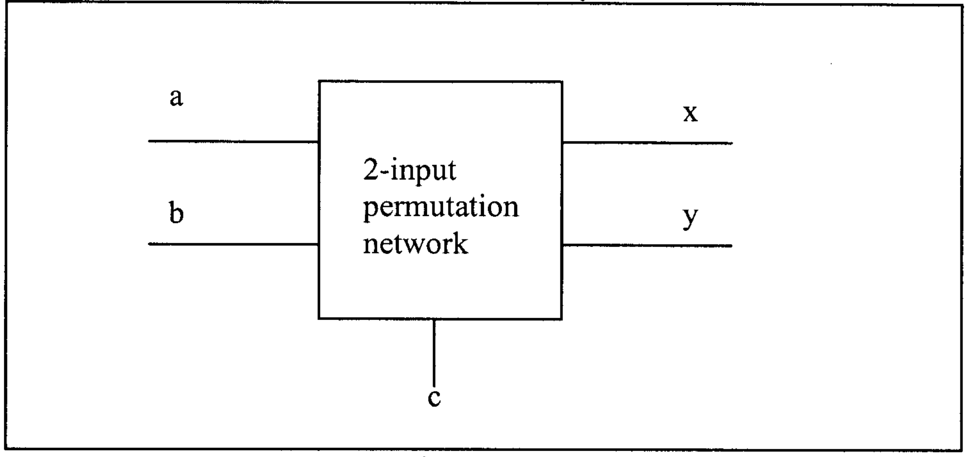


Figure 1

Each part of this problem may introduce some additional assumptions. The additional assumptions of each part are to be used only for that part. Do NOT carry the additional assumptions of one part into the other parts of the problem.

(a) **(4 points)** Write down algebraic expressions for x and y in terms of the input variables. **(Your answer must be written on the following lines!)**

x = ____

y = ____

(b) **(4 points)** Draw the K-maps for x and y.

(c) **(4 points)** For only the output variable x, write down algebraic expressions for each prime implicant and say which of these expressions are essential prime implicants.

(d) **(8 points)** Give a minimum sum-of-products (SOP) and a minimum product-of-sums (POS) expression for each of the outputs x and y.

Minimum SOP:

x = ______________________________

y = ______________________________

Minimum POS:

x = ______________________________

y = ______________________________

(You may do any extra work in the following space:)

(e) **(5 points)** By drawing the schematic, implement the 2-by-2 permutation network using only NOR gates.

(f) **(5 points)** By drawing the schematic, implement the 2-by-2 permutation network using only tri-state buffers.

(g) **(5 points)** Implement the 2-by-2 permutation network as a Verilog module, **using only continuous assignments**.

Problem # 2 [38 points]:

We want to implement a **synchronous** counter that counts in the sequence 2, 1, 0, 2, 1, 0, … unless its Reset input is asserted. If Reset is asserted, then the counter **sets to its output to the value of 2** and then starts counting down again.

The only inputs to the counter are Reset and a clock input.

We will implement the counter as a **Moore machine**.

(a) **(1 point)** Draw the interface schematic for this counter.

(b) **(8 points)** Draw the state diagram for this counter. (All transition arrows must be shown and marked completely.)

(c) **(8 points)** Write down the state table that corresponds to your state diagram from Part (b).

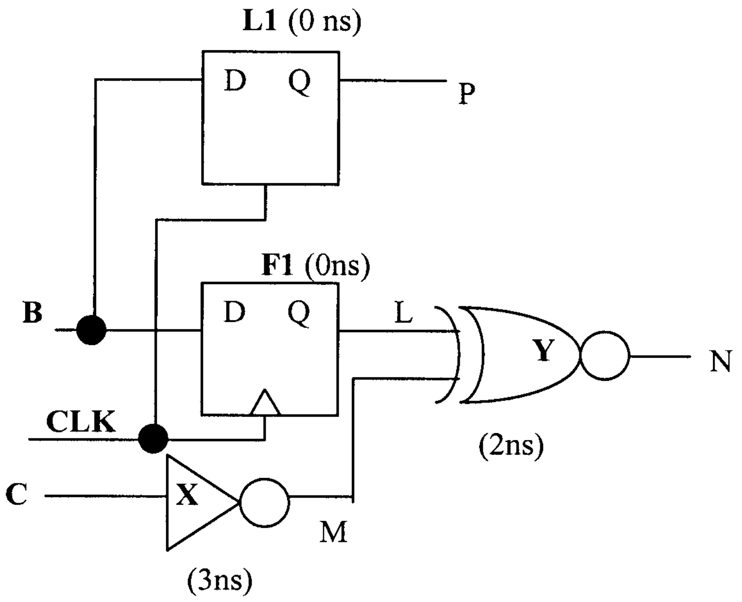
(d) **(8 points)** Write down the next-state and output equations in minimum SOP form by using K-map minimization.

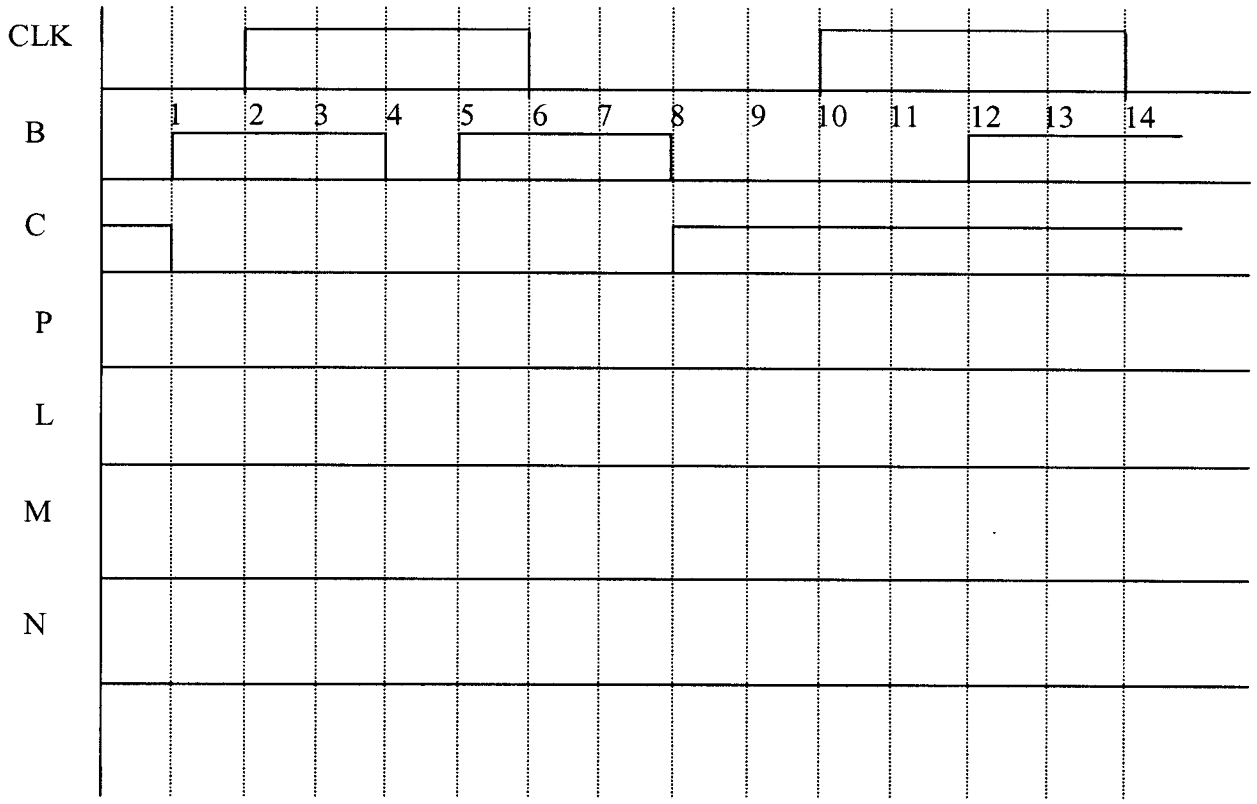
(e) **(6 points)** Implement this counter using only D flip-flops. (Draw the schematic.)

(f) **(7 points)** We would like to re-design this counter such that the **Reset input is eliminated** and the counter is instead "self-starting". This means the following: When the counter powers up, if it finds itself in the state corresponding to a count of 3 (which is not part of the allowed sequence), the counter is "smart enough" to find a way to get into the correct sequence 2, 1, 0, 2, 1, 0, ... (after a small number of clock pulses). This should happen without the addition of any extra inputs.

Give the **interface schematic** AND **the state diagram** of this self-starting synchronous counter. Use a **Moore machine** implementation. (Note: DO NOT map this to flip-flops! We are NOT asking for an implementation schematic.)

Problem # 3 [17 points]:
The circuit for this problem is given below. **See the next page for the problem statement.**





In this circuit, L1 is a positive level-sensitive D latch. F1 is positive edge-triggered D flip-flop. CLK is the clock input signal. B and C are data input signals. L, M, N, and P are nodes in the circuit.

The delay of the inverter X is 3 ns, and the delay of the XNOR gate Y is 2 ns.

The propagation delays of latch L1 and flip-flop F1 are negligible (0 ns).

(Large black dots indicate wire connections. No large black dot means there is no connection between crossing wires.)

External wires have negligible (i.e. zero) delay.

Assume that the data inputs B and C have been stable for a very long time at B = 0 and C = 1, before time t = 0.)

Complete the timing diagram **that appears beneath the circuit on the previous page**. The waveforms for the inputs B, C and CLK are given. Fill in the waveforms for P, L, M and N.

-----------------------END OF EXAM---