ECE 152A - Quick Guide for Setting Up Quartus II

This tutorial was adapted from the UCSB DigiLab FPGA Board website for use with ECE 152A. For more detailed information please refer to the website:
http://vader.ece.ucsb.edu/digilab-fpga/

1. Start a New Project

- Select File > New Project Wizard. Press Next to get the window shown in Figure 1.

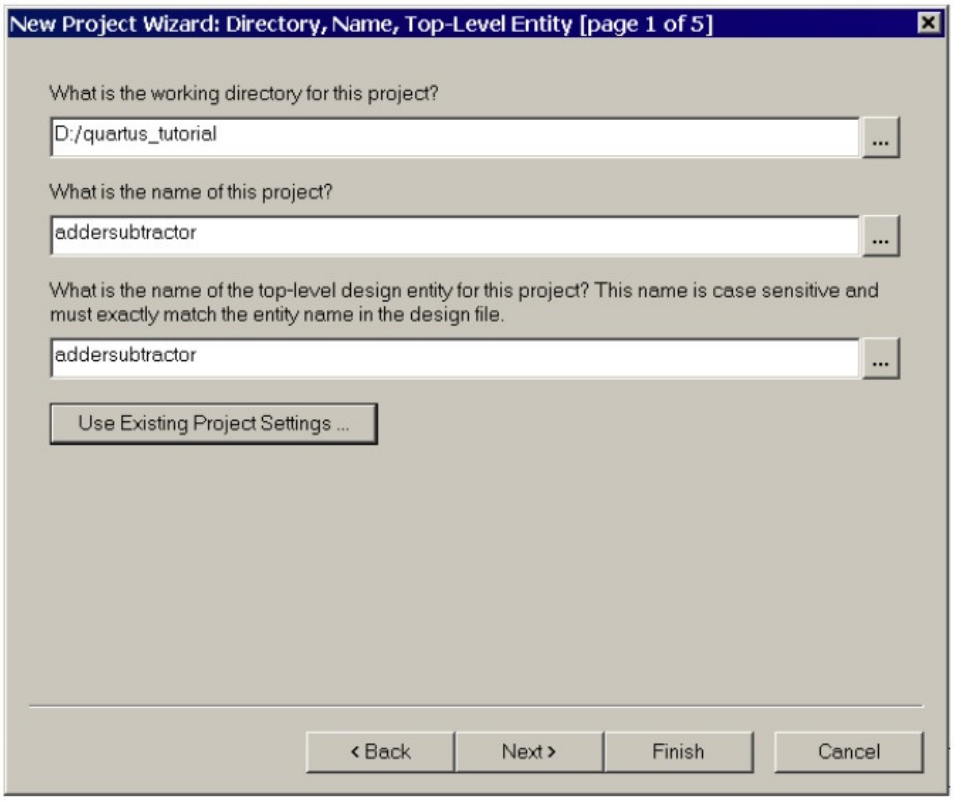


Figure 1: New Project Wizard Screen

- Set the working directory to be on your personal network drive.
- The project must be named the same as the top-level design entity that will be included in the project.
- Select FINISH. This will create your new project.

2. Specify Device and Pin Options

- Select Assignments > Device.
- Choose the options and device shown in Figure 2.
- Click on the "Device & Pin Options" button. See Figure 3 on the next page.

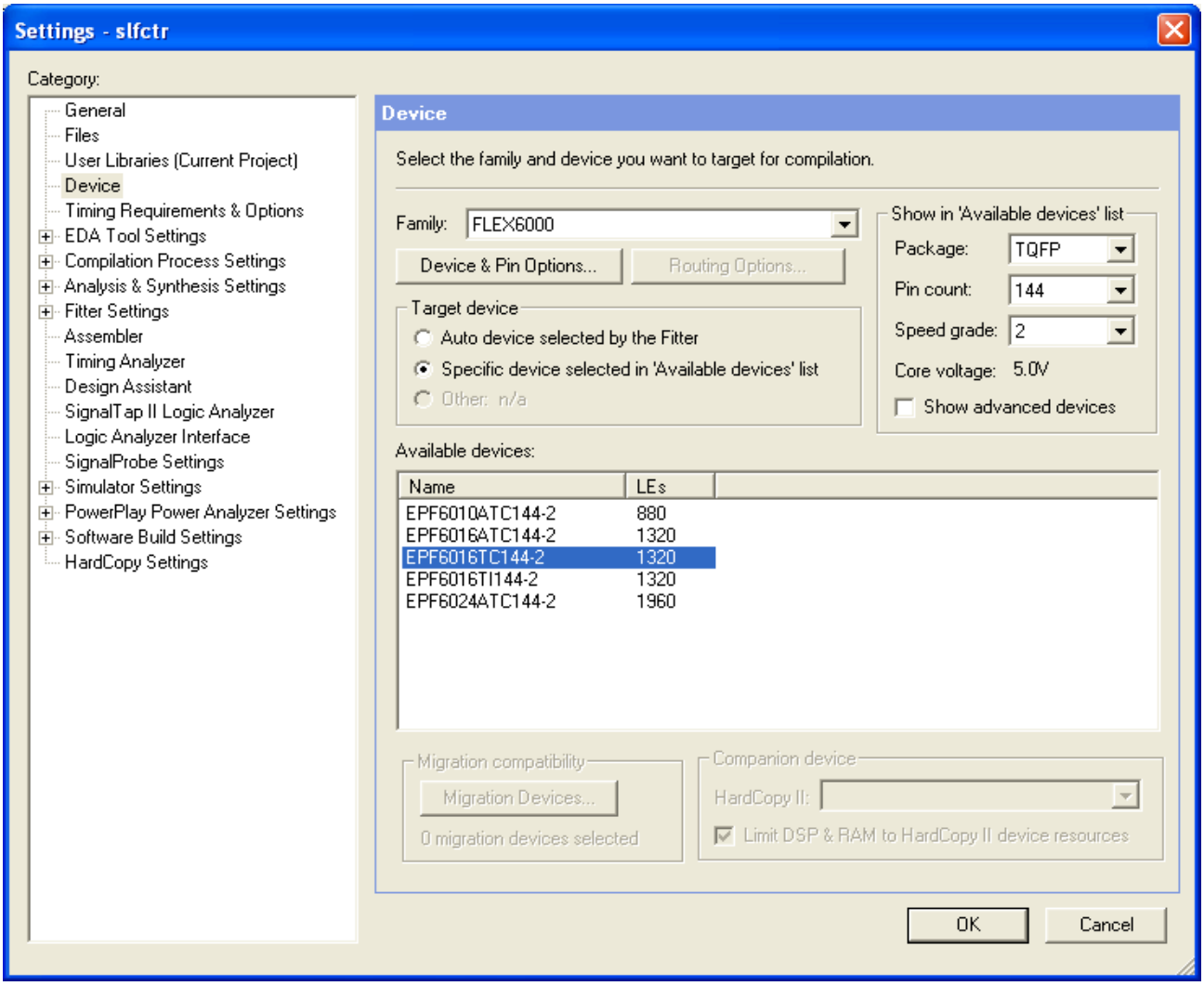


Figure 2: Device Assignment Screen

- Under the General tab, select "Enable JTAG-BST Support" as shown below in Figure 3.
- Under the Configuration tab, select Passive Serial for the Configuration Scheme. Be sure to leave the Use configuration device option unselected.
- Under the Programming Files tab, select Raw Binary File (.rbf) for the file format. Leave all other programming file format options unselected.
- Under the Unused Pins tab, select "As input tristated" for the behavior of all unused pins.

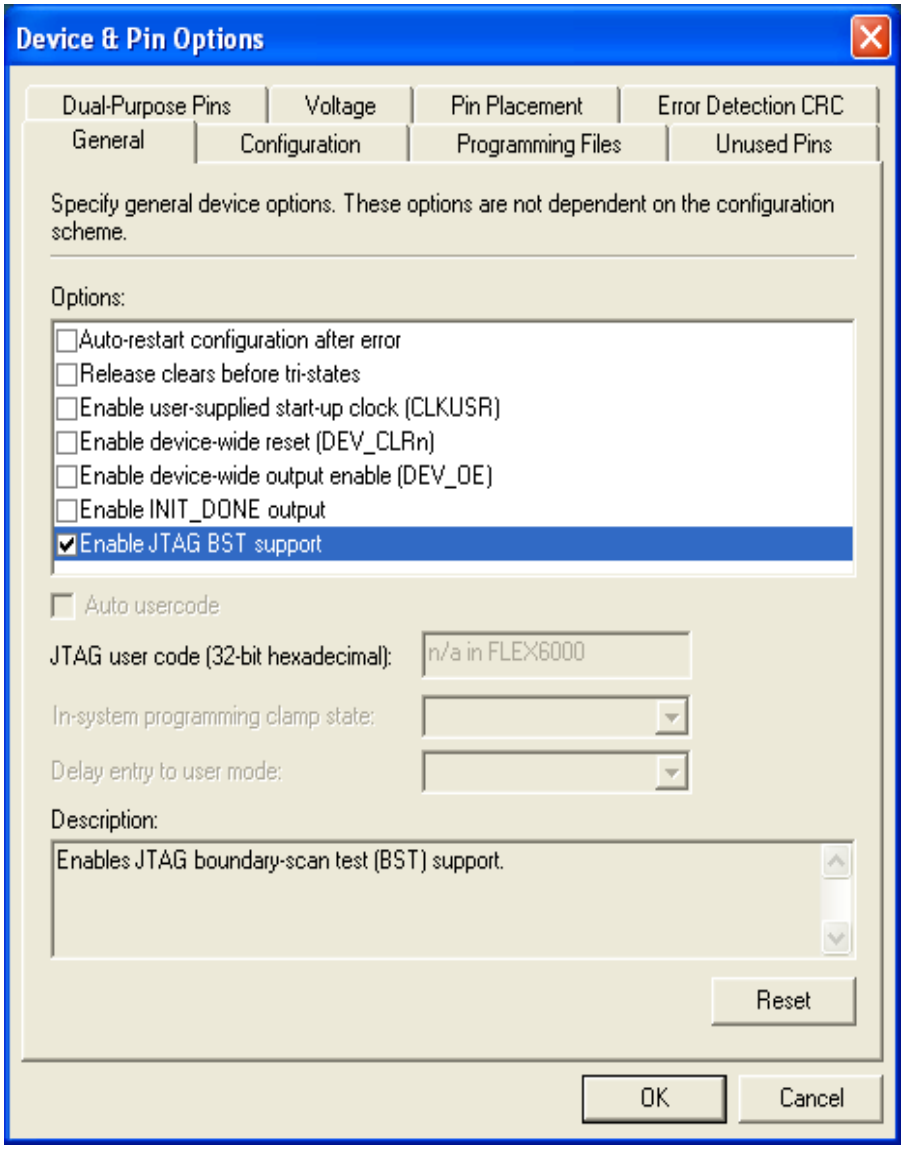


Figure 3 – Device and Pin Options Screen

- Select OK to close the Device and Pin Options Screen
- Select OK to close the Device Assignment Screen

3. Add the Verilog file to the project

Note: You need to ensure that the Verilog file name is the same name as your project and module.

- Select Project > Add/Remove Files in Project.
- Add your Verilog file to the project and click OK.

4. Set Top Level Entry

- In the Project Navigator window, click on the “Files” tab on the bottom. Your added Verilog file should be included now in the Device Design Files folder. See Figure 4.
- Right-click on the file added and choose "Set – as top level entry"

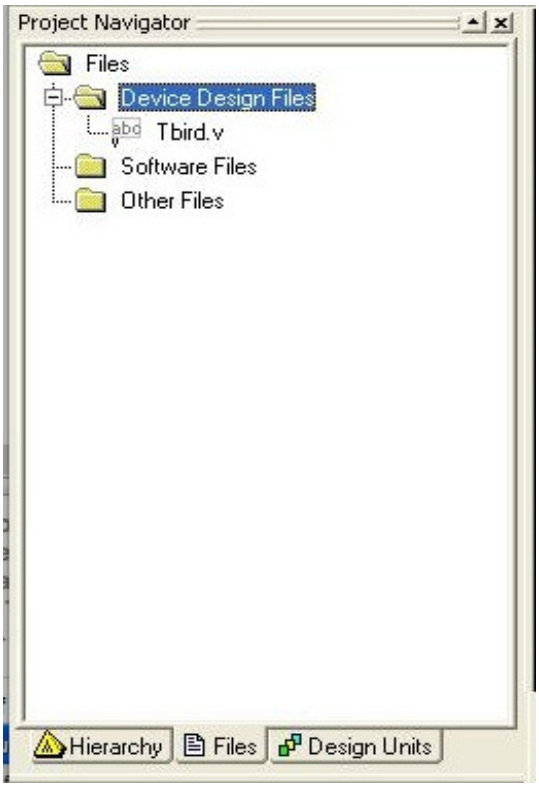


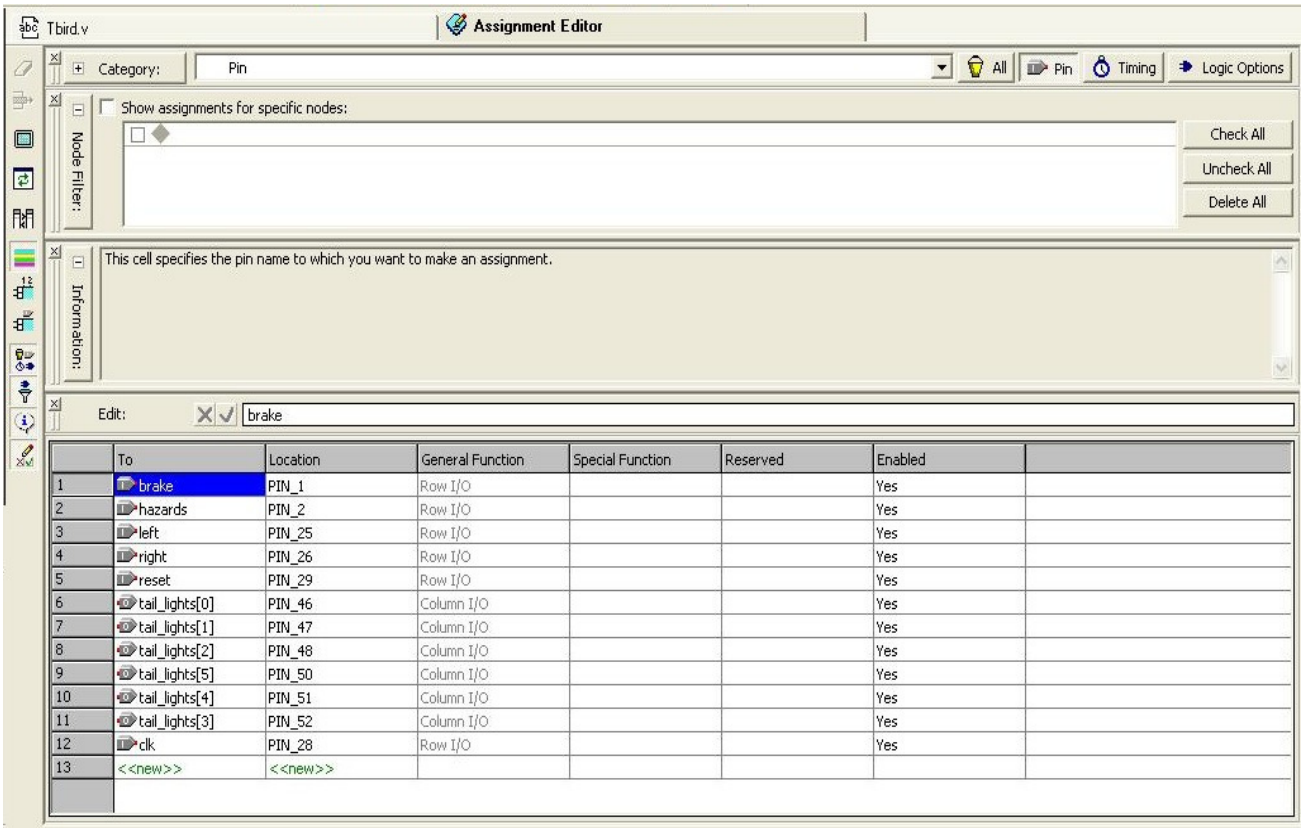
Figure 4 – Project Navigator Window

5. Compile Project

- Select Processing > Start Compilation

6. Assign Pins

- After compilation is successful, Select Assignments > Pins. See Figure 5.



	To	Location	General Function	Special Function	Reserved	Enabled	
1	brake	PIN_1	Row I/O			Yes	
2	hazards	PIN_2	Row I/O			Yes	
3	left	PIN_25	Row I/O			Yes	
4	right	PIN_26	Row I/O			Yes	
5	reset	PIN_29	Row I/O			Yes	
6	tail_lights[0]	PIN_46	Column I/O			Yes	
7	tail_lights[1]	PIN_47	Column I/O			Yes	
8	tail_lights[2]	PIN_48	Column I/O			Yes	
9	tail_lights[5]	PIN_50	Column I/O			Yes	
10	tail_lights[4]	PIN_51	Column I/O			Yes	
11	tail_lights[3]	PIN_52	Column I/O			Yes	
12	clk	PIN_28	Row I/O			Yes	
13	<<new>>	<<new>>					

Figure 5 – Assignment Editor

- Assign all inputs and outputs to any of the general purpose pins on the FPGA board. For a list of available pins, refer to http://vader.ece.ucsb.edu/digilab-fpga/pintable.html
- If you are driving LED outputs, assign those to "high-drive" I/O pins
- Save your project.

7. Compile Project Again

- Select Processing > Start Compilation

8. Download to Board

After a successful compilation, an ".rbf" file is generated in your project folder.

- Download onto your local machine the program FPGATool.exe from the FPGA website:

http://vader.ece.ucsb.edu/digilab-fpga/

- Use this program to test your FPGA board and download the .rbf to your board.