ECE 152A-Winter 2014

University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 152A Digital Design Principles
Course Syllabus

A. Basic Course Information

Instructor: Prof. Volkan Rodoplu
Room 4113, Engineering I
Email: vrodoplu@ece.ucsb.edu
Office Hours: TBA

Lecture Hours and Location:
3:30 PM - 4:45 PM Monday & Wednesday LSB 1001

Course web page:

http://www.ece.ucsb.edu/courses/ECE152/152A_W14Rodoplu/ECE_152A/Home.html

Labs:

All labs are held in "DigiLab": Harold Frank Hall, Room 1124.

TA Weekly Office Hours:

See the course web page for the TA office hours.

Textbook and References:

(Optional) Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd edition, McGraw-Hill.

(Optional) Charles H. Roth, Jr., "Fundamentals of Logic Design", 7th Edition, Brooks/Cole.

Grading:

30% Homework

35% Laboratories
[Lab 1: 6%, Lab 2: 7%, Lab 3: 7%, Lab 4: 15%]

35% Final Exam

Final Exam Date:

Check the course catalog for time. Place will be announced on the course web page.

Prerequisites:

Know the material in Chapters 1-5 of Charles Roth's book "Fundamentals of Logic Design".

B. Tentative Course Calendar and Topics:

Week of	**LABORATORY**	**Monday Lecture**	**Wednesday Lecture**
Jan.6	NO LABS	(Lecture 0) Organizational Lecture	(Lecture 1) Review of Boolean algebra, map word problem to combinational logic.
Jan. 13	Lab 1 check-in [Lab # 1: Pre-lab encouraged to finish, but due next week]	(Lecture 2) Algebraic simplification theorems, Boolean functions, bubble-pushing, functional completeness, NAND/NOR-only circuit design.	(Lecture 3) Muxes, half and full adder, Boolean cube, K-maps, maxterm and minterm expansions, don't cares.
Jan.20	Lab 1 continues [Lab # 1 Pre-lab due]	HOLIDAY	(Lecture 4) Propagation delay, timing diagram, critical path, Verilog for combinational logic; interface and implementation. **[HW # 1 due, this Friday]**

Jan.27	Lab 1 check-out. Lab 2 check-in. [Lab # 2: No pre-lab due]	(Lecture 14) [Note: This numbering matches the lecture #'s on the web page.] 2's complement arithmetic, adder/subtractor, fast adders: carry look-ahead adder.	(Lecture 14) Fast Adders (continued)
Feb.3	Lab 2 continues.	(Lecture 5) Basic latch, D latch and D flip-flop (behavioral); design of registers, shift registers and counters.	(Lecture 6A) Timing diagrams of latches, flip-flops, shift registers, counters; T flip-flop, JK flip-flop, use of tristate buffers with memory elements.
Feb.10	Lab 2 check-out Lab 3 check-in [Lab # 3: Pre-lab encouraged to finish, but due next week]	(Lecture 6B) More design examples with latches, flip-flops, shift registers, counters.	(Lecture 7) Finite State Machines: Mapping word problems to FSMs; state diagram, state table, state assignment; Mealy/Moore machines. **[HW # 2 due, this Friday]**
Feb.17	Lab 3 continues [Lab # 3: Pre-lab due]	HOLIDAY	(Lecture 8) Timing diagrams for Mealy/Moore machines; map state diagram to flip-flop implementation.
Feb.24	Lab 3 check-out Lab 4 check-in [Lab # 4: No pre-lab due]	(Lecture 9A) Verilog for sequential design; RTL and behavioral Verilog for FSMs.	(Lecture 9B) Examples of Mealy/Moore machines; mapping word problems to state diagrams.

Mar. 3	Lab 4 continues	(Lecture 11A) Timing of sequential circuits: set-up, hold times, propagation delays, minimum clock period	(Lecture 11B) Examples of timing problems in sequential circuit design. **[HW # 3 due, this Friday] (This is a long homework. You are given 3 weeks to do it.)**
Mar.10	Lab 4 check-out	(Lecture 13) Review for Final Exam	(Lecture 16) Review for Final Exam **[HW # 4 due, this Friday]**

C. Graded Course Work and Rules:

C. 1. Laboratory Rules and Recommendations:

Rules:
The labs will be done in teams of two people. You may not have someone else outside the course or a member of another team in class do your lab (or sections of the lab) for you. It is fine to discuss, to get help from others in class as well as other students on debugging, but once you understand the problem, you (as a team) must go ahead and carry out the solution on your own. Only 1 write-up is required per team.

Usually, we will not accept any late labs. Each lab's grading is divided into demonstrable milestones. Any milestones completed before the deadline, if demonstrated and are correct, will get full credit. For some labs, we may advertise a late policy of a few days. In that case, any milestone of the lab that is late will get 50% of the credit that would be earned if that milestone had been completed on time.

There is usually a pre-lab due at the beginning of each lab. SUBMIT your pre-lab to the TA electronically before the lab starts, or hand in a clear photocopy of your pre-lab at the beginning of the lab, to the TA. Keep the actual write-up for yourself as you will be using that in the rest of the lab.

If you burn an FPGA board that you have checked out from the ECE shop, you will be charged 1/2 of the cost of the board, in order to get a new one. Follow the wiring guidelines for each lab.

Recommendations:
The strategy that we recommend for the labs is to start early and make as much progress as possible on your own as a team. Use the lab sessions very well: Ask the TA's the troubling points to remove any problems that are preventing your progress in the labs. Go to the TA's office hours held in the laboratory room for extra help. When you do the labs, try to understand fully why things are the way they are. The clarity of the top level design on any project is extremely important. Before you jump into implementation, make sure that you have understood the problem at the highest level of abstraction correctly and designed the top level solution with the tools at this level. If you have any doubts about the project specification, it is important to clear them as high up in the design abstraction chain as possible.

C. 2. Homework Rules and Recommendations:

Rules:
For the homework, you have a choice: (1) You may choose to work alone on each homework, OR (2) each homework may be be done by a team of 2 people (in which case you hand in only 1 homework solution per team). Your team need not be the same as your lab team; however, once you choose it, it must be fixed for the rest of the term.

The only exception that will be allowed to the above is if two people who chose to work alone, decided to become homework partners on a longer homework. If they do this, they must stick together for the rest of the term.

No homework teams of 3 or more people will be allowed (even if it means that one person in class will need to work alone).

Homework is due in the HOMEWORK BOX on the 3rd floor of Harold Frank Hall, on the date and time shown for that homework on the course web page.

Late homework gets a zero. The only exception to this is a well-documented, legitimate emergency.

You are allowed to talk about homework with other teams in this class; however, when it comes to writing up your solutions, each team must produce its own write-up. You may not copy someone else's solutions, solutions from the instructor's manual or solutions from previous years. You may not have someone outside the course (e.g. a student who has taken the course before) do you homework for you. You may discuss the homework assignments and solution strategies with anyone, but the work that a team hands in must be the team's own write-up.

Recommendations:
The strategy that we recommend is to start the homework early and do as much of the homework as possible on your own. Then, get together with other students who have done the same to check your answers with each other's, discuss the points on which you disagree, find correct solutions and then write up the corrected solution yourself.

C. 3. Exam Rules and Recommendations:

Rules:
The following rules govern the final exam:

At the end of the exam, we will tell you to stop writing and raise your exam booklet high. If you continue writing, we will deduct roughly 5%

per minute from your exam score. Wait in your seat until we announce that ALL of the exams in the exam room have been collected.

If you finish your exam early, you may hand in your exam and then leave the exam room until 10 minutes before the exam is over. Once you hand in your exam, you may not get it back to make further changes. After we enter the last 10 minutes of the exam, even if you finish early, you need to wait in your seat for time to be called.

If you arrive late for the exam, you will not be given extra time at the end of the exam.

If you need any special accommodations for the exam room, you need to talk to the instructor in advance and as soon as you become aware of such special needs.

You must write the exam on your own. Receiving or giving help during the exam is prohibited. The exam will be in class and will be closed book. You may not bring any devices to the exam on which equations can be stored or any wireless devices that can retrieve such data.

If we cannot read your answer, we cannot give you any credit. If you have very bad handwriting, please see the instructor at the beginning of the quarter.

If you do not show up for the exam, you receive a zero for that exam. The only exception to this rule is an emergency that is well-documented. As soon as you become aware of such an emergency, you need to contact me so that I can find a reasonable solution.

You must write your name on the sheet that contains the exam questions and hand in this sheet along with your exam. We will return the exam questions along with graded the exam.

It is usually impossible to take the exam earlier or later. However, in case of emergencies, you will be allowed to receive an Incomplete for the course, and take the exam the next time the course is offered.

Recommendations:
The strategy that we recommend for the exam is (1) clear up your confusions way before the exam by going to the office hours of the professor and the TA's, (2) have a clear understanding of the digital design chain, i.e. how high-level abstractions are successively mapped down to low layers.

A common pitfall in studying for the exam is to "go over" the lecture and homework material by flipping pages and recognizing correct solutions. This will usually not prepare you well for the exam in this course. You need to take new problems (from your textbook, previous year's the exam that we hand out, or from other textbooks or sources) and actively solve new problems. If you had difficulty with a homework problem, don't look at any solutions or textbooks; instead try solving the problem again from scratch and figure out where you are having difficulty.

The final exam will be comprehensive, and cover all of the lecture notes, reading, laboratories and discussions. It will be design-oriented. On the exam, you will typically be given a word problem and asked to produce a design that solves the problem. It is very important to internalize the design process and get the system timing right on these problems. A superficial understanding of the material will not suffice.

D. Policy on Student Misconduct:

We will be vigilant to detect student misconduct and to investigate any reported cases. In this course, copying someone else's solutions, copying solutions from the instructor's manual, copying solutions from previous years' labs, student folders, or published homework and exam solutions, using books in a closed-book exam, copying from someone else during the exam, are first-degree offenses. If we find any evidence of these or other offenses, we will refer the case immediately to the committee on student misconduct.