University of California, Santa Barbara

Department of Electrical & Computer Engineering

CMOS Analog VLSI I ECE 194A/594A

Professor Theogarajan

Design Project 1, Due November 10, 2008

The design project is meant to give you design experience and make you familiar with design tools. Though you can work in teams it will be more beneficial for you if you work individually.

The best design will be presented in class!! GOOD LUCK

For NMOS Devices

Strong-Inversion:

$$\text{Linear Region: } I_{ds} = \frac{\mu_n C_{ox} W}{L}\left[\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}\right]$$

$$\text{Saturation: } I_{ds} = \frac{\mu_n C_{ox} W}{2L}\left[(V_{gs} - V_{tn})^2(1 + \lambda V_{ds})\right]$$

$$\text{Weak Inversion(Subthreshold): } I_{ds} = I_{0n} W \exp\frac{qV_{gs}}{nkT} \exp\frac{-q(n-1)V_{sb}}{nkT}\left(1 - \exp\frac{-qV_{ds}}{kT}\right)$$

For PMOS Devices:

Strong-Inversion:

$$\text{Linear Region: } I_{sd} = \frac{\mu_p C_{ox} W}{L}\left[\left(V_{sg} - |V_{tp}| - \frac{V_{sd}}{2}\right)V_{sd}\right]$$

$$\text{Saturation: } I_{sd} = \frac{\mu_p C_{ox} W}{2L}\left[(V_{sg} - |V_{tp}|)^2(1 + \lambda V_{sd})\right]$$

$$\text{Weak Inversion(Subthreshold): } I_{sd} = I_{0p} W \exp\frac{qV_{sg}}{nkT} \exp\frac{-q(n-1)V_{bs}}{nkT}\left(1 - \exp\frac{-qV_{sd}}{kT}\right)$$

For the $0.18\mu m$ TSMC process you can use the following in your hand calculations. Note that this is valid *only* for the minimum channel length of $0.18\mu m$

$$V_{tn} = |V_{tp}| = 0.5V$$

$$\frac{\mu_n C_{ox}}{2} = 175\frac{\mu A}{V^2}$$

$$\frac{\mu_p C_{ox}}{2} = 35\frac{\mu A}{V^2}$$

$$I_{0n} = 20\frac{pA}{\mu m}$$

$$I_{0p} = 10\frac{pA}{\mu m}$$

For PMOS & NMOS $n = 1.2$

1. The goal of this design project is to design a current bias network that is capable of generating $10\mu A$ currents. The target process for this design is the $0.18\mu m$ CMOS process from TSMC. The design must meet the following criteria. For each criteria that is not met points will be taken off.

    1. No resistor value greater than $10K\Omega$ may be used and can only be changed in increments of $0.1K\Omega$. Assume the resistor has a $\pm 10\%$ Variation.
    2. The bias network must have a PSRR better than 60dB in all corners
    3. The circuit must be minimally sensitive ($\leq 1\%$ current variation) to process variation.
    4. The circuit must operate reliably in a supply range of $1V \leq V_{dd} \leq 1.8V$.
    5. Power dissipation $\leq 30\mu W$ with a 1V power supply
    6. The bias network must contain a start-up network
    7. The current density matching in all branches of your circuit must be better than 1%

    (a) (30 points) Choose a topology that will fit the criteria 1-7 and size it by hand.

    (b) (15 points) Simulate(Transient) the circuit in the nominal corner and using a power supply of 1.8V, plot the various branch currents. Resize the circuit if necessary to meet the current criteria. Repeat the simulation for 1V

    (c) (10 points) Do an AC simulation on the supply and plot the results in a bode plot format. Does it meet the PSRR criteria?

    (d) (20 points) Redo the above simulations (b&c) in the fast,slow, slow N-fastP, fast N-slow P corners for both power supply corners. Also vary the resistor value for each corner. Is your circuit robust to variations? If not could you suggest a way to fix it?

    (e) (10 points) Does the circuit behave as designed, if you had to resize or change the topology(honor system!) can you explain why and what you did to solve the problem.

    (f) (10 points) Plot the current in the power supply and multiply this by 1V this will give you the power dissipation. Do you meet the power dissipation specifications?

    (g) (5 points) Create a Table with the required design specs 1-7 and the specs that were obtained. Indicate if you met the design specifications or not.