University of California, Santa Barbara

Department of Electrical & Computer Engineering

CMOS Analog VLSI I ECE 194A/594A

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Design Project 2, Due December 8, 2008

As transistor channel lengths start to decrease, it becomes harder to design analog circuits in theses processes. Nevertheless, designing high performance analog circuits is necessary for high performance A/D, D/A and filters. This design project will highlight some of the obstacles that you might face as an analog designer. You can work in teams of 2 or individually if prefer. You are expected to turn in a hard-copy of a power-point presentation of your design which you will then present in class. The duration of the presentation is 20 minutes with 5-10 minutes for questions.

You are advised to start early!!! GOOD LUCK!

For NMOS Devices

Strong-Inversion:

$$\text{Linear Region: } I_{ds} = \frac{\mu_n C_{ox} W}{L}\left[\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}\right]$$

$$\text{Saturation: } I_{ds} = \frac{\mu_n C_{ox} W}{2L}\left[\left(V_{gs} - V_{tn}\right)^2\left(1 + \lambda V_{ds}\right)\right]$$

$$\text{Weak Inversion(Subthreshold): } I_{ds} = I_{0n} W \exp\frac{qV_{gs}}{nkT}\exp\frac{-q(n-1)V_{sb}}{nkT}\left(1 - \exp\frac{-qV_{ds}}{kT}\right)\left(1 + \lambda V_{ds}\right)$$

For PMOS Devices:

Strong-Inversion:

$$\text{Linear Region: } I_{sd} = \frac{\mu_p C_{ox} W}{L}\left[\left(V_{sg} - |V_{tp}| - \frac{V_{sd}}{2}\right)V_{sd}\right]$$

$$\text{Saturation: } I_{sd} = \frac{\mu_p C_{ox} W}{2L}\left[\left(V_{sg} - |V_{tp}|\right)^2\left(1 + \lambda V_{sd}\right)\right]$$

$$\text{Weak Inversion(Subthreshold): } I_{sd} = I_{0p} W \exp\frac{qV_{sg}}{nkT}\exp\frac{-q(n-1)V_{bs}}{nkT}\left(1 - \exp\frac{-qV_{sd}}{kT}\right)\left(1 + \lambda V_{ds}\right)$$

For the $0.18\mu m$ TSMC process you can use the following in your hand calculations. Note that this is valid *only* for the minimum channel length of $0.18\mu m$. The channel length modulation parameter can be found by simulation, you may (at your own risk) use a value of 0.1 for a channel length of $0.18\mu m$ in strong inversion. In weak inversion this will degrade and you can use a value of around 0.4

$$V_{tn} = |V_{tp}| = 0.5V$$
$$\frac{\mu_n C_{ox}}{2} = 175\frac{\mu A}{V^2}$$
$$\frac{\mu_p C_{ox}}{2} = 35\frac{\mu A}{V^2}$$
$$I_{0n} = 20\frac{pA}{\mu m}$$
$$I_{0p} = 10\frac{pA}{\mu m}$$

For PMOS & NMOS $n = 1.2$

1. The goal of this design project is to design a fully differential high-gain , high-bandwidth CMOS operational transconductance amplifier with a large dynamic range

   The following constraints must be met.

   1. The bias current for your amplifier *must* be derived from a bias generator. Preferably you will use the design from you design project 1.
   2. The open-loop gain of your amplifier must be $\geq 100dB$
   3. The unity gain frequency of your design must be $\geq 50MHz$ for a 1pF load to ground on each output.
   4. An input common-mode range of $\geq \pm 200mV$ at a supply voltage of 1V
   5. The circuit must operate reliably (i.e meet all specs) in a supply range of $1V \leq V_{dd} \leq 1.8V$.
   6. Power dissipation $\leq 250\mu W$ with a 1.8V power supply including the bias network.
   7. A CMFB Circuit is expected for this fully differential design
   8. An output swing of 1.5V for a 1.8V supply
   9. Worst Case Systematic offset of 1mV
   10. Settling time of $\leq 120ns$ to settle with 0.1% of the final value
   11. A Common mode rejection ratio (CMRR) $\geq 70dB$ at an input common-mode equal to $\frac{V_{dd}}{2}$
   12. A phase-margin of $\geq 50°$, additionally you may not use compensation capacitors greater than 5pF.
   13. Power-Supply Rejection Ration (PSRR+,PSSR-) $\geq 70dB$ at 100kHz. The PSRR+ refers to the a voltage applied on VDD and PSSR- to an ac votage applied between the negative rail and gnd. For this you will have to tie all the NMOS nodes normally at GND to a pin.
   14. A dynamic range $\geq 83dB$ at a supply voltage of 1.8V.
       Dynamic range is given by $DR = \frac{V_{\text{output swing}}}{\text{Input Referred Noise}}$ For a 1.8V supply with an output swing of 1.5V this translates to $\cong 100\mu V$ of input referred noise of in-band noise given by $\left(\sqrt{\frac{V_{noise}^2}{Hz} \times \text{Unity gain bandwidth}}\right)$ when the amplifier is in unity gain configuration driving a 1pF load.
   15. The circuit must be minimally sensitive (i.e. meet all specifications) to process variation.

   Some additional things you should consider

   1. You will be graded on the overall size of your circuit
   2. Using widths $> 100\mu m$ or lengths $> 1.8\mu m$ will result in points being deducted.

Your presentation needs to contain the following

(a) (50 points) Design a topology and size it by hand, describe how this topology meet the above criteria and the basis for your choices. A table comparing the specifications from your hand calculation and the simulator

(b) (15 points) Step response of your amplifier for a 100mV step for both rising and falling steps with your op-amp in unity gain configuration, see figure 1.

(c) (15 points) AC responses indicating the phase margin, the open-loop gain and unity-gain frequency, noise simulation, PSRR and CMRR. A clear explanation of the shape of your AC response.

(d) (20 points) A table listing the performance of the circuit in all corners

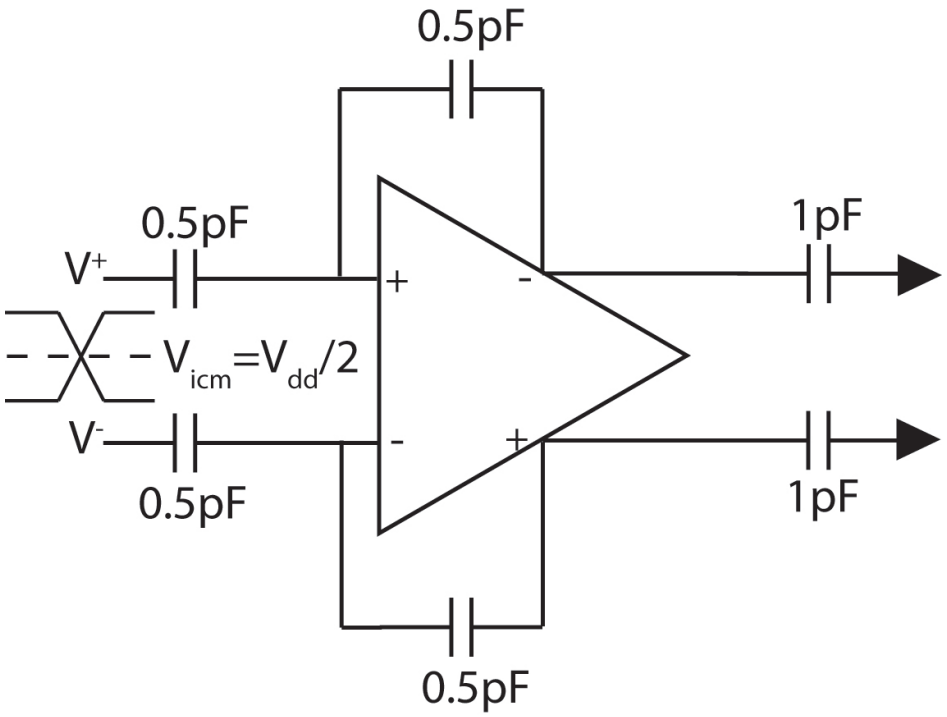

Figure 1: Configuration for testing step response