# Problem Set 1

Prof. Luke Theogarajan
ECE 194A/594A
Department of Electrical & Computer Engineering,
University of California, Santa Barbara

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For all problems, unless otherwise stated, assume room temperature of 300K, i.e $\frac{kT}{q} \cong 26mV$ and $n_i^2 = 10^{20}$

**Problem 1**

You have joined one of the leading circuit design companies as a junior designer. One of your colleagues cannot understand why the characteristics of the two transistor configurations shown in figure 1 are the same. You having taken 594A and from your knowledge of device physics would like to understand this quantitatively. Assume that the body effect and channel modulation are absent to make matters simple.

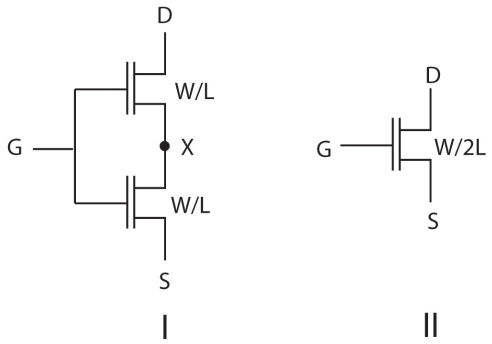


Figure 1: The two circuit configurations for Problem 1

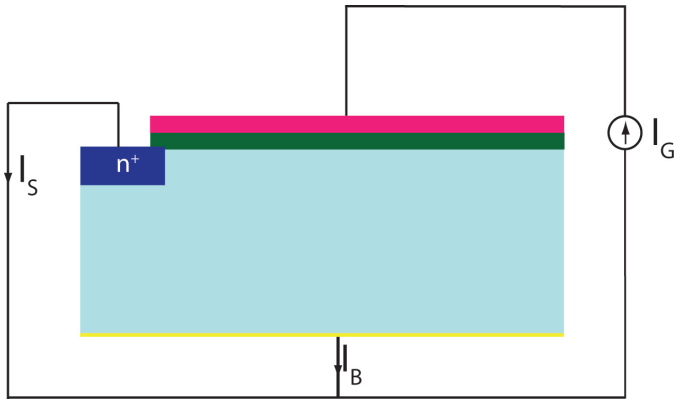


Figure 2: Three terminal MOS structure for Problem 2

a) For configuration I for $V_{ds} \geq V_{dsat}$ what regions are the two transistors operating in?

b) For configuration I for $V_{ds} \geq V_{dsat}$ derive the drain current for each transistor in terms of $V_{gs}$,$V_{ds}$,$V_T$ and $V_{xs}$. From this derive an expression for $V_{xs}$

c) For the same value of $V_{gs}$,$V_{ds}$ in both transistors with $V_{ds} \geq V_{dsat}$ derive the saturation current$I_{DSAT}$ in both configurations shown. How do the values compare?

d) Derive the expression for $V_{dsat}$ for both configurations with the same $V_{gs}$.

e) From the above can you qualitatively explain why the configurations exhibit similar characteristics?

**Problem 2**

Consider the three terminal MOS structure shown in the figure 2 below. The Work function of the gate material, $W_M = 4.04eV$, the oxide thickness, $x_{ox} = 10nm$ and the doping concentration of the p-tye substrate is $N_A = 10^{17}cm^{-3}$.

For $t < 0$ the sturcture is in equilibrium i.e. $I_G = 0$ and t=0, the current source is stepped to a value of $I_G = 10nA$.

*Quantitatively* sketch the current evolution through time in the bulk $I_B$ and in the source $I_S$.

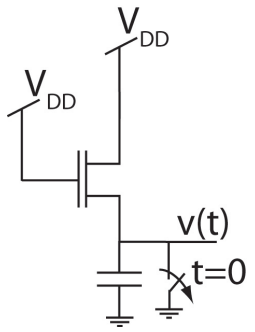


Figure 3: Circuit for problem 3

**Problem 3**

Prob 2.8 In CMOS-OPAMPS and Comparators In the circuit shown below in figure 3 the switch S is opened at time t=0 Answer the following questions

(a) In what region is the transistor operating at the time the switch opens

(b) Neglecting body-effect and channel length modulation find v(t)

**Problem 4**

A normal trick used by circuit designers to save area and in some process that do not have dedicated linear capacitors ( Metal-Metal or Poly-Poly) is to use the MOSFET as a capacitor. You are designing a charge-pump for a Delay Locked Loop that needs a large capacitor in 0.18 $\mu$m process with an oxide thickness of 4.1 nm and nwell doping of $N_D = 4.1 \times 10^{17}$ and $V_{TH0} = -0.39$. The circuit A is shown in figure 4. You notice that it would be better from a performance standpoint of view if the capacitor decreased linearly with the voltage on the output node $V_{ctrl}$. While discussing this with you friend, Anna Logue, she tells you to try out the configuration in circuit B.

a) What is $\phi_{bi}$ of this process?

b) Quantitatively sketch the capacitance/area as a function of voltage in circuit A.

c) Quantitatively sketch the capacitance/area as a function of voltage in circuit B.

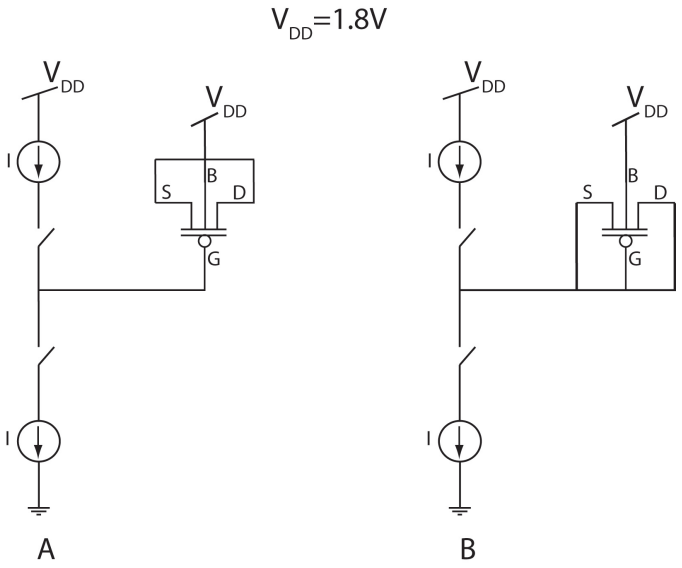


Figure 4: The charge pump and capacitor in two configurations

d) Comment on the results found in b & c.