Problem Set 2

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Problem 1

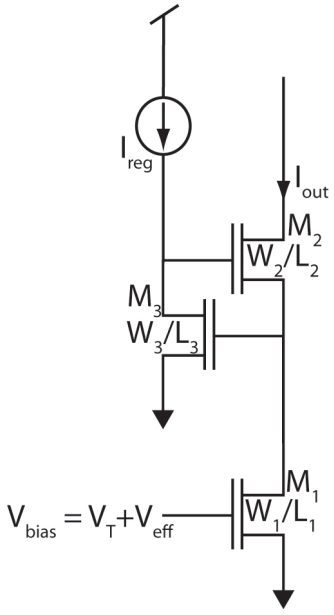

Figure 1: Figure for Problem 1

The circuit in figure 1 is called the *regulated cascode*, since the V_{ds1} of transistor M_1 is regulated by the common source amplifier.

a What is the gate voltage of transisotr M_2? Confirm your answer with an appropriate derivation.

b Calculate the output impedance of this circuit. Assume all transistors are biased in the saturation region(*Hint:* It will be easier if you use a feedback block diagram approach)

c What is the minimum voltage the o/p of this stage can swing to?

d One of the problems with this circuit is that V_{ds1} needs to be at least $V_T + V_{eff3}$, one of your friends suggest that why don't you change the current in the common source to operate n the subthreshold thereby enabling $V_{ds1} < V_T$, will this work? If so are there any problems with this circuit?

Problem 2 One of the problems of the regulated cascode was the o/p swing.

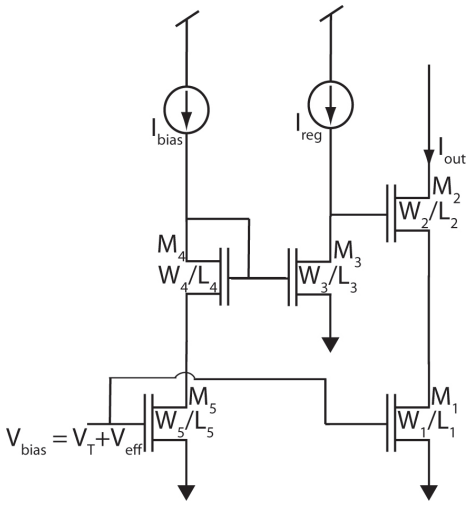

Figure 2: Figure for Problem 2

Your friend Smar T. Pants comes up with the circuit shown in figure 2. While you were looking at his notes in Goleta beach park, the sheet which has the explanation of how the circuit works, the size and current relationships gets swept by a gust of wind into the ocean. You decide that you would like to figure out how the circuit works and how to size it.

a Give a *qualitative* description of how the circuit works

b Assume that transistor M_1 and M_2 are sized the same. One of the supposed advantages of this circuits is that it gives the maximum output swing i.e. $2V_{eff}$ from each supply rail. From your knowledge of current mirror design

- what is the gate voltage of transistor M_2 have to be for this to be satisfied?

- You notice that the transistors M_3 and M_4 form a current mirror but one whose gate-source voltages are not equal? What is the consequence of this?
- If the optimal gate voltage is to be imposed on M_2 as you calculated what should the gate voltage of Transistor M_3 given that this optimal voltage is the drain voltage of M_3?
- If all these voltages are imposed correctly what is the drain voltage of M_5 and M_1?

c What should the value of I_{reg} be in terms of I_{bias} to ensure that voltages are imposed correctly?

d Do I_{bias} and I_{out} have to be related? Explain

e Give the relationship between all the currents and W/L of all the transistors.

Problem 3

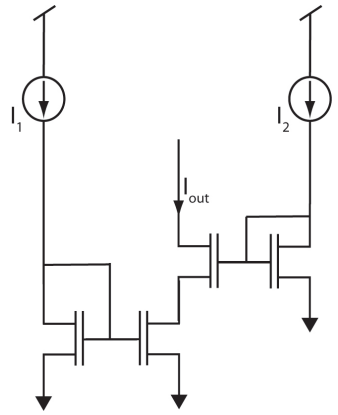

Figure 3: Figure for Problem 3

Your friend D.J.Tal sees your 594 notes and the draws the circuit shown in figure 3 and claims that the circuit is an analog AND gate with current inputs I_1 and I_2 i.e the o/p is a high current when both currents are high and low if one of them is smaller than the other.However, your friend Anna Logue whom you met in while discussing the last problem set says that it looks more like a normalized multiplier. You want to find out quantitatively who is right. Assume all transistor parameters are the same.

a Assume I_1 and I_2 are subthreshold (i.e $I = I_0 \exp \frac{qV_{gs}}{kT}$)currents compute the current I_{out} as function of I_1 and I_2 (*Hint:* Current through both transistors must be equal!)

b Assume that I_1 and I_2 are now operated above threshold, calculate I_{out}.

c From your answers to a & b how does the circuit behave according to you.

Problem 4

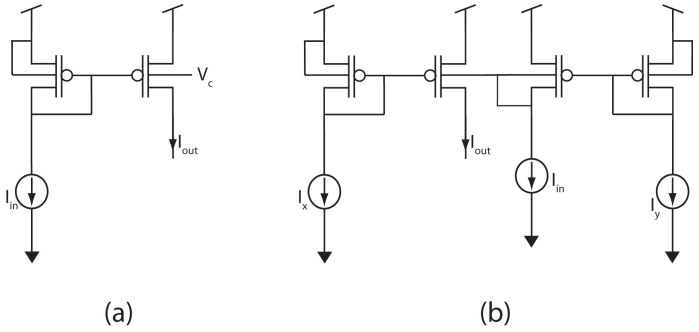

Figure 4: Figure for problem 4

Consider the circuit shown in figure 4(a), assume that all the transistors operate in the subthreshold regime i.e. the input current is a subthreshold current.

a Calculate I_{out} as a function of I_{in} and V_c.

b Consider the circuit shown in figure 4(b) Using your answer from (a) derive a relationship between I_{out}, I_x, I_y and I_{in}.

c Would these circuits work similarly in the above threshold regime? Explain

d Are there any precautions that must be taken when operating this circuit?