Is Nanoelectronics the Future of Microelectronics?

Mark Lundstrom
Electrical and Computer Engineering
1285 EE Building
West Lafayette, IN USA
01-765-494-3515
lundstro@purdue.edu

ABSTRACT
We examine current research in nanoelectronics and discuss the role it may play in future electronic systems.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, memory technologies, VLSI*

General Terms
Design, Performance, Theory

Keywords
nanoelectronics, Moore's Law, molecular electronics

1. INTRODUCTION
Silicon technology continues to progress rapidly, with current generation technologies having physical gate lengths below 100 nm. At the same time, remarkable advances in non-silicon nano- and molecular technologies is occurring. It is time to think seriously about the role that nanoelectronics and non-traditional technologies could play in future electronic systems.

I come to nanoelectronics from a traditional route, having worked on the physics of conventional semiconductor devices. Device scaling carried me into the nanoworld. Some years ago, I saw this coming and forged a partnership with researchers in molecular electronics. I didn't see ideas that seemed likely to replace silicon technology, but I was convinced that the tools, techniques, and understanding developed by nano- and molecular electronics researchers were sure to be useful for small electronic devices of any kind. That prediction is coming true; well-established concepts from mesoscopic physics [1] are now entering the working knowledge of device researchers and engineers as silicon transistors enter the nanoscale [2]. In addition, several interesting new devices that may have important applications are also being developed [3-6].

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Nanoelectronics can play an important role in future electronic systems, if the design community is engaged to exploit the opportunities that nanoelectronics offers. So I welcome this opportunity to present some thoughts to you. The paper begins by trying to define what nanotechnology is, then examines where nanoscale silicon technology is heading. Radically new devices and what they might offer are also discussed.

2. WHAT IS NANOELECTRONICS?
The National Science Foundation defines nanotechnology as work at the 1 – 100 nm length scale to produce structures, devices, and systems that have novel properties because of their nanoscale dimensions [7]. Some insist that two dimensions lie in the 1-100 nm regime, which would rule out traditional technologies such as thin films. A key part of the definition is that new phenomena occur (caused, for example, by the dominance of interfaces and quantum mechanical effects) and that these new phenomena may be exploited to improve the performance of materials, device, and systems. Nanotechnologies also involve the manipulation and control of matter at the nanoscale. Semiconductor technology does much of this with a "top-down" approach that lithographically imposes a pattern, then etches away bulk material to create a nanostructure. Some argue that self-assembly is an essential component of nanotechnology. The hope is that nanostructures can be self-assembled from the "bottom up" molecule by molecule.

In the next section, I will argue that current-day silicon technology meets the definition of nanoelectronics, that future silicon technologies will meet it even better, and that nontraditional technologies could play an important role in future electronic systems by complementing the capabilities of nanoscale silicon technology.

3. Si CMOS AT THE SCALING LIMIT
Figure 1 is a schematic illustration of a fully-depleted, double gate (DG) MOSFET, a device thought to offer the best prospects for scaling silicon transistors to their limits [8]. The ITRS extrapolations for 2016 call for 9 nm physical gate lengths. At such gate lengths, acceptable short channel effects require a fully-depleted silicon body thickness of 3 nm or less, and an equivalent gate oxide thickness of less than 1 nm. At such dimensions, the properties of the silicon material will be affected by quantum confinement (e.g. the bandgap will increase), and device properties will be influenced by quantum transport.

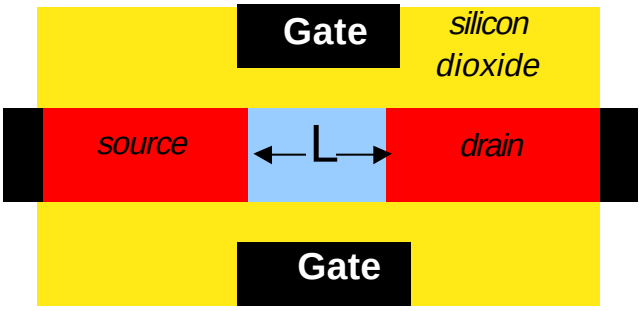

Figure 1. The double-gate MOSFET device structure.

Traditional CAD tools miss the new phenomena that occur at the nanoscale, but techniques to simulate quantum transport in small devices (e.g. a nanoscale silicon transistor or even a single molecule) are being developed [9, 10]. Figure 2 shows the result of a nonequilibbrium Green's function (NEGF) simulation of an L = 10 nm double-gate MOSFET under high gate and drain bias. The white line is the conduction subband profile, and the colors show the electron density vs. position and energy. Although quantum interference effects are apparent and tunneling through the source to channel barrier is seen, transistors at the 10nm scale continue to operate very much like classical MOSFETs. Using simulation techniques like this, we can explore silicon transistors at the scaling limit [11, 12].

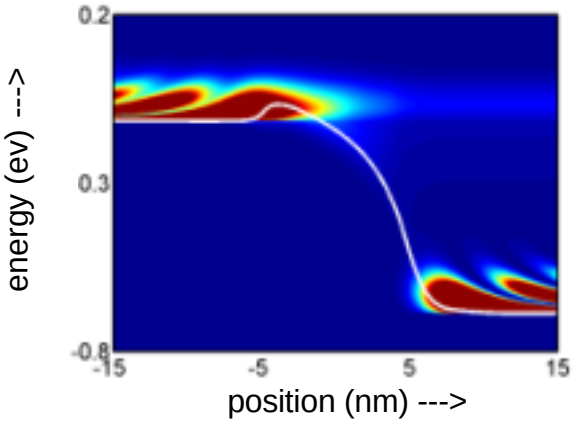

Figure 2. Simulated electron density in a DG MOSFET

Simulation techniques that capture the new phenomena that occur at the nanoscale provide a reliable guide to what we can expect from silicon technology at the scaling limit [11, 12]. Maintaining drive current at low supply voltages (~0.5V) will be very difficult, and devices parasitics will be much more important than for current technology. Devices will be extremely sensitive to manufacturing variations (a single monolayer change in the body thickness may change the off-current by a factor of 25. New design techniques will be needed to make use of devices with low drive current, high-leakage, and large process variations.

Current silicon technology, with physical gate lengths below 100 nm, and future devices at the scaling limit are true nanoelectronic devices. The materials used have dimensions in the 1-100 nm range (channel length, body thickness, junction depth, oxide thickness, etc.). The material properties are altered by the small scale (e.g. quantum confinement changes the properties of the silicon body). Manufacturing processes will have to be controlled at the atomic scale. Device fabrication makes use of top down approaches, but self-aligned device structures assemble critical features without nanoscale lithography. Finally, device performance is changing at the nanoscale, and designers will have to grapple with the same issues that face those exploring radically new devices. Silicon microelectronics is rapidly evolving into silicon nanoelectronics and will continue to do so for some time [13].

Before we turn to devices beyond CMOS, we should review the important device performance metrics for digital systems. First, the device should display gain, so that signal level can be restored. For unloaded circuits, the device delay metric, CV/I, determines circuit speed, but for loaded circuits, the on-current (typically specified per unit width) is the important metric. Device leakage is increasingly important, and is typically controlled by the subthreshold swing, S, in mV of gate voltage to change the drain current by a factor of 10.

4. MOLECULAR TRANSISTORS

A molecule has a well-defined structure with a finite number of atoms. Recently, techniques to attach contacts to molecules and measure their I-V characteristics have been developed [14-16]. Molecular transistors using carbon nanotubes have been reported [17]. More recently, complete CMOS circuits have been demonstrated [18], and the performance of individual transistors has been advancing rapidly [19]. Molecular transistors of this type are of great interest because: i) they could provide substantially improved device performance metrics, and ii) they retain the CMOS paradigm, so the design infrastructure for silicon CMOS could be retained.

One can think of a carbon nanotube as a 2D sheet of graphene (in which carbon atoms in a hexagonal lattice are bonded to three nearest neighbors as shown in Fig. 3) that is rolled up into a tube. Depending on how the sheet is rolled up to produce a tube (in a "zigzag" pattern, "armchair," or in between (chiral), the nanotube can be either metallic or semiconducting. For semiconducting tubes, the bandgap is inversely proportional to the nanotube diameter. A diameter of 1 nm (a typical value) gives a bandgap of about 0.8eV.

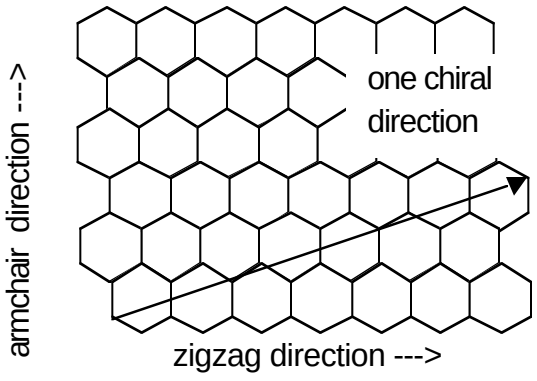

Figure 3. A 2D sheet of graphene showing the roll-up directions for different nanotubes.

The interest in carbon nanotubes arises from the unique material properties they display. The 1D energy bandstructure suppresses scattering, so ballistic transport can be achieved over relatively long distances. The thermal conductivity is exceptional, higher than diamond. These properties make nanotubes interesting for interconnects and heat removal in gigascale systems. Semiconducting nanotubes also display excellent transport properties, and the absence of dangling bonds may make it easier to incorporate high-K gate dielectrics into CNT FETs. Because the valence and conduction bands are mirror images of each other, NMOS and PMOS transistors should display essentially identical characteristics, a significant advantage for CMOS circuits. Initially, CNTFETS suffered from high series resistance and low gate capacitance. Improved contacts are being developed, and new structures employ high-K gate dielectrics. The ITRS calls for an on-current of 750 μA/μm (0.75μA/nm) for PMOS transistors in 2016, which will be very difficult to meet at the low supply voltages needed (V_{DD} ~ 0.5V). Experimental CNTFETs have already achieved over 7 μA/nm at 0.9V [19].

It's clear that carbon nanotubes have great promise, but what are the challenges? The growth of CNTs with well-defined electronic properties is a critical issue. Growth from a catalic seed can be used to control the CNT diameter, but it is more difficult to control the CNT's chirality (i.e. how it is rolled-up). For applications in terascale systems, we will need to grow at least 10^{12} CNT's – all semiconducting with well-controlled diameters. Device structures and process flows are still primitive. One approach is to produce planar FET's with arrays of CNT's to provide sufficient current for conventional digital applications [20]. This approach aims to replace the silicon CMOS transistor with a higher performance device. Another approach would be to explore the use of single nanotube electronics in dense locally interconnected architectures that could complement silicon CMOS. As CNT materials and device work proceeds, work at the system design level is needed to identify the most promising opportunities.

5. A GENERIC VIEW OF TRANSISTORS

Conventional field-effect transistors make use of silicon, III-V, or heterostructure materials. Current research is examining much different materials, such as carbon nanotubes or even self-assembled organic monolayers. The operating principles of transistors are, however, essentially the same. (Indeed, the close connection between field-effect and bipolar transistors was recognized long ago [22].) The result is that our intuition on how small silicon transistors operate provides a reasonably good guide for what to expect from molecular transistors, but some surprises can occur.

Figure 4 is a sketch of a generic transistor. The channel (silicon, a carbon nanotube, another molecule, etc.) is connected to source and drain contacts. A gate voltage modulates the charge in the active device. Because the channel is short, the drain voltage can also modulate the charge in the device, so

$$Q = C_G V_{GS} + C_D V_{DS} \qquad (1)$$

For a well-designed transistor with minimal short channel effects, $C_G >> C_D$, and the charge in the device is primarily determined by the gate voltage. Molecules may permit very short channel lengths, but the 2D Poisson equation imposes serious constraints. No matter what the material, the minimum channel length is likely to be set by the same 2D electrostatics that apply to silicon MOSFETs. Important device performance metrics like the subthreshold swing are intimately related to the operation of a transistor (thermal injection over a barrier) and are unlikely to improve for molecular transistors. The conclusion is that molecular transistors will not provide qualitatively new performance characteristics, but they may offer better performance through improved materials parameters or manufacturing considerations. There may be some interesting differences, however. For example, in a MOSFET above threshold, $C_{ins} << C_s$, where C_s is the semiconductor capacitance (sometimes called the quantum capacitance). For carbon nanotubes, high-K gate dielectrics may be more feasible, and the semiconductor capacitance is expected to be smaller. The result is that one may envision CNTFETs for which $C_{ins} >> C_s$, which is opposite to that of a conventional MOSFET and may cause a field-effect transistor to behave more like a bipolar transistor [22].

The fact that these unconventional transistors should operate similarly to the silicon MOSFET is an advantage because the CMOS design infrastructure and the enormous number of engineers who have been trained in CMOS design could be readily adapted to new CMOS technologies. Fundamentally new technologies that dispense with CMOS transistors will face the daunting task of developing a CAD design environment and an engineering workforce trained to design in the new technology.

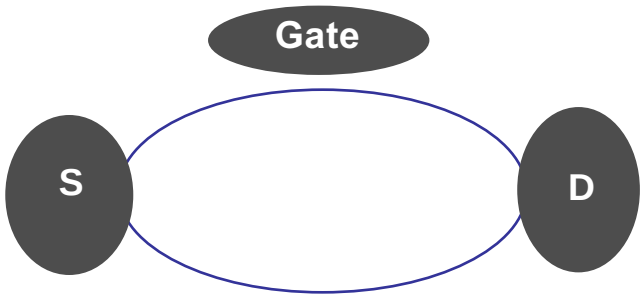

Figure 4. A generic transistor showing the active device, a gate that induces charge in it, and two contacts.

6. SINGLE ELECTRON TRANSISTORS

For future nanoscale transistors, the total number of electrons in the channel may be on the order of 10, but a single electron transistor (SET) is not just a smaller version of the same device. To produce a single electron transistor, the size of the "island" between the source and drain must be small enough so that the change in voltage due to a single electron is large compared to the thermal energy,

$$q^2/2C_G >> k_B T\,. \qquad (2)$$

Reliable room temperature operation requires an island size of less that about 1 nm. In addition, we also require that the source and drain be weakly coupled to the gated island, which is usually accomplished by introducing tunnel barriers at the two contacts. When these conditions are met, some unique IV characteristics result [23]. For example. the number of electrons on the island changes in discrete steps as the gate voltage increases, and a "Coulomb blockade" prevents current flow until V_{DS} exceeds a critical value. The critical voltage for conduction is periodic in gate voltage. Single electron transistors have been investigated for applications in digital systems, but they have several limitations [23]. The voltage gain is low and so is the drive current (because the tunnel junctions introduce a large series resistance). As might be expected, they are also extremely sensitive to stray background charges. There are, however, some hybrid SET/MOSFET circuits that are interesting for memory applications [23].

7. SPIN TRANSISTORS?

The operation of a conventional transistor is based on the charge that electrons carry, but electrons also carry spin, a fundamental unit of magnetic moment. The electron's spin is the basis for magnetic memories, but it is also conceivable that spin transistors could be achieved [24]. For example, if the source and drain were ferromagnetic, then spin-polarized electrons might be injected into a semiconductor. If they retain their spin as the propagate across the channel, they could easily exit the ferromagnetic drain, but it may be possible to rotate the electron spins by a gate voltage thereby preventing them from exiting through the drain and contributing to the drain current. Devices of this type have not yet been demonstrated, but current research is examining how to combine ferromagnetic metals and semiconductors, how to inject spin-polarized electrons into the semiconductor, and how to maintain the spin polarization once the electrons are in the semiconductor [25]. If devices of this type could be realized, they promise faster switching and lower switching energy than conventional electrostatic MOSFETs. Eventually, it may be possible to manipulate the spins of individual electrons (single electron spin transistors), which could lead to the realization of quantum computers.

8. BEYOND TRANSISTORS

I have concentrated on transistors because no alternative device with the performance, gain, and wide applicability of the transistor has yet emerged, but several novel devices are being explored. They may fill important niche applications, and if suitable novel architectures are developed, they could find wider applications. Experienced circuit designers stress the importance of gain to restore weak signals and provide voltage noise margins [James Eaton, Jr., personal communication]. Several new technologies envision using CMOS circuitry to provide gain. One example is the work at Hewlett Packard and UCLA on molecular field programmable gate arrays (FPGAs) [26]. Rotaxane organic molecules are introduced into a crossbar array of nanowires. Wherever two wires cross, a rotaxane molecule attaches itself. This array of switches is used to produce an FPGA array, but CMOS transistors are used to read out the AND and OR arrays. The technology promises a degree of self-assembly. The fabrication is designed to be simple; the system functionality is obtained from a complex programming process.

Another example of how unconventional technologies can be combined with conventional technology are integrated tunnel diode/transistors [27]. The negative differential resistance provides at least two stable bias points, which could be utilized for high-speed signal processing or for low power memory [27,28]. III-V RTD's have been used to demonstrate a variety of high-speed devices (memory, logic, ADC, dividers, etc.) [28]. The challenges for this technology lie in its extreme sensitivity to layer thickness, which limits circuit density [26]. On the other hand, recent work at Yale and Rice on nitroamine molecules [4] show resonant tunneling behavior and open up the possibility of integrating molecular resonant tunneling diodes with CMOS technology.

Another interesting hybrid is an integrated single electron device and transistor, which may prove useful for memory [23]. Many other possibilities exist, both for devices that complement CMOS or ones that are designed to replace it (e.g. Notre Dame's Quantum Cellular Automata [28]). Such work could lead to technologically significant breakthroughs.

9. BEYOND MICROELECTRONICS

Nanoelectronics is not simply a smaller version of microelectronics; things change at the nanoscale. At the device level, silicon transistors may give way to new materials such as organic molecules or inorganic nanowires [29]. At the interconnect level, microelectronics uses long, fat wires, but nanoelectronics seeks to use short nanowires [29]. Finally, fundamentally new architectures will be needed to make use of simple, locally connected structures that are imperfect and are comprised of devices whose performance varies widely.

I have argued in this paper that 21st century silicon technology is rapidly evolving into a true nanotechnology. Critical dimensions are already below 100 nm. The materials used in these silicon devices have properties that differ from the bulk. Nanoscale silicon transistors have higher leakage, lower-drive current, and exhibit more variability from device to device. New circuits and architectures will need to be developed to accommodate such devices. It matters little whether the material is silicon or something else, the same issues face any nanoelectronics technology. It's likely that many of the advances and breakthroughs at the circuits and systems levels that will be needed to make nanoelectronics successful will come from the silicon design community.

Given that we have a nanoelectronics technology and that another 20 years of exponential progress in silicon technology can be expected (leading to terascale integration [13]), why explore radically new technologies? One reason, of course, is that 20 years is not a long time to develop fundamentally new technologies, so that we need to start now, but there are other reasons. The most compelling practical reason is that the fabrication and assembly processes and the materials, device, circuit, and system understanding that we develop by examining radically new technologies are almost certain to be useful in silicon nanotechnology.

Developing an understanding of how to engineer devices at the nanoscale is a good reason to support nanoscience research. Another reason is that devices to complement silicon technology might be discovered. For example, carbon nanotube FETs could be exquisite single molecule detectors, and single electron devices could be integrated with MOSFETs for high density memory applications. Another possibility is

molecular structures that improve the performance of a CMOS platform. For example, ballistic CNTs could be high performance interconnects and efficient at heat removal. Nanowire thermoelectric cooling could lower chip temperature and increase performance [27]. So there are several good reasons to expect that research on nanoelectronics will prove to be a good investment.

The successful development of nanoelectronics will require a partnership between science and engineering. It was the same for semiconductor technology. The scientific community developed the understanding of semiconductor materials and physics and the engineering community used this base to learn how to design devices, circuits, and systems. Figure 5 summarizes this partnership. Science works in the nanoworld with individual atoms, molecules, nanoscale structures and devices, and assembly processes. Systems engineers work in the macroworld on complex systems with terascale device densities. In the middle are the device and circuit engineers. They must learn to think and work at the nanoscale to build devices and circuits that can connect to the macroworld. Their job is to hide the complexity of the nanoscale device by packaging it in a form that systems engineers can use (e.g. a compact circuit model). To turn the promise of nanoscience into practical technologies, it is essential that the systems engineering community be engaged in the effort.

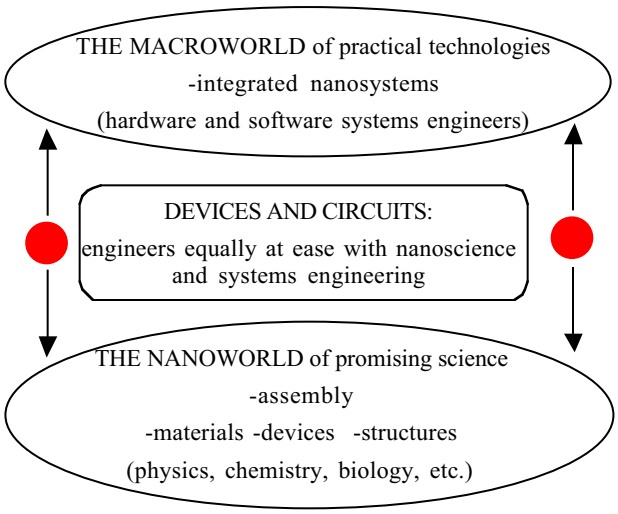

Figure 5. Science, Engineering, and Nanoelectronics.

10. CONCLUSION

The scenario that I have outlined is an evolutionary one, but exponential evolution for another two to three decades would have a revolutionary impact on society. It's also true that it's hard to predict the future. The march of science and technology has carried us to the nanoscale; it's where the action is and where unforeseen breakthroughs may occur. Remember that the transistor was developed for a very specific purpose - to replace the vacuum tube; the integrated circuit was an unexpected bonus. Our march towards nanoelectronics is unstoppable; it is the right thing to do, and who knows where it may lead?

11. ACKNOWLEDGMENTS

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