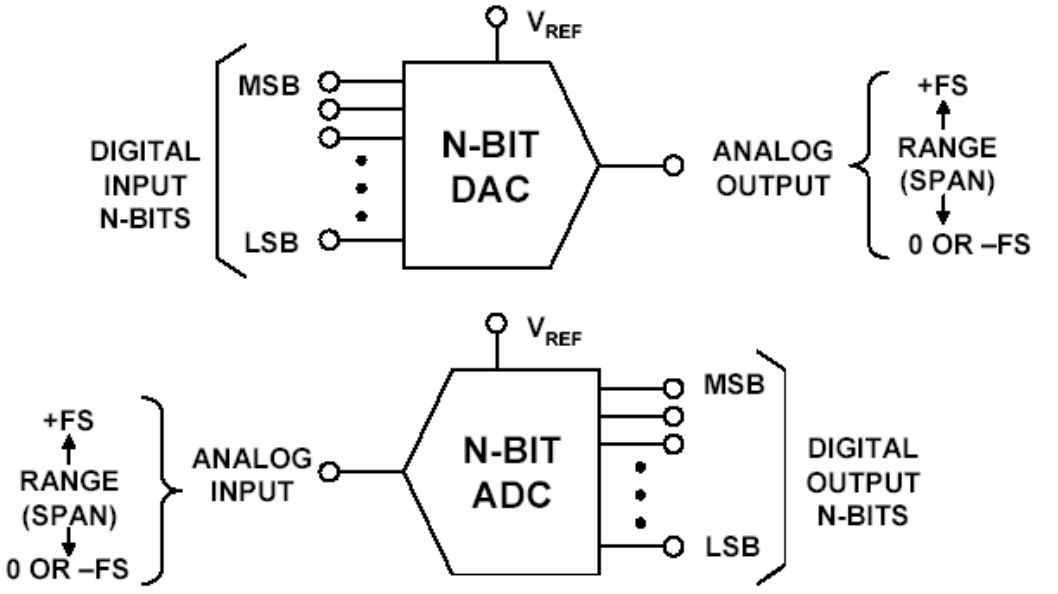


Figure 2.1: *Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) Input and Output Definitions*

Notes

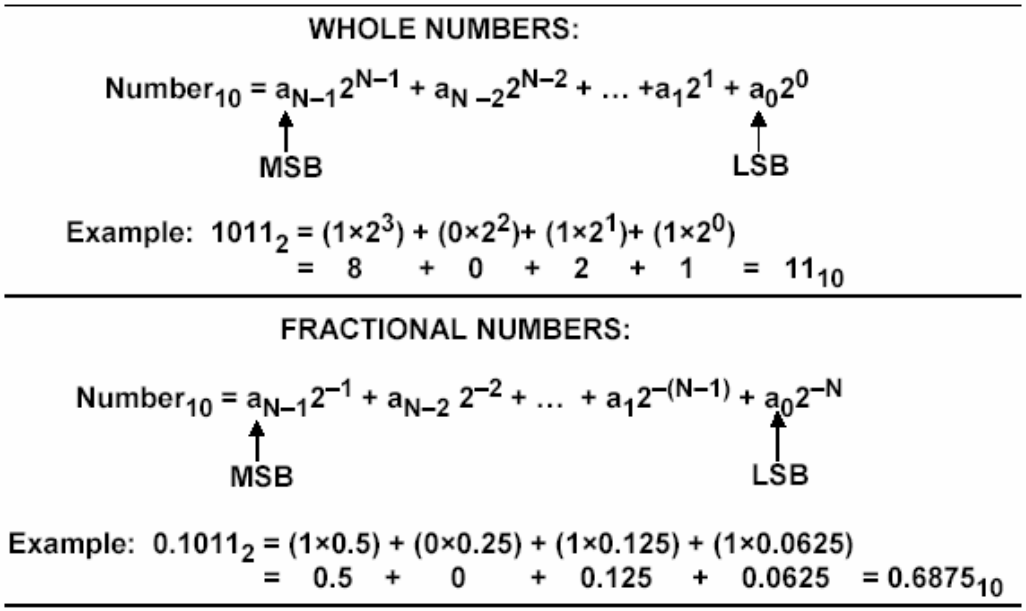


Figure 2.2: *Representing a Base-10 Number with a Binary Number (Base 2)*

Notes

BASE 10 NUMBER	SCALE	+10V FS	BINARY	GRAY
+15	+FS – 1LSB = +15/16 FS	9.375	1 1 1 1	1 0 0 0
+14	+7/8 FS	8.750	1 1 1 0	1 0 0 1
+13	+13/16 FS	8.125	1 1 0 1	1 0 1 1
+12	+3/4 FS	7.500	1 1 0 0	1 0 1 0
+11	+11/16 FS	6.875	1 0 1 1	1 1 1 0
+10	+5/8 FS	6.250	1 0 1 0	1 1 1 1
+9	+9/16 FS	5.625	1 0 0 1	1 1 0 1
+8	+1/2 FS	5.000	1 0 0 0	1 1 0 0
+7	+7/16 FS	4.375	0 1 1 1	0 1 0 0
+6	+3/8 FS	3.750	0 1 1 0	0 1 0 1
+5	+5/16 FS	3.125	0 1 0 1	0 1 1 1
+4	+1/4 FS	2.500	0 1 0 0	0 1 1 0
+3	+3/16 FS	1.875	0 0 1 1	0 0 1 0
+2	+1/8 FS	1.250	0 0 1 0	0 0 1 1
+1	1LSB = +1/16 FS	0.625	0 0 0 1	0 0 0 1
0	0	0.000	0 0 0 0	0 0 0 0

Figure 2.3: *Unipolar Binary Codes, 4-bit Converter*

Notes

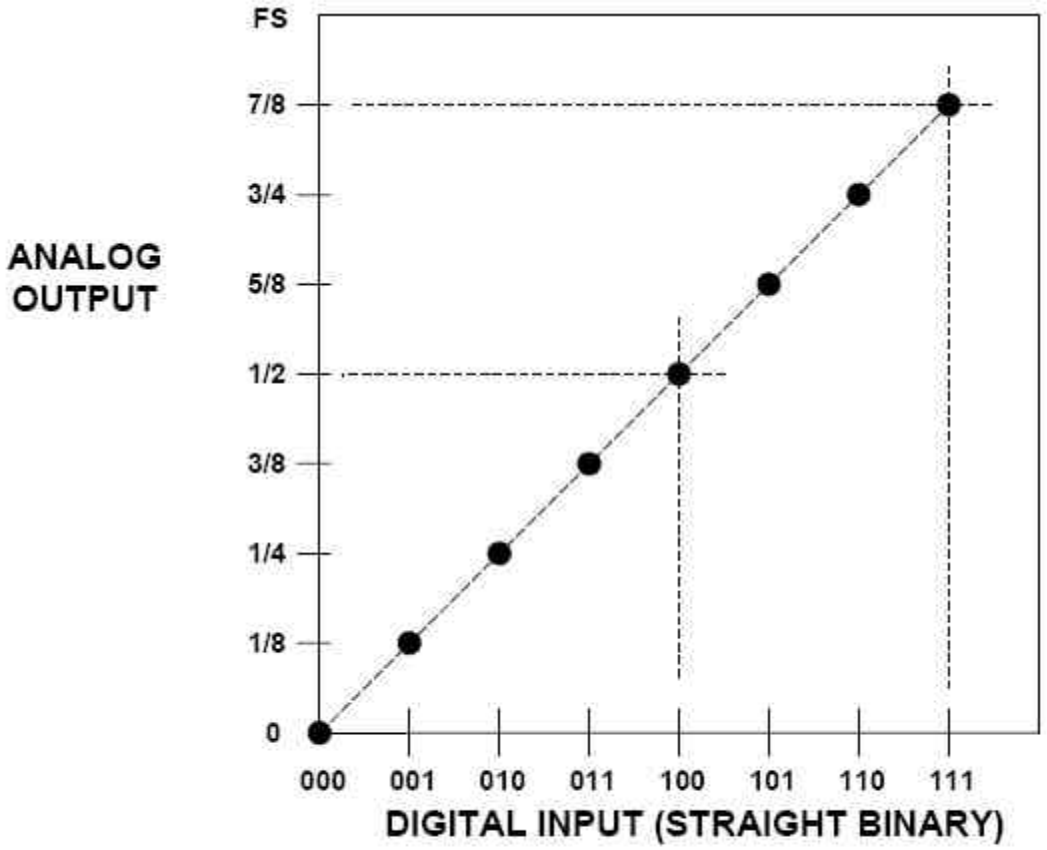


Figure 2.4: *Transfer Function for Ideal Unipolar 3-bit DAC*

Notes

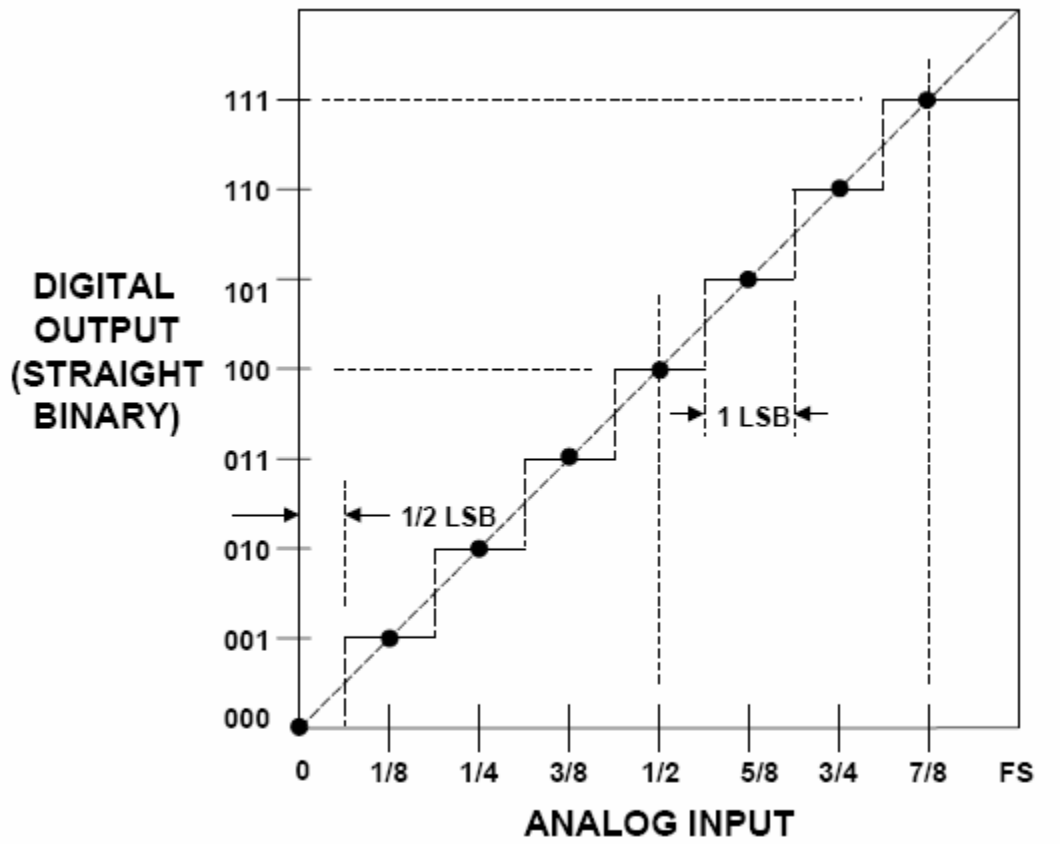


Figure 2.5: *Transfer Function for Ideal Unipolar 3-bit ADC*

Notes

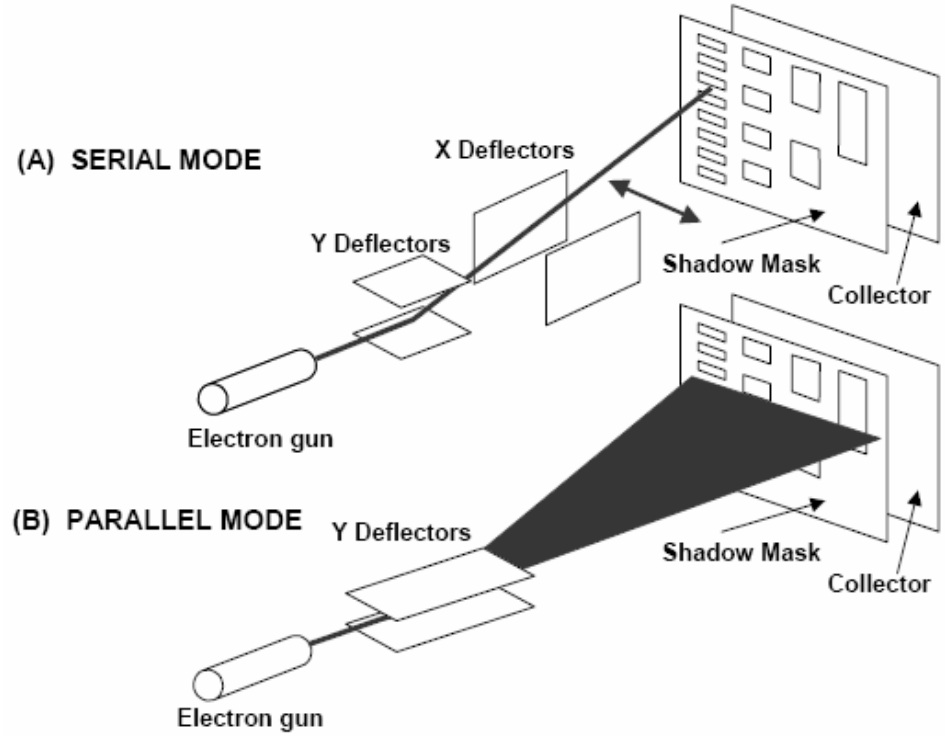


Figure 2.6: *The Electron Beam Coder: (A) Serial Mode and (B) Parallel or "Flash" Mode*

Notes

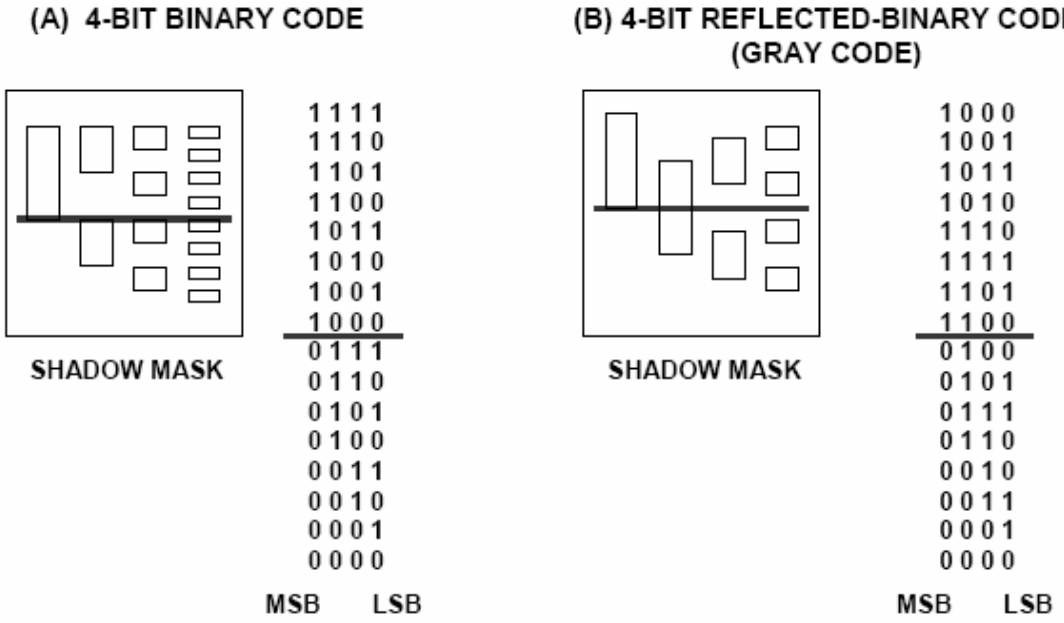


Figure 2.7: *Electron Beam Coder Shadow Masks for Binary Code (A) and Gray Code (B)*

Notes

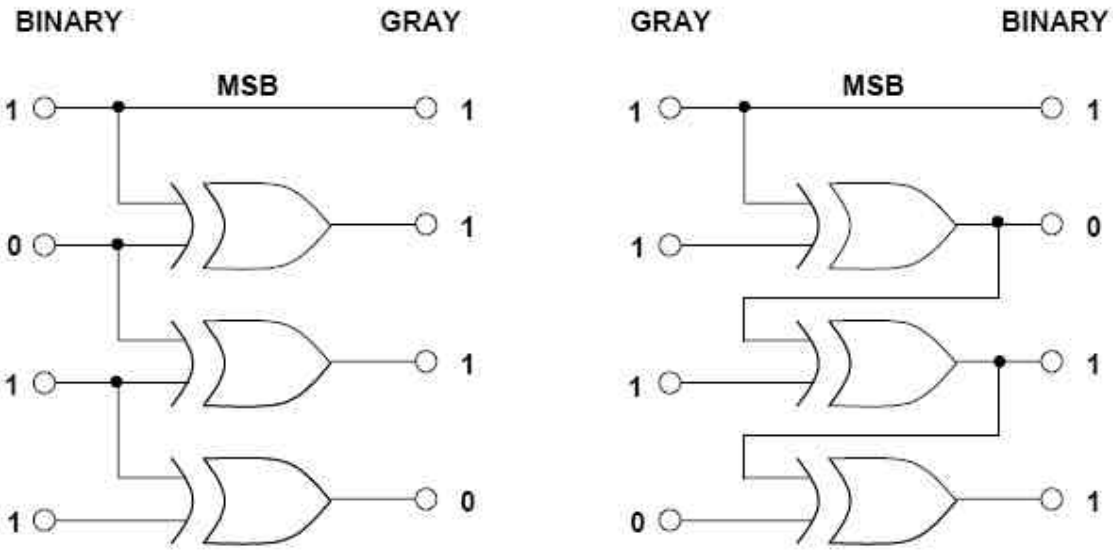
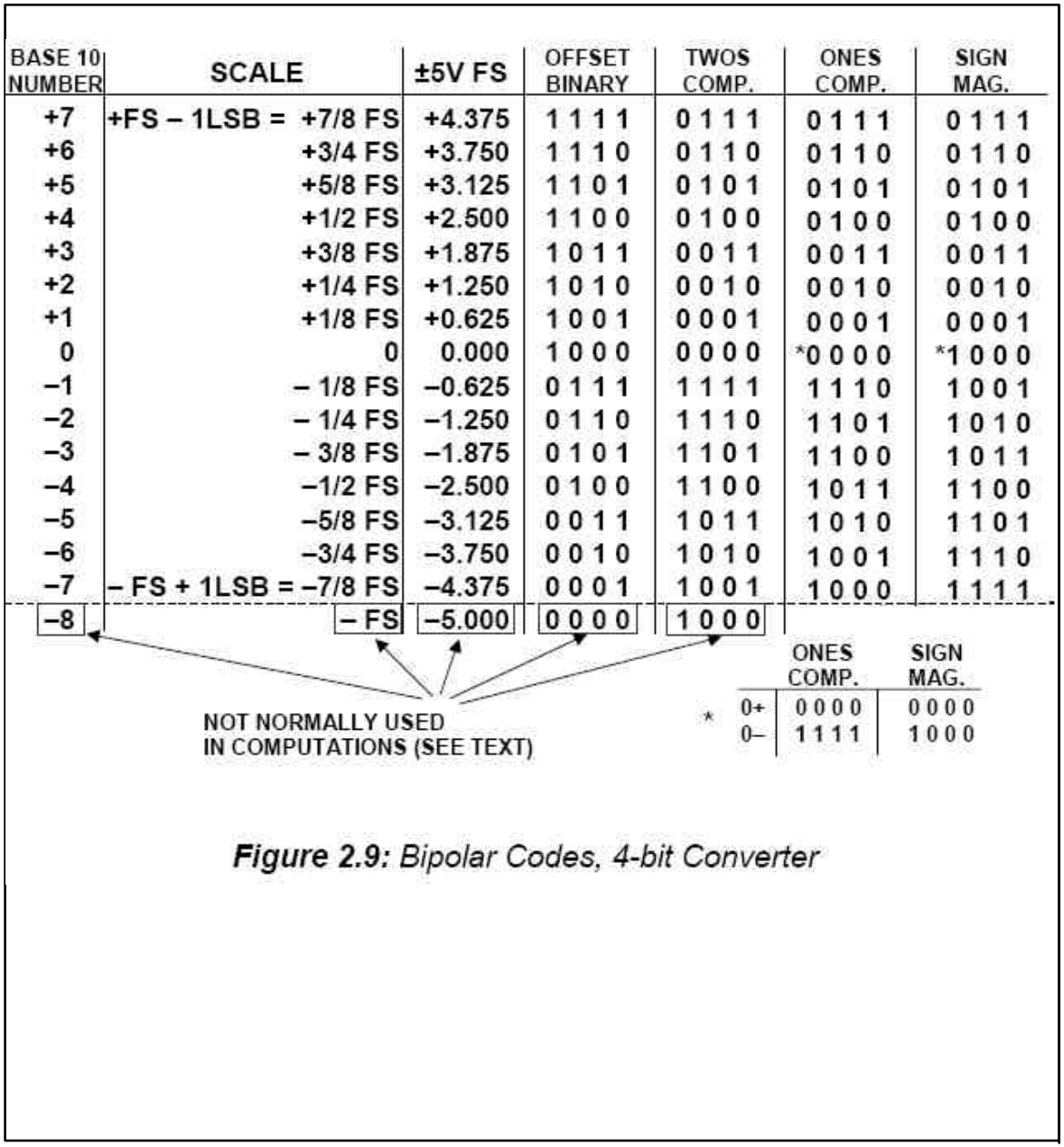


Figure 2.8: *Binary-to-Gray and Gray-to-Binary Conversion Using the Exclusive-Or Logic Function*

Notes

Notes



BASE 10 NUMBER	SCALE	±5V FS	OFFSET BINARY	TWOS COMP.	ONES COMP.	SIGN MAG.
+7	+FS – 1LSB = +7/8 FS	+4.375	1 1 1 1	0 1 1 1	0 1 1 1	0 1 1 1
+6	+3/4 FS	+3.750	1 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0
+5	+5/8 FS	+3.125	1 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1
+4	+1/2 FS	+2.500	1 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0
+3	+3/8 FS	+1.875	1 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1
+2	+1/4 FS	+1.250	1 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0
+1	+1/8 FS	+0.625	1 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1
0	0	0.000	1 0 0 0	0 0 0 0	*0 0 0 0	*1 0 0 0
–1	– 1/8 FS	–0.625	0 1 1 1	1 1 1 1	1 1 1 0	1 0 0 1
–2	– 1/4 FS	–1.250	0 1 1 0	1 1 1 0	1 1 0 1	1 0 1 0
–3	– 3/8 FS	–1.875	0 1 0 1	1 1 0 1	1 1 0 0	1 0 1 1
–4	–1/2 FS	–2.500	0 1 0 0	1 1 0 0	1 0 1 1	1 1 0 0
–5	–5/8 FS	–3.125	0 0 1 1	1 0 1 1	1 0 1 0	1 1 0 1
–6	–3/4 FS	–3.750	0 0 1 0	1 0 1 0	1 0 0 1	1 1 1 0
–7	– FS + 1LSB = –7/8 FS	–4.375	0 0 0 1	1 0 0 1	1 0 0 0	1 1 1 1
–8	– FS	–5.000	0 0 0 0	1 0 0 0		

NOT NORMALLY USED IN COMPUTATIONS (SEE TEXT)

*

	ONES COMP.	SIGN MAG.
0+	0 0 0 0	0 0 0 0
0–	1 1 1 1	1 0 0 0

Figure 2.9: *Bipolar Codes, 4-bit Converter*

Notes

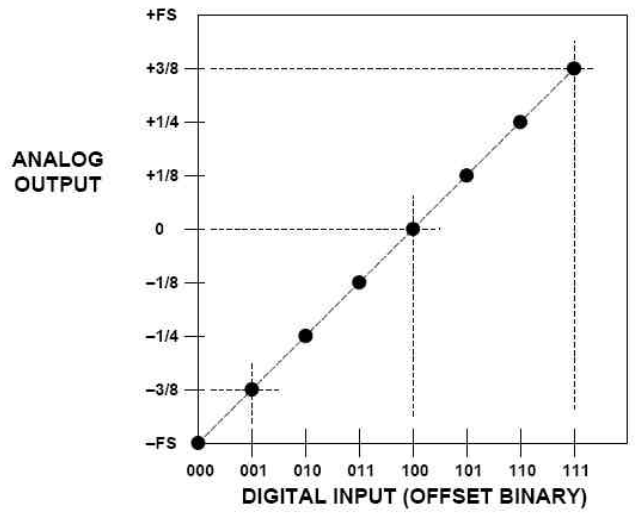


Figure 2.10: *Transfer Function for Ideal Bipolar 3-bit DAC*

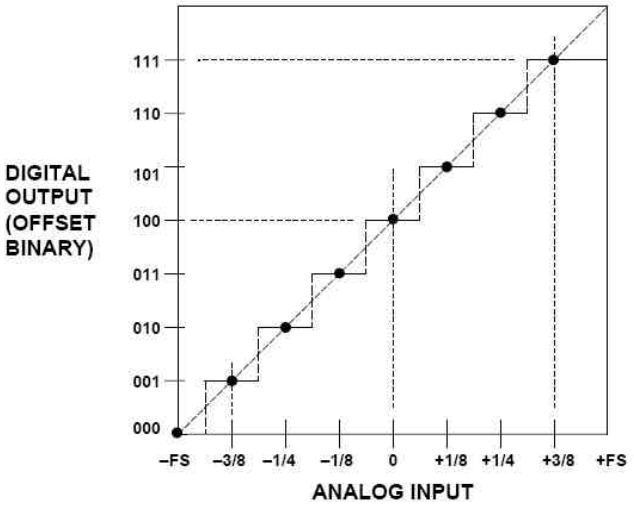


Figure 2.11: *Transfer Function for Ideal Bipolar 3-bit ADC*

To Convert From → / To ↓	Sign Magnitude	2's Complement	Offset Binary	1's Complement
Sign Magnitude	No Change	If MSB = 1, complement other bits, add 00…01	Complement MSB If new MSB = 1, complement other bits, add 00…01	If MSB = 1, complement other bits
2's Complement	If MSB = 1, complement other bits, add 00…01	No Change	Complement MSB	If MSB = 1, add 00…01
Offset binary	Complement MSB If new MSB = 0 complement other bits, add 00…01	Complement MSB	No Change	Complement MSB If new MSB = 0, add 00…01
1's Complement	If MSB = 1, complement other bits	If MSB = 1, add 11…11	Complement MSB If new MSB = 1, add 11…11	No Change

Figure 2.12: *Relationships Among Bipolar Codes*

Notes

BASE 10 NUMBER	SCALE	+10V FS	DECADE 1	DECADE 2	DECADE 3	DECADE 4
+15	+FS – 1LSB = +15/16 FS	9.375	1 0 0 1	0 0 1 1	0 1 1 1	0 1 0 1
+14	+7/8 FS	8.750	1 0 0 0	0 1 1 1	0 1 0 1	0 0 0 0
+13	+13/16 FS	8.125	1 0 0 0	0 0 0 1	0 0 1 0	0 1 0 1
+12	+3/4 FS	7.500	0 1 1 1	0 1 0 1	0 0 0 0	0 0 0 0
+11	+11/16 FS	6.875	0 1 1 0	1 0 0 0	0 1 1 1	0 1 0 1
+10	+5/8 FS	6.250	0 1 1 0	0 0 1 0	0 1 0 1	0 0 0 0
+9	+9/16 FS	5.625	0 1 0 1	0 1 1 0	0 0 1 0	0 1 0 1
+8	+1/2 FS	5.000	0 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0
+7	+7/16 FS	4.375	0 1 0 0	0 0 1 1	0 1 1 1	0 1 0 1
+6	+3/8 FS	3.750	0 0 1 1	0 1 1 1	0 1 0 1	0 0 0 0
+5	+5/16 FS	3.125	0 0 1 1	0 0 0 1	0 0 1 0	0 1 0 1
+4	+1/4 FS	2.500	0 0 1 0	0 1 0 1	0 0 0 0	0 0 0 0
+3	+3/16 FS	1.875	0 0 0 1	1 0 0 0	0 1 1 1	0 1 0 1
+2	+1/8 FS	1.250	0 0 0 1	0 0 1 0	0 1 0 1	0 0 0 0
+1	1LSB = +1/16 FS	0.625	0 0 0 0	0 1 1 0	0 0 1 0	0 1 0 1
0	0	0.000	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Figure 2.13: *Binary Coded Decimal (BCD) Code*

Notes

RESOLUTION N	2^N	VOLTAGE (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	– 12
4-bit	16	625 mV	62,500	6.25	– 24
6-bit	64	156 mV	15,625	1.56	– 36
8-bit	256	39.1 mV	3,906	0.39	– 48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	– 60
12-bit	4,096	2.44 mV	244	0.024	– 72
14-bit	16,384	610 µV	61	0.0061	– 84
16-bit	65,536	153 µV	15	0.0015	– 96
18-bit	262,144	38 µV	4	0.0004	– 108
20-bit	1,048,576	9.54 µV (10 µV)	1	0.0001	– 120
22-bit	4,194,304	2.38 µV	0.24	0.000024	– 132
24-bit	16,777,216	596 nV*	0.06	0.000006	– 144

*600nV is the Johnson Noise in a 10kHz BW of a 2.2kΩ Resistor @ 25°C

Remember: 10-bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%.
All other values may be calculated by powers of 2.

Figure 2.14: *Quantization: The Size of a Least Significant Bit (LSB)*

Notes

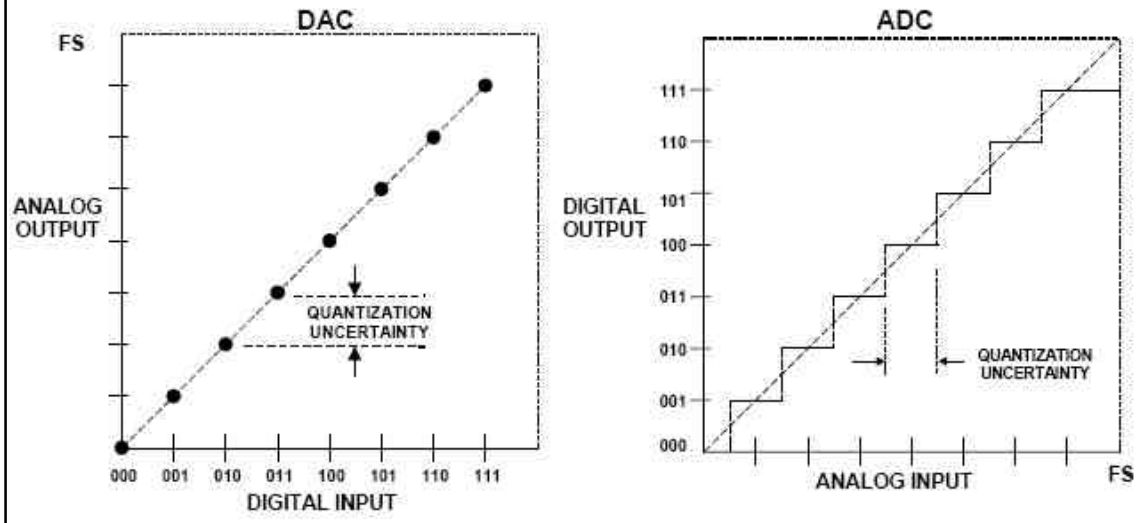


Figure 2.15: *Transfer Functions for Ideal 3-Bit DAC and ADC*

Notes

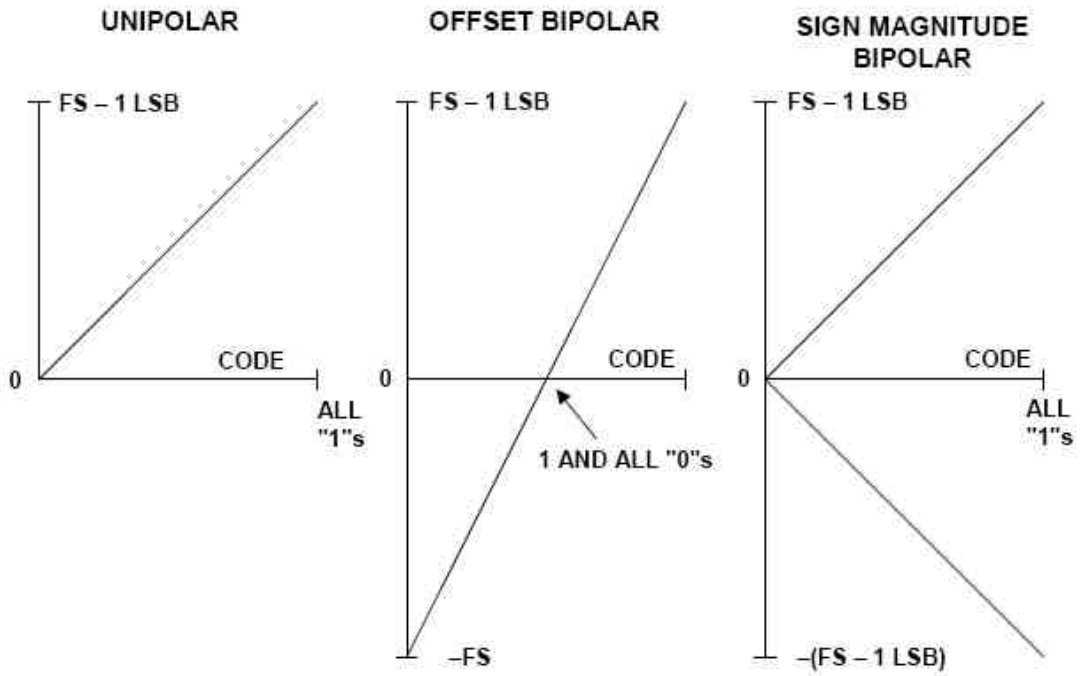


Figure 2.16: *Unipolar and Bipolar Converters*

Notes

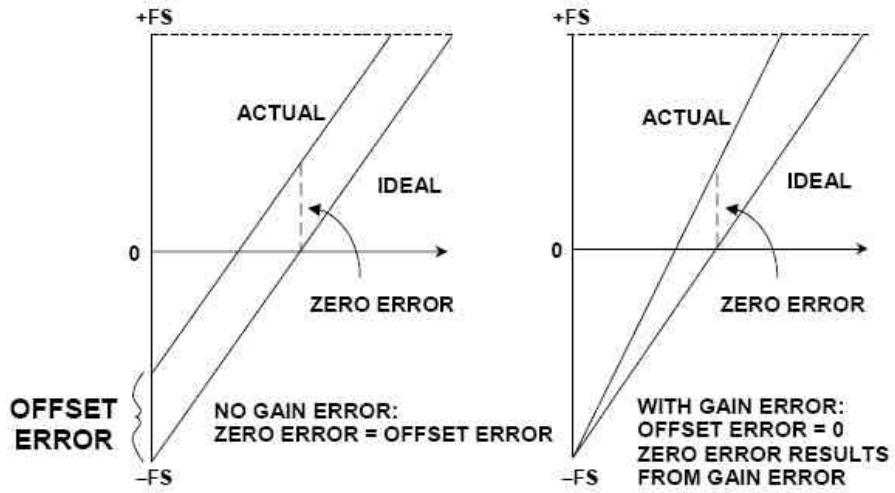


Figure 2.17: *Bipolar Data Converter Offset and Gain Error*

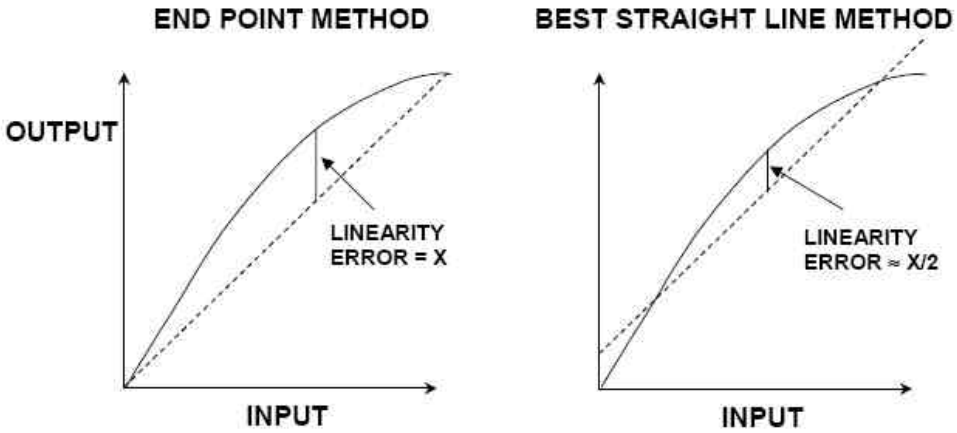


Figure 2.18: *Method of Measuring Integral Linearity Errors (Same Converter on Both Graphs)*

Notes

Notes

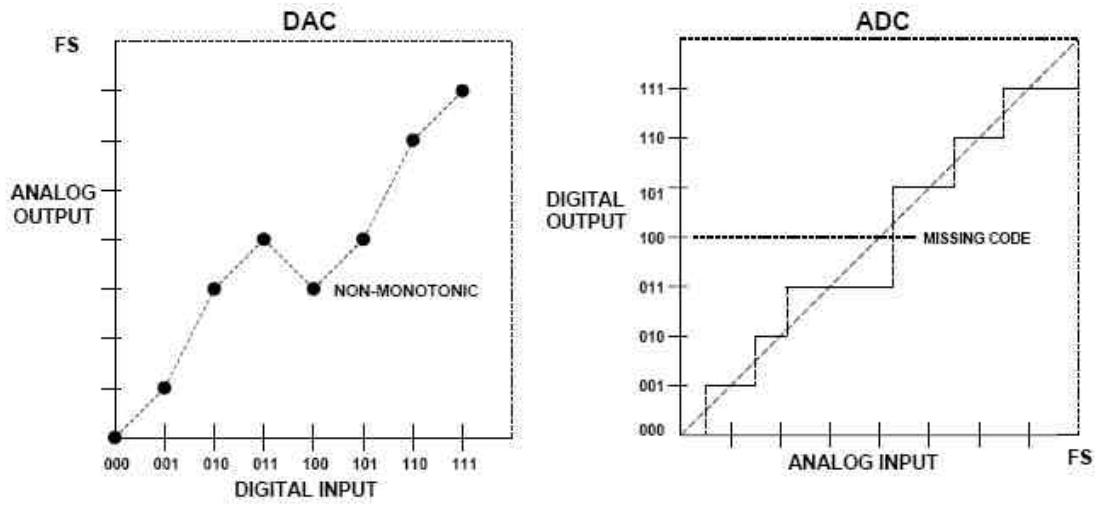


Figure 2.19: *Transfer Functions for Non-Ideal 3-Bit DAC and ADC*

Notes

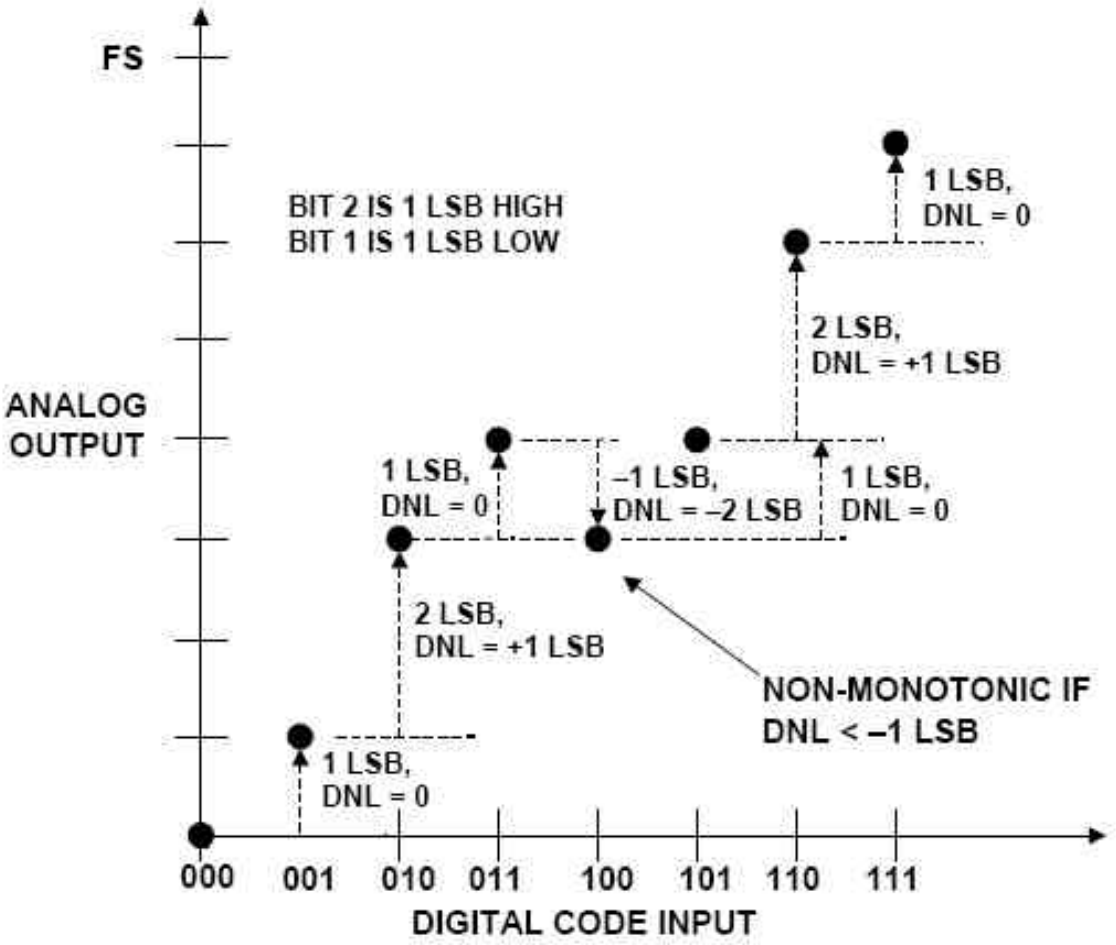


Figure 2.20: *Details of DAC Differential Nonlinearity*

Notes

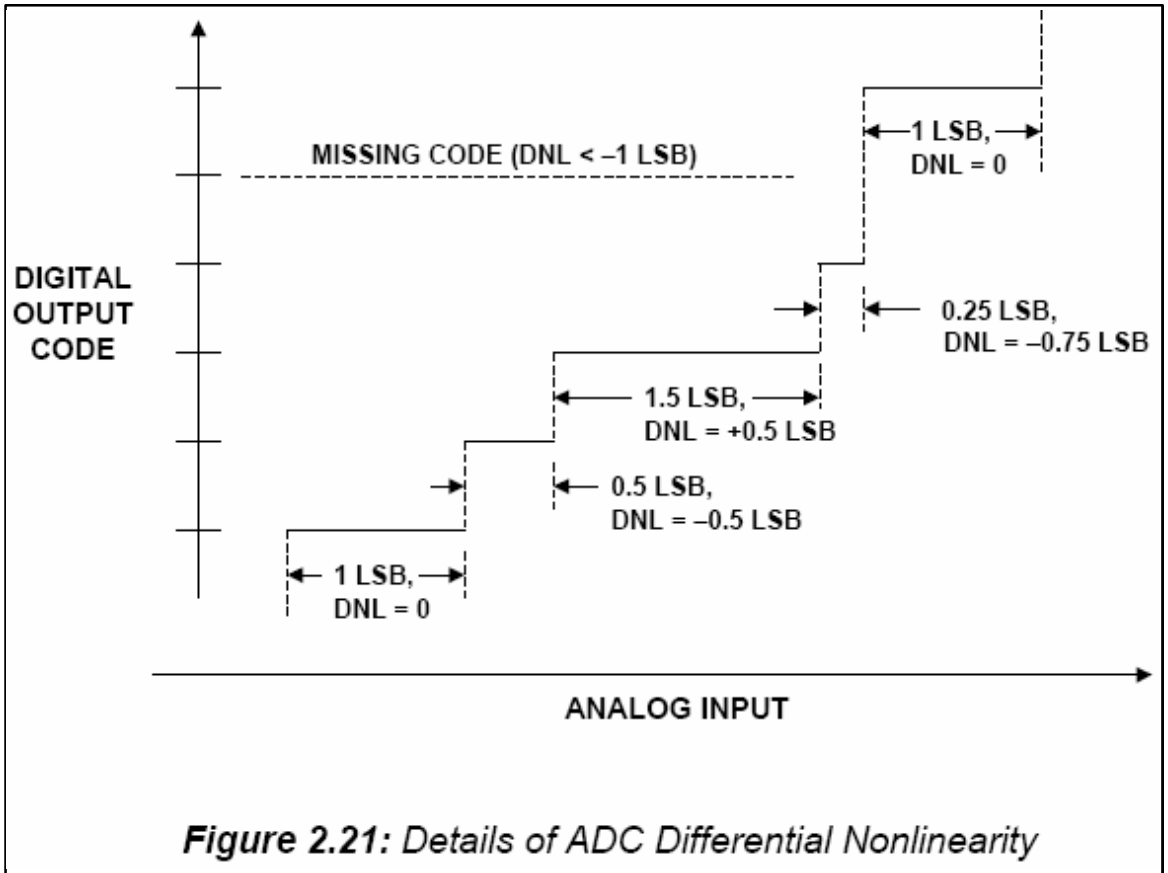


Figure 2.21: *Details of ADC Differential Nonlinearity*

Notes

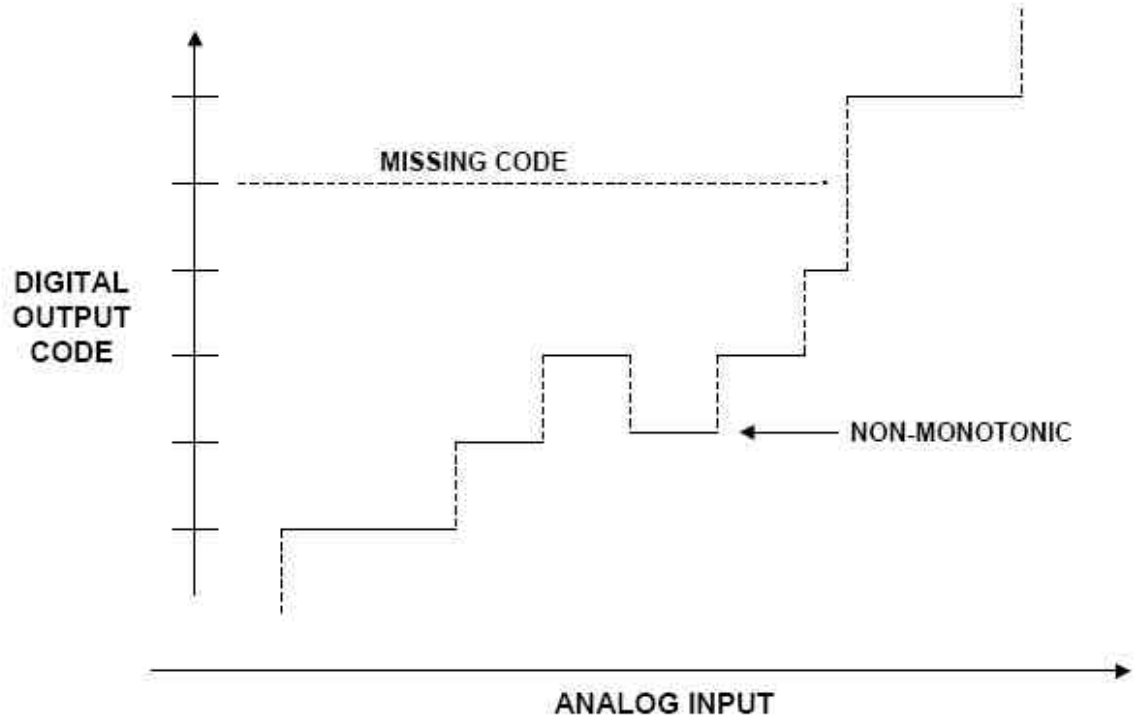


Figure 2.22: *Non-Monotonic ADC with Missing Code*

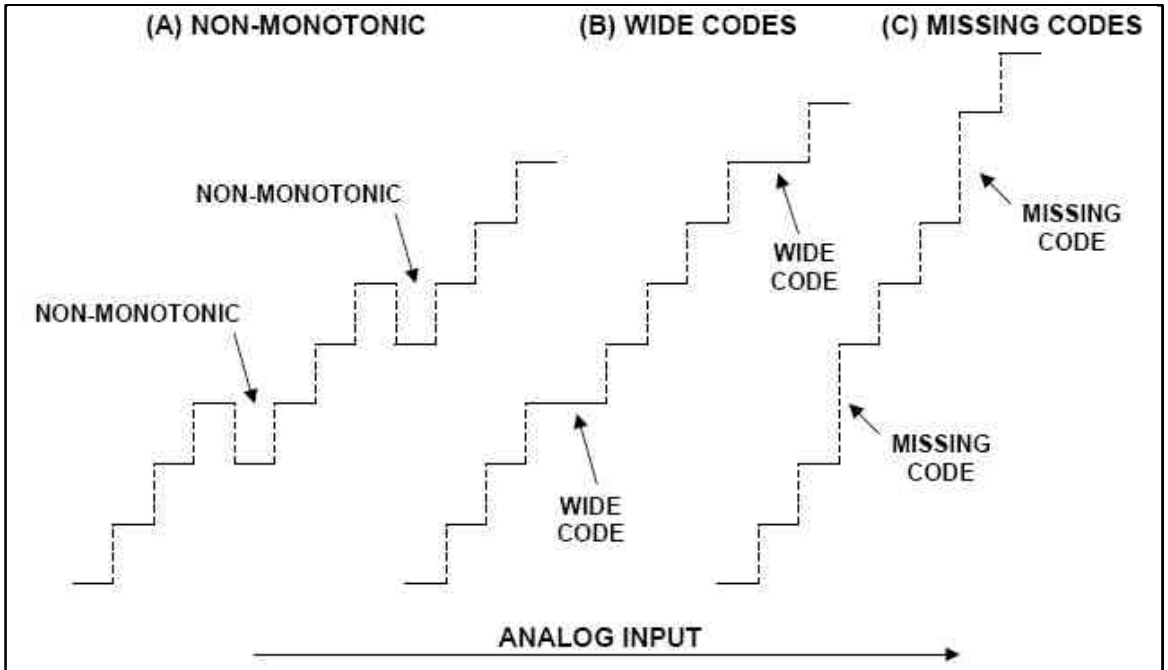


Figure 2.23: *Errors Associated with Improperly Trimmed Subranging ADC*

Notes

Notes

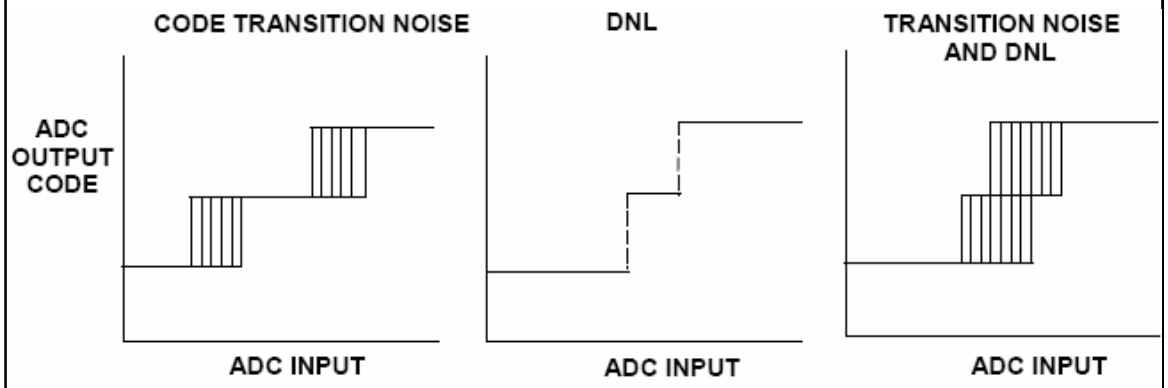


Figure 2.24: *Combined Effects of Code Transition Noise and DNL*

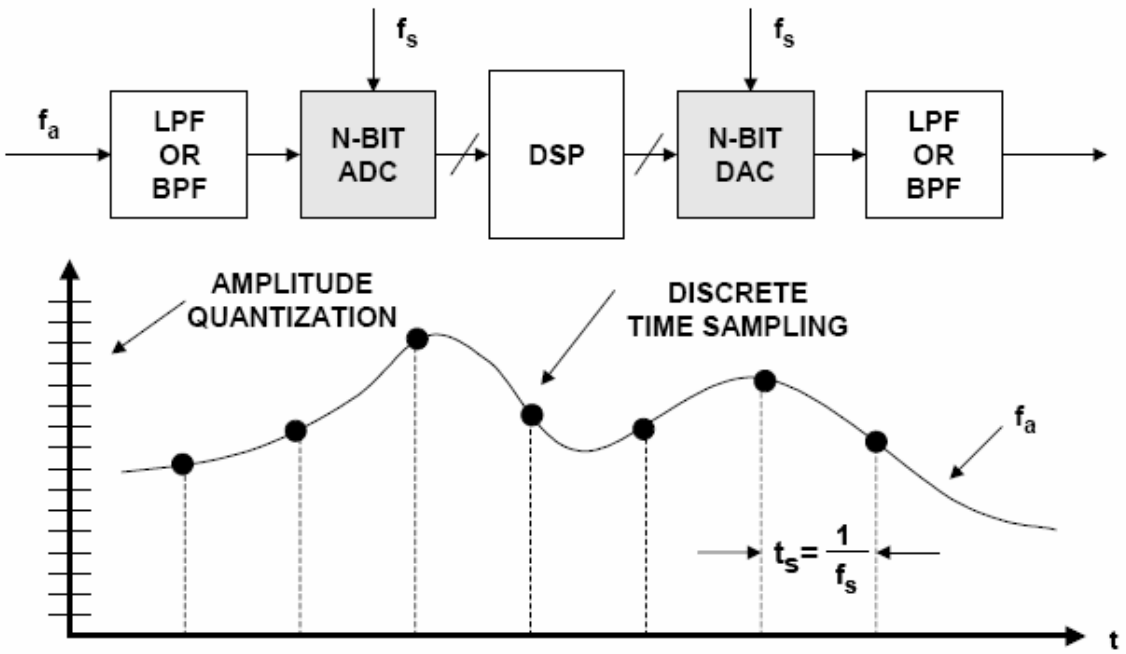


Figure 2.25: *Sampled Data System*

Notes

Notes

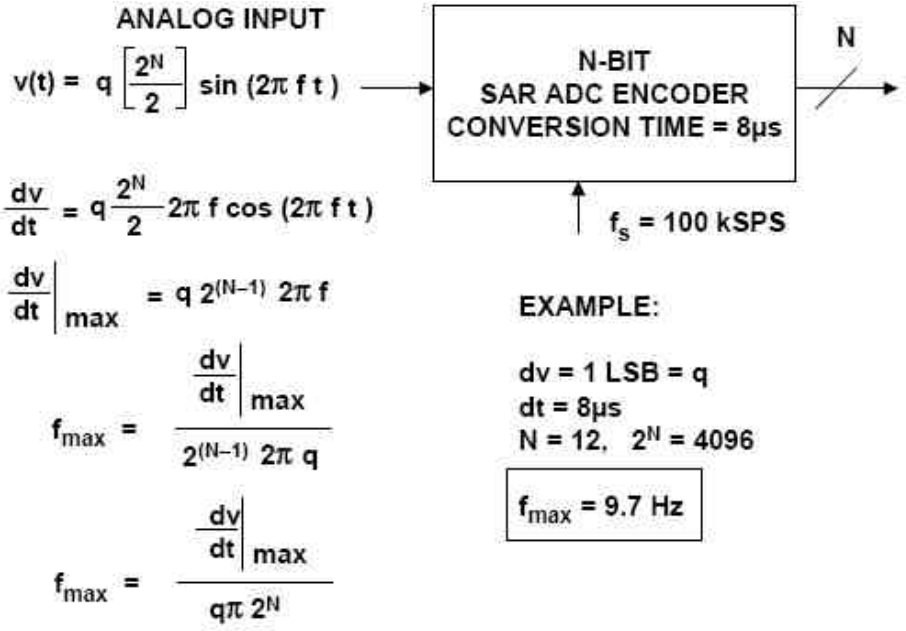


Figure 2.26: *Input Frequency Limitations of Non-Sampling ADC (Encoder)*

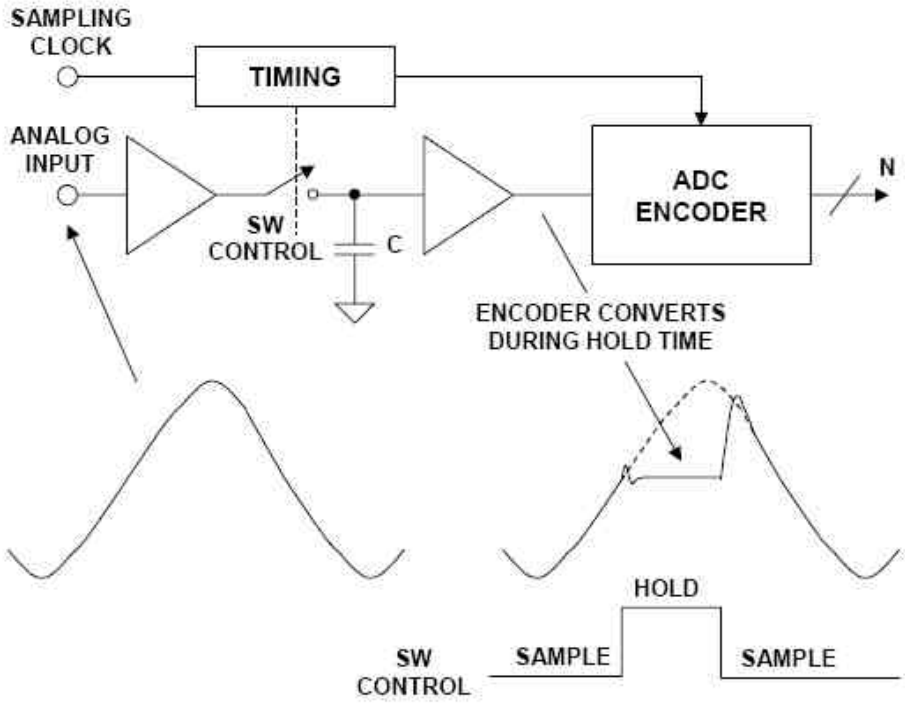


Figure 2.27: *Sample-and-Hold Function Required for Digitizing AC Signals*

Notes

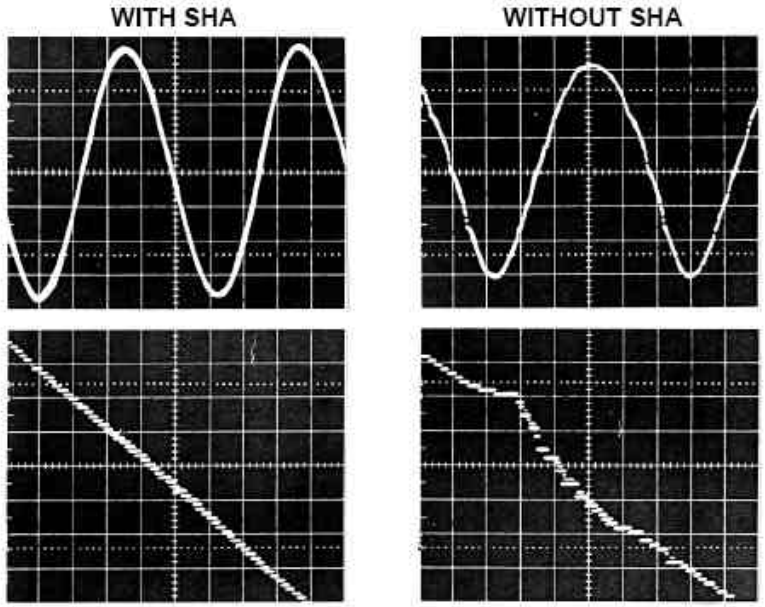


Figure 2.28: *8-bit, 20-MSPS Flash ADC With and Without Sample-and-Hold*

Notes

- A signal with a *maximum frequency* f_a must be sampled at a rate $f_s > 2f_a$ or information about the signal will be lost because of aliasing.
- Aliasing occurs whenever $f_s < 2f_a$
- The concept of aliasing is widely used in communications applications such as direct IF-to-digital conversion.
- A signal which has frequency components between f_a and f_b must be sampled at a rate $f_s > 2\,(f_b - f_a)$ in order to prevent alias components from overlapping the signal frequencies.

Figure 2.29: *Nyquist's Criteria*

Notes

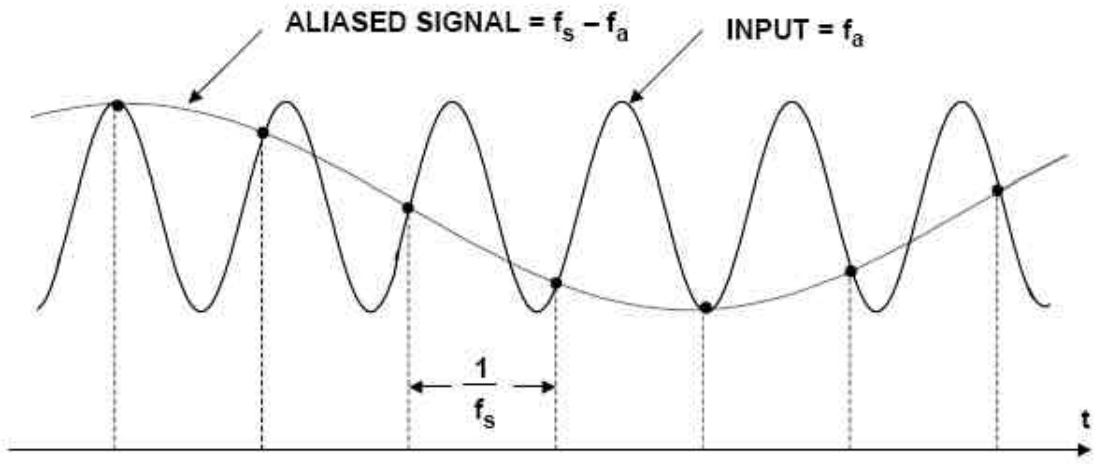


Figure 2.30: *Aliasing in the Time Domain*

Notes

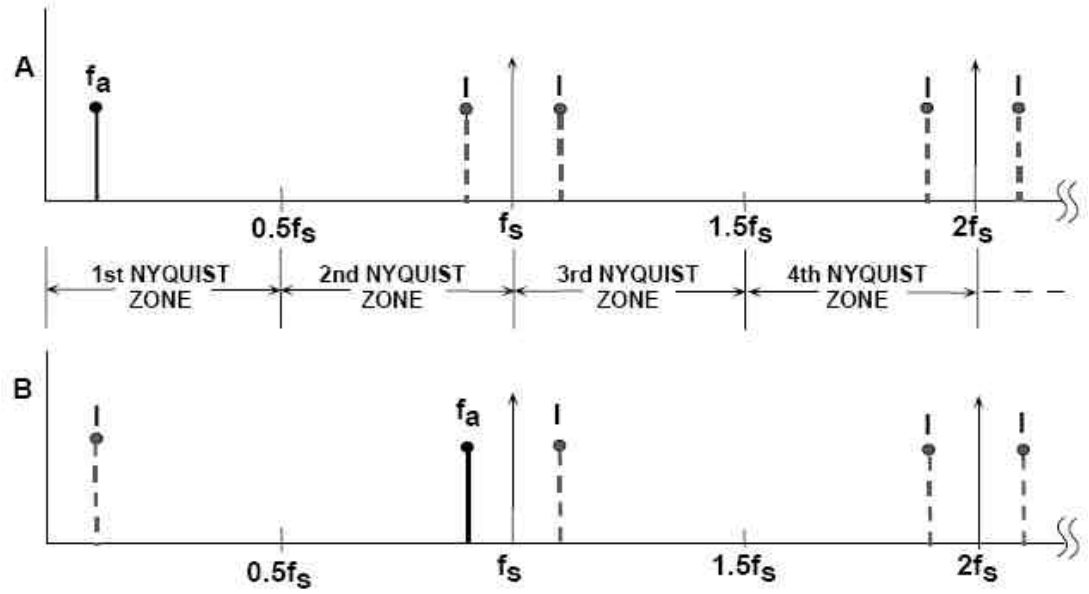


Figure 2.31: *Analog Signal f_a Sampled @ f_s Using Ideal Sampler Has Images (Aliases) at $|\pm Kf_s \pm f_a|$, K = 1, 2, 3, . . .*

Notes

Notes

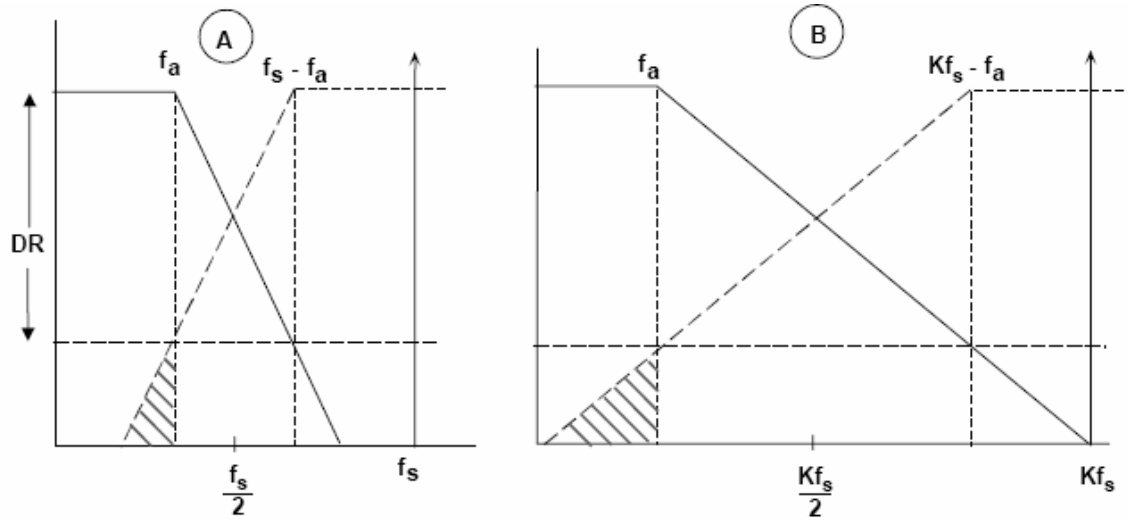
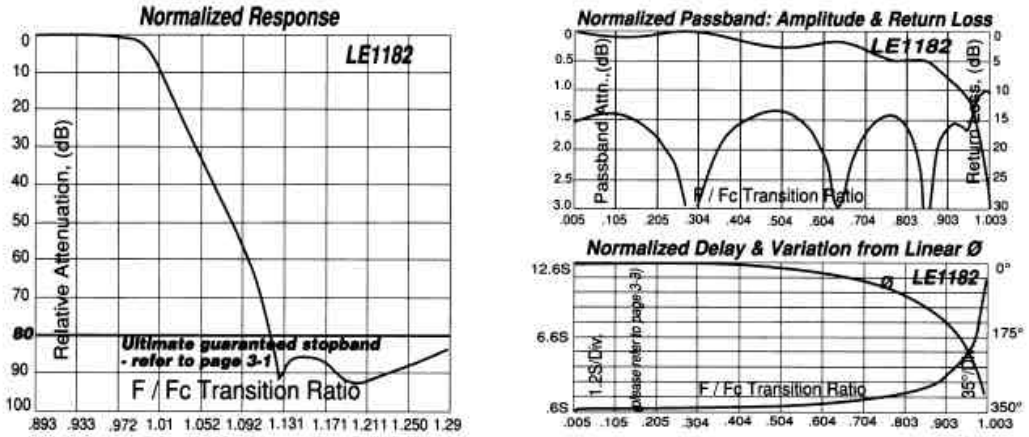


Figure 2.32: *Oversampling Relaxes Requirements on Baseband Antialiasing Filter*

Notes



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http://www.tte.com

Figure 2.33: *Characteristics of 11-Pole Elliptical Filter (TTE, Inc., LE1182-Series)*

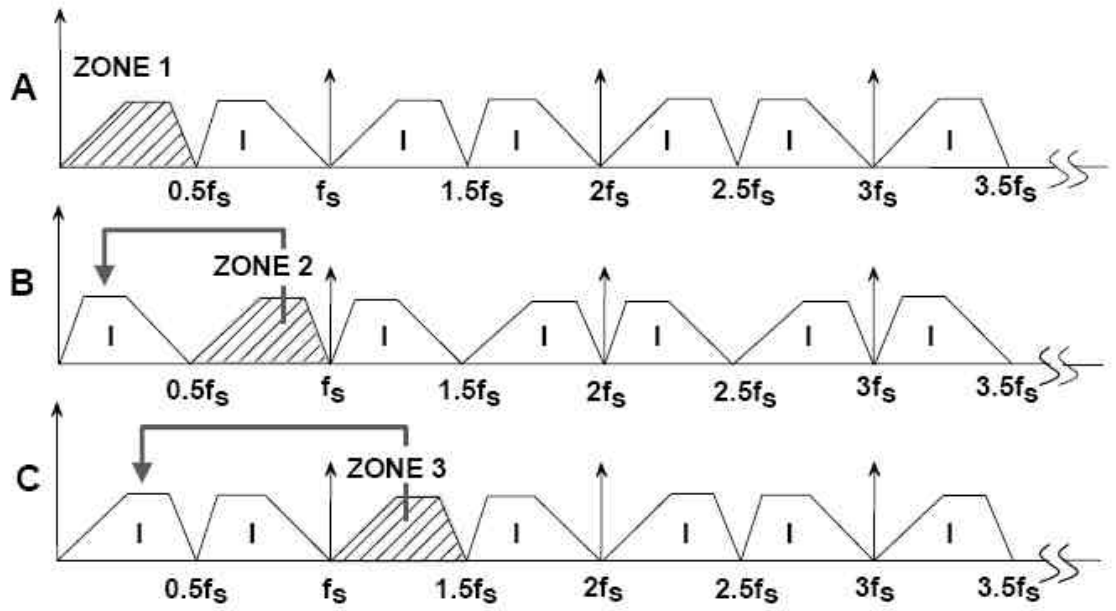
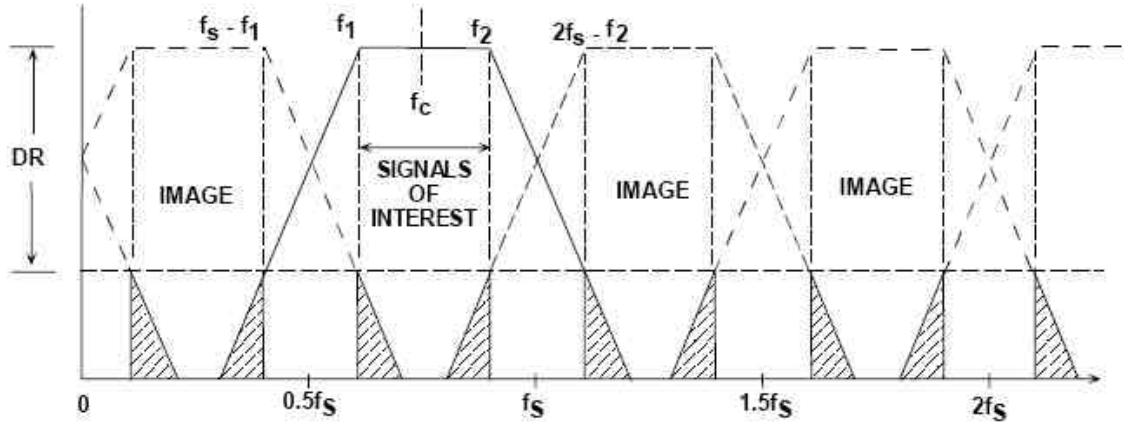


Figure 2.34: *Undersampling and Frequency Translation Between Nyquist Zones*

Notes



BANDPASS FILTER SPECIFICATIONS:
- STOPBAND ATTENUATION = DR
- TRANSITION BAND: f_2 TO $2f_s - f_2$
  f_1 TO $f_s - f_1$
- CORNER FREQUENCIES: f_1, f_2

Figure 2.35: *Antialiasing Filter for Undersampling*

Notes

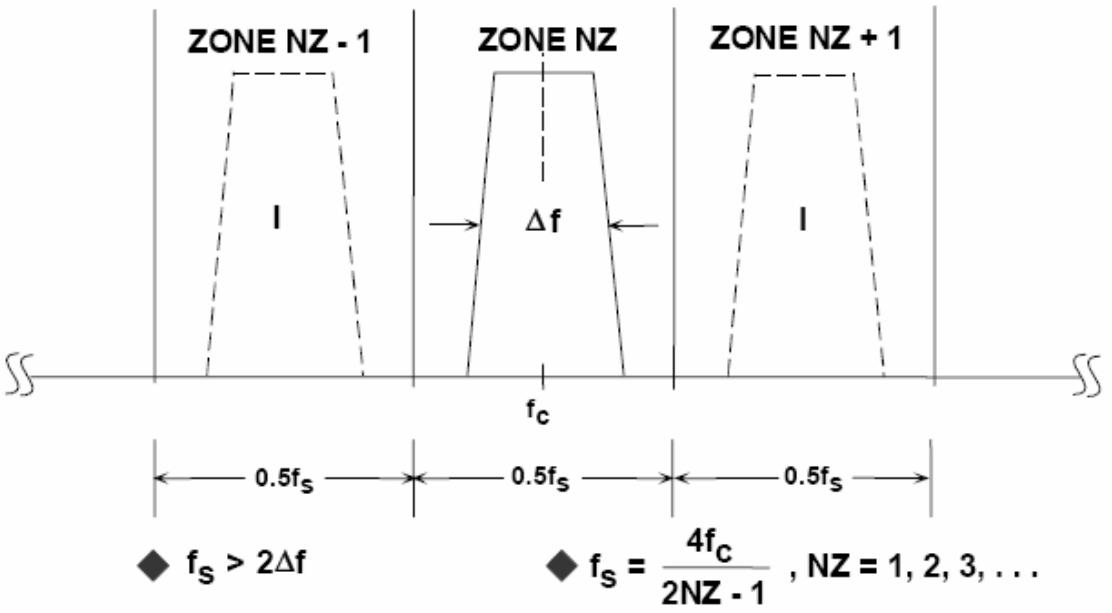


Figure 2.36: *Centering an Undersampled Signal within a Nyquist Zone*

Notes

Notes

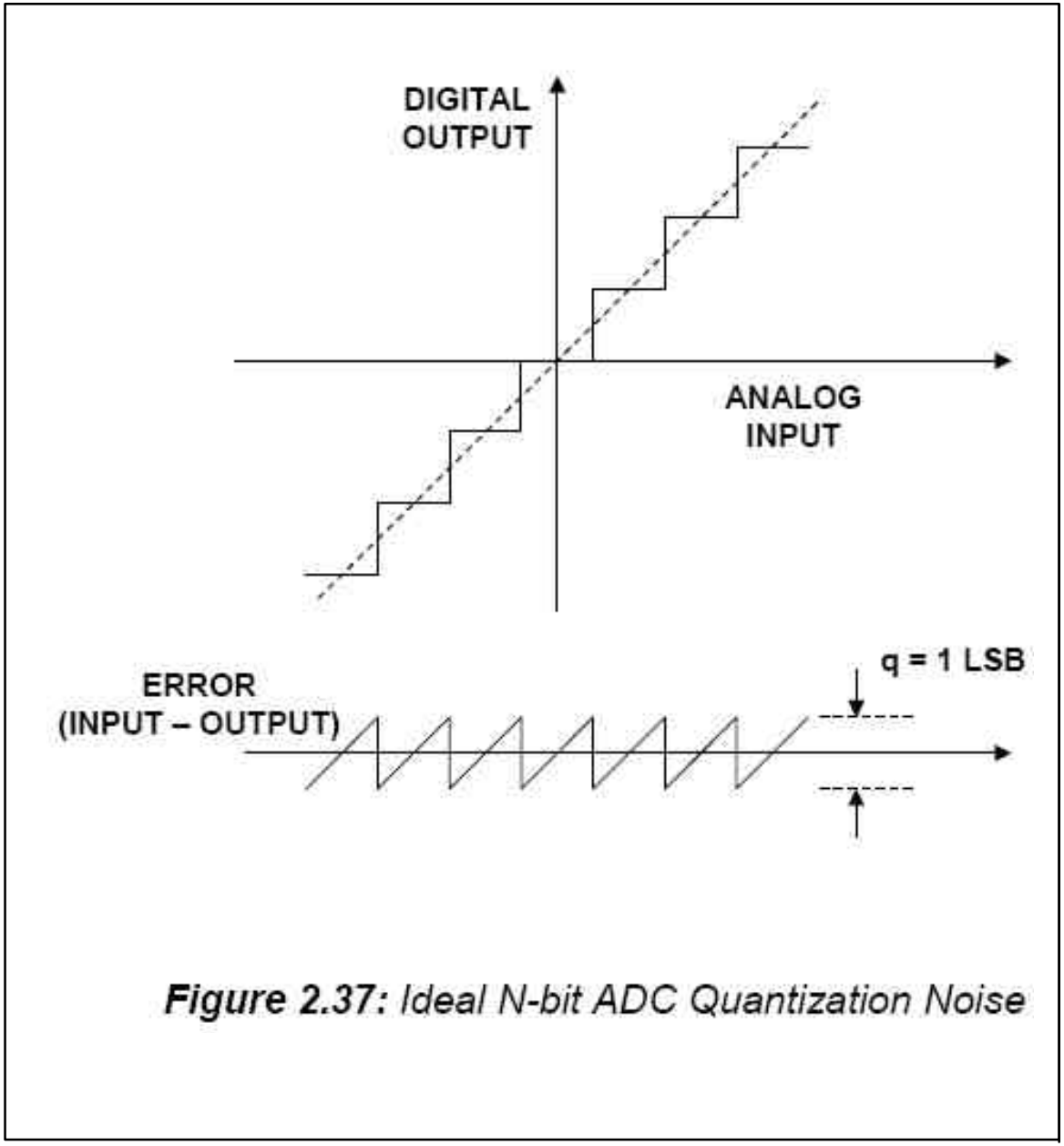
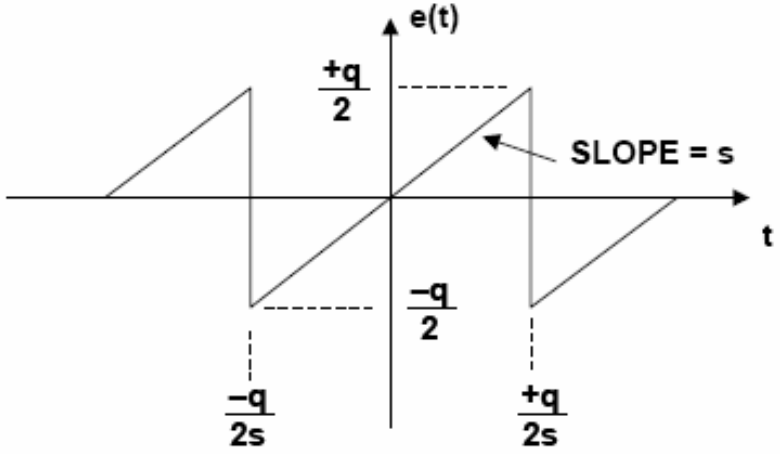


Figure 2.37: *Ideal N-bit ADC Quantization Noise*

Notes



- ERROR = $e(t) = st, \quad \frac{-q}{2s} < t < \frac{+q}{2s}$
- MEAN-SQUARE ERROR = $\overline{e^2(t)} = \frac{s}{q} \int_{-q/2s}^{+q/2s} (st)^2 \, dt = \frac{q^2}{12}$
- ROOT-MEAN-SQUARE ERROR = $\sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}}$

Figure 2.38: *Quantization Noise as a Function of Time*

Notes

- FS INPUT = $v(t) = \left[\frac{q\,2^N}{2}\right] \sin(2\pi f t)$
- RMS Value of FS Sinewave = $\frac{q\,2^N}{2\sqrt{2}}$
- RMS Value of Quantization Noise = $\frac{q}{\sqrt{12}}$
- SNR = $20 \log_{10} \left[\frac{\text{RMS Value of FS Sinewave}}{\text{RMS Value of Quantization Noise}}\right] = 20 \log_{10} 2^N + 20 \log_{10} \sqrt{\frac{3}{2}}$

SNR = 6.02N + 1.76dB

(Measured over the Nyquist Bandwidth : DC to $f_S/2$)

Figure 2.39: *Theoretical Signal-to-Quantization Noise Ratio of an Ideal N-Bit Converter*

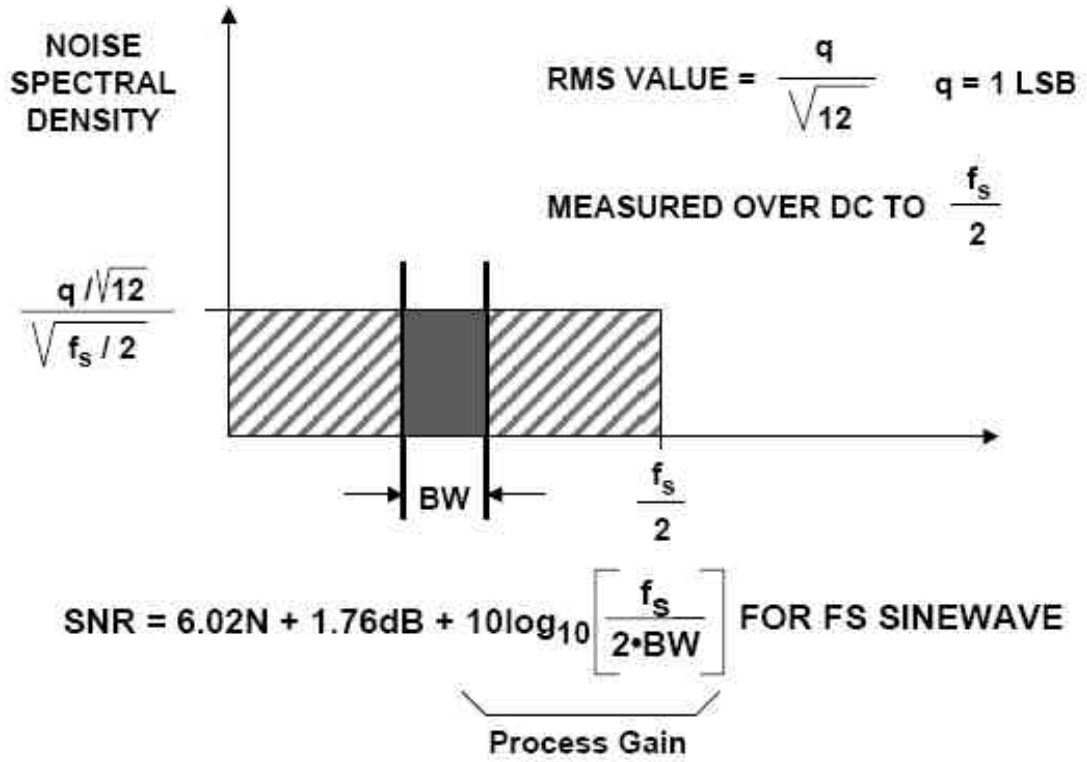


Figure 2.40: *Quantization Noise Spectrum*

Notes

Notes

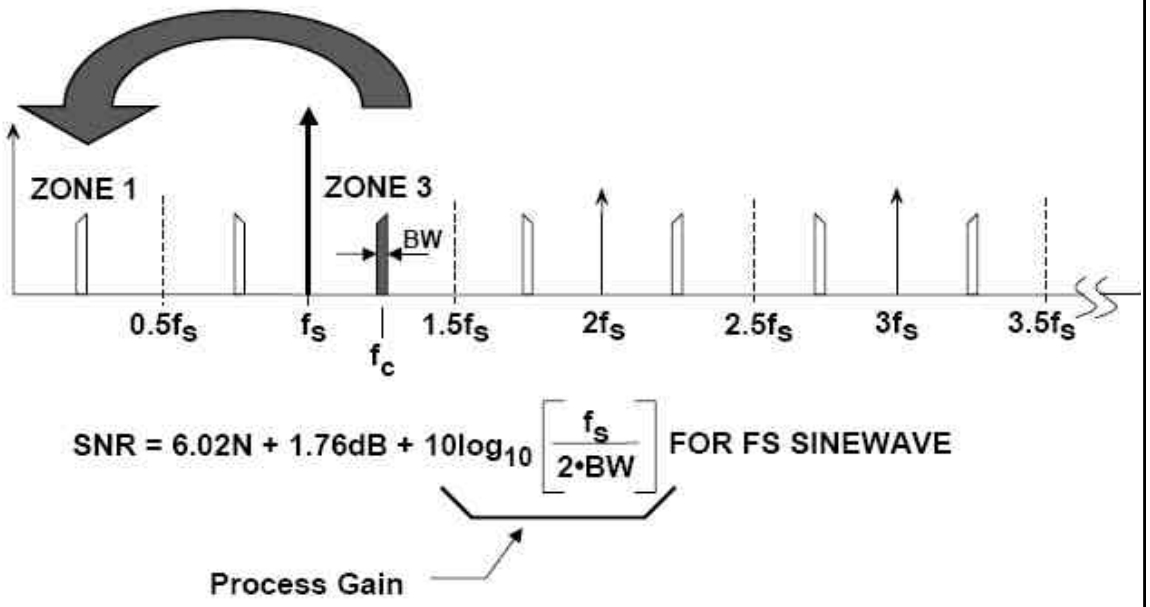


Figure 2.41: *Undersampling and Oversampling Combined Results in Process Gain*

Notes

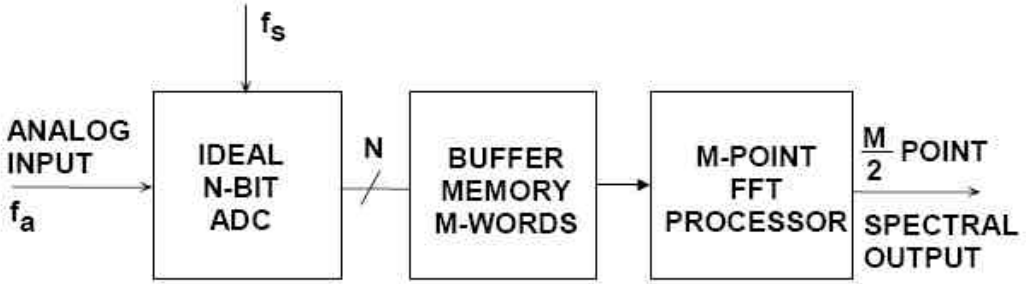


Figure 2.42: *Dynamic Performance Analysis of an Ideal N-bit ADC*

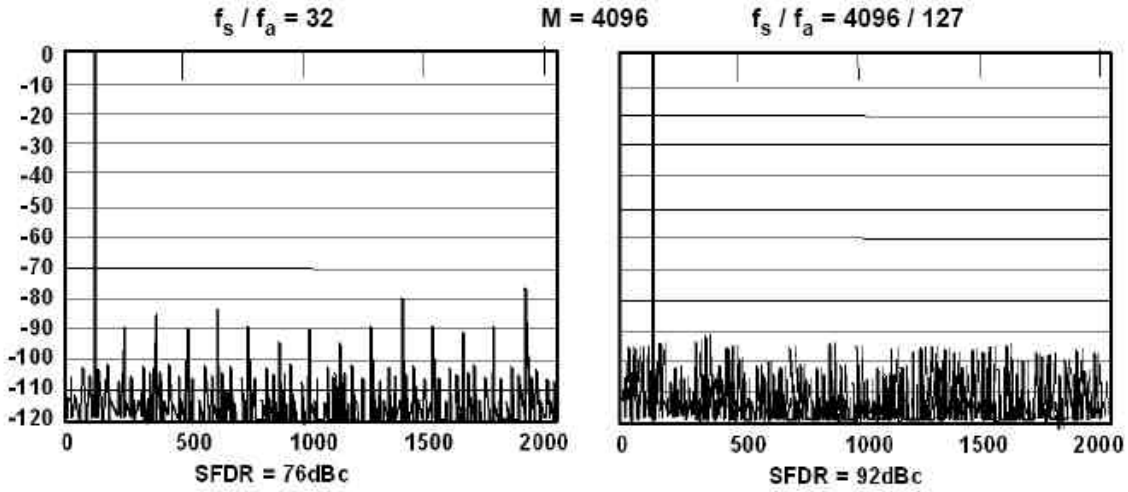


Figure 2.43: *Effect of Ratio of Sampling Clock to Input Frequency on SFDR for Ideal 12-bit ADC*

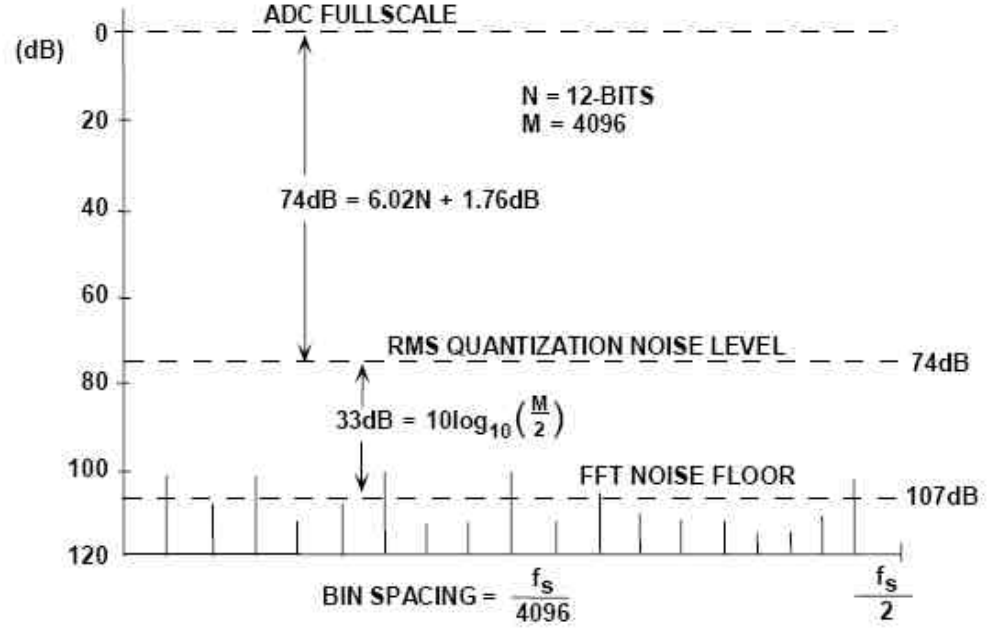


Figure 2.44: *Noise Floor for an Ideal 12-bit ADC Using 4096-point FFT*

Notes

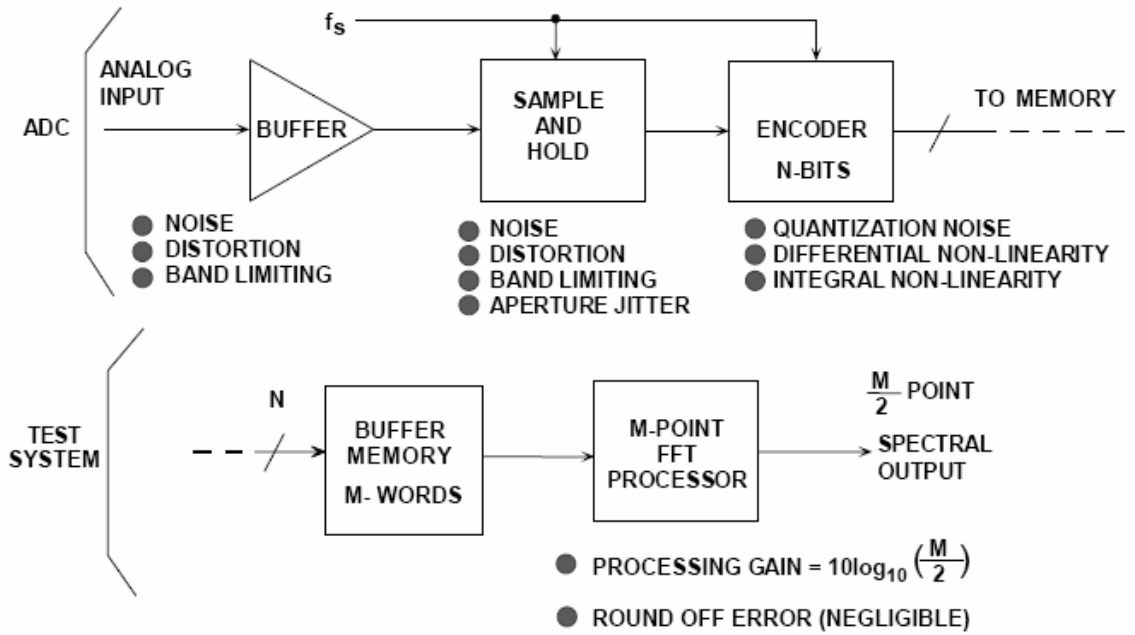


Figure 2.45: *ADC Model Showing Noise and Distortion Sources*

Notes

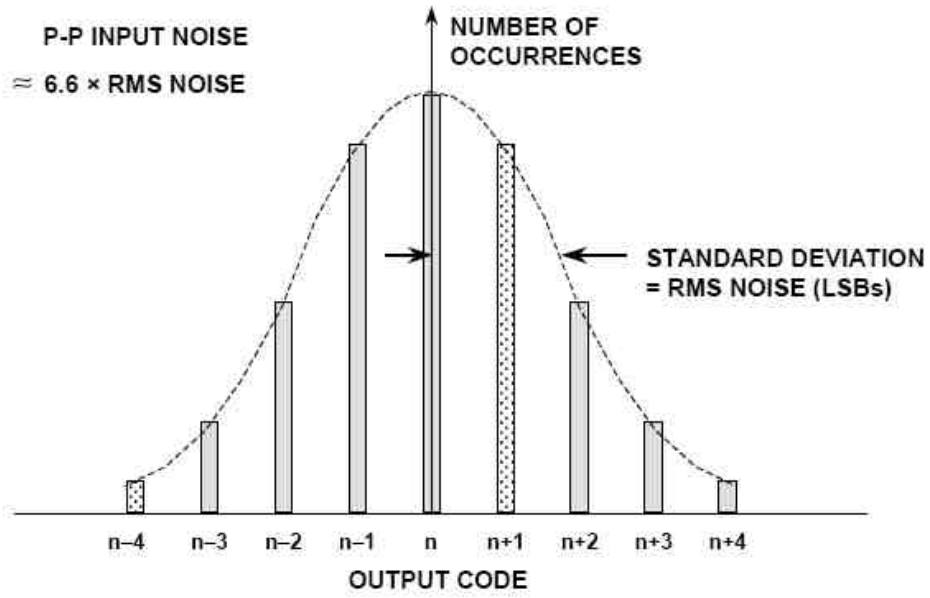


Figure 2.46: *Effect of Input-Referred Noise on ADC "Grounded Input" Histogram*

Notes

Notes

- Effective Input Noise = $e_{n\ rms}$
- Peak-to-Peak Input Noise = $6.6\ e_{n\ rms}$
- Noise-Free Code Resolution $= \log_2 \left[\dfrac{\text{Peak-to-Peak Input Range}}{\text{Peak-to-Peak Input Noise}} \right]$

$$= \log_2 \left[\frac{2^N}{\text{Peak-to-Peak Input Noise (LSBs)}} \right]$$

- "Effective Resolution" $= \log_2 \left[\dfrac{\text{Peak-to-Peak Input Range}}{\text{RMS Input Noise}} \right]$

$$= \log_2 \left[\frac{2^N}{\text{RMS Input Noise (LSBs)}} \right]$$

$$= \text{Noise-Free Code Resolution} + 2.7 \text{ bits}$$

Figure 2.47: *Calculating Noise-Free (Flicker-Free) Code Resolution from Input-Referred Noise*

- Harmonic Distortion
- Worst Harmonic
- Total Harmonic Distortion (THD)
- Total Harmonic Distortion Plus Noise (THD + N)
- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N +D)
- Effective Number of Bits (ENOB)
- Signal-to-Noise Ratio (SNR)
- Analog Bandwidth (Full-Power, Small-Signal)
- Spurious Free Dynamic Range (SFDR)
- Two-Tone Intermodulation Distortion
- Multi-tone Intermodulation Distortion
- Noise Power Ratio (NPR)
- Adjacent Channel Leakage Ratio (ACLR)
- Noise Figure
- Settling Time, Overvoltage Recovery Time

Figure 2.48: *Quantifying Data Converter Dynamic Performance*

Notes

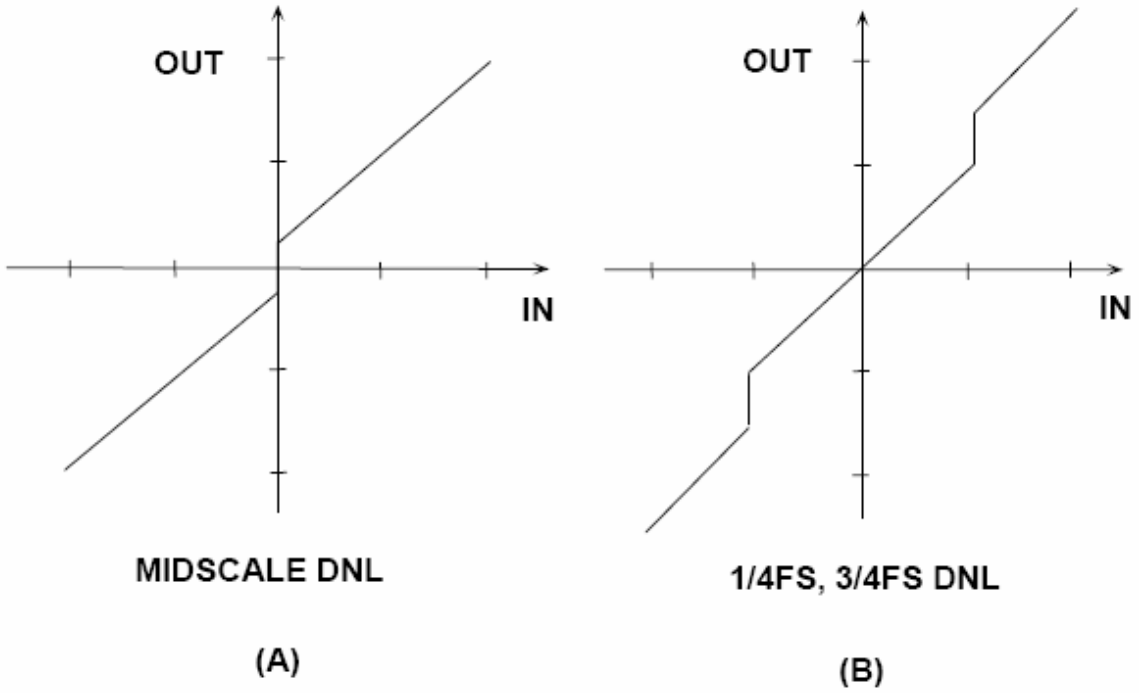


Figure 2.49: *Typical ADC/ DAC DNL Errors (Exaggerated)*

Notes

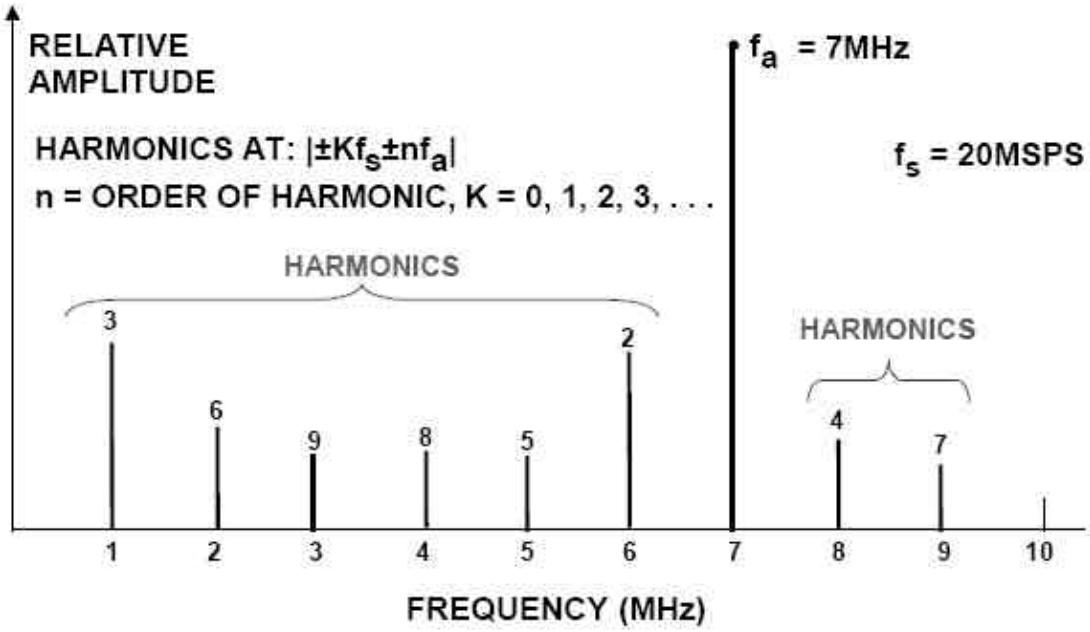


Figure 2.50: *Location of Distortion Products: Input Signal = 7 MHz, Sampling Rate = 20 MSPS*

Notes

- **SINAD (Signal-to-Noise-and-Distortion Ratio):**
  - The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding DC.

- **ENOB (Effective Number of Bits):**

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}$$

- **SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio Without Harmonics:**
  - The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first 5 harmonics and DC

Figure 2.51: *SINAD, ENOB, and SNR*

Notes

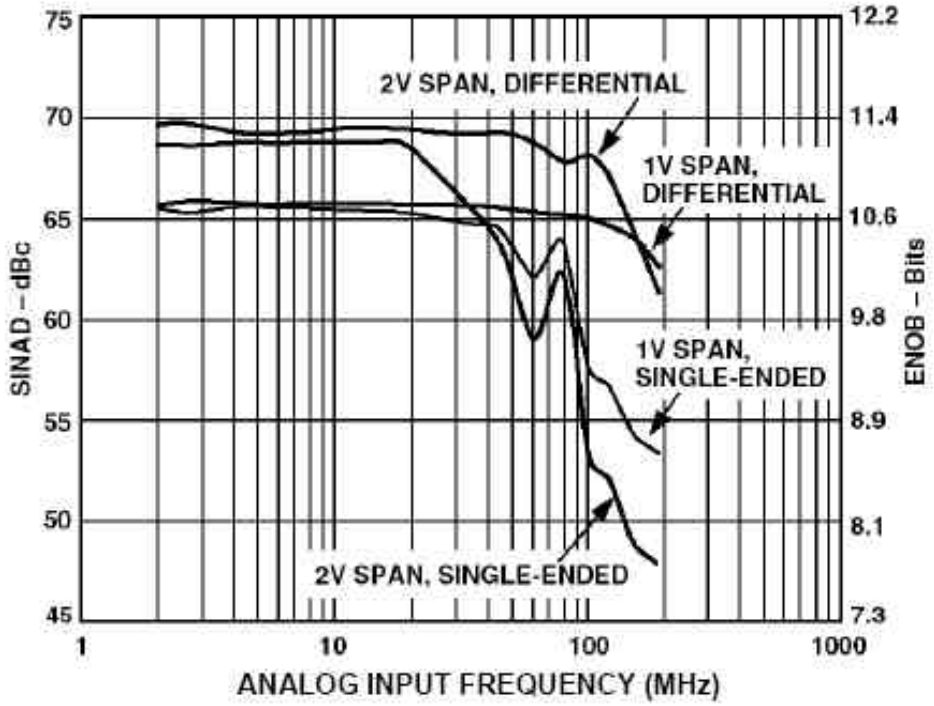


Figure 2.52: *AD9226 12-bit, 65-MSPS ADC SINAD and ENOB for Various Input Full-Scale Spans (Range)*

Notes

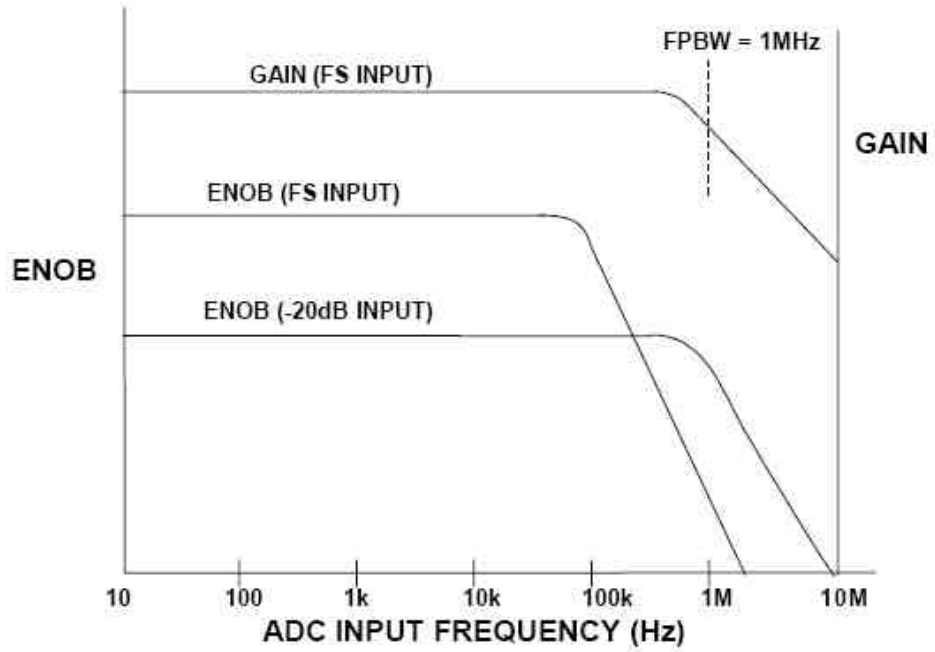


Figure 2.53: *ADC Gain (Bandwidth) and ENOB Versus Frequency Shows Importance of ENOB Specification*

Notes

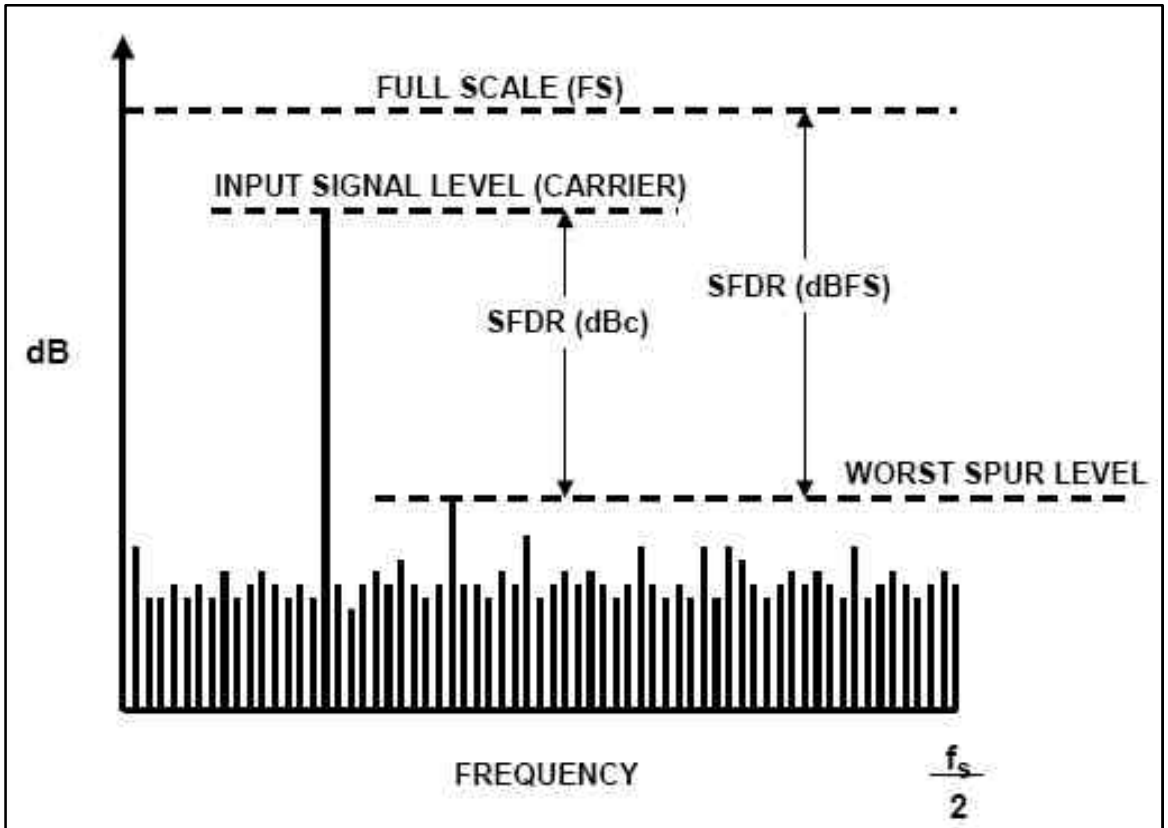


Figure 2.54: *Spurious Free Dynamic Range (SFDR)*

Notes

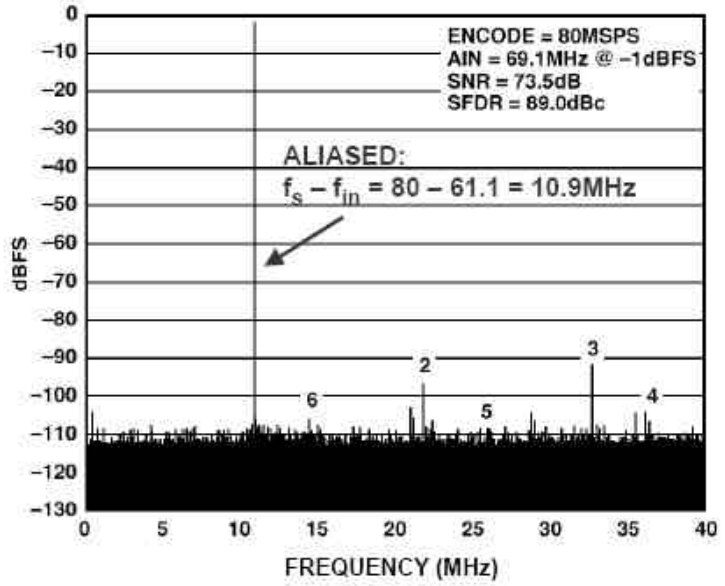


Figure 2.55: *AD6645 14-bit, 80-/105-MSPS ADC SFDR for 69.1-MHz Input*

Notes

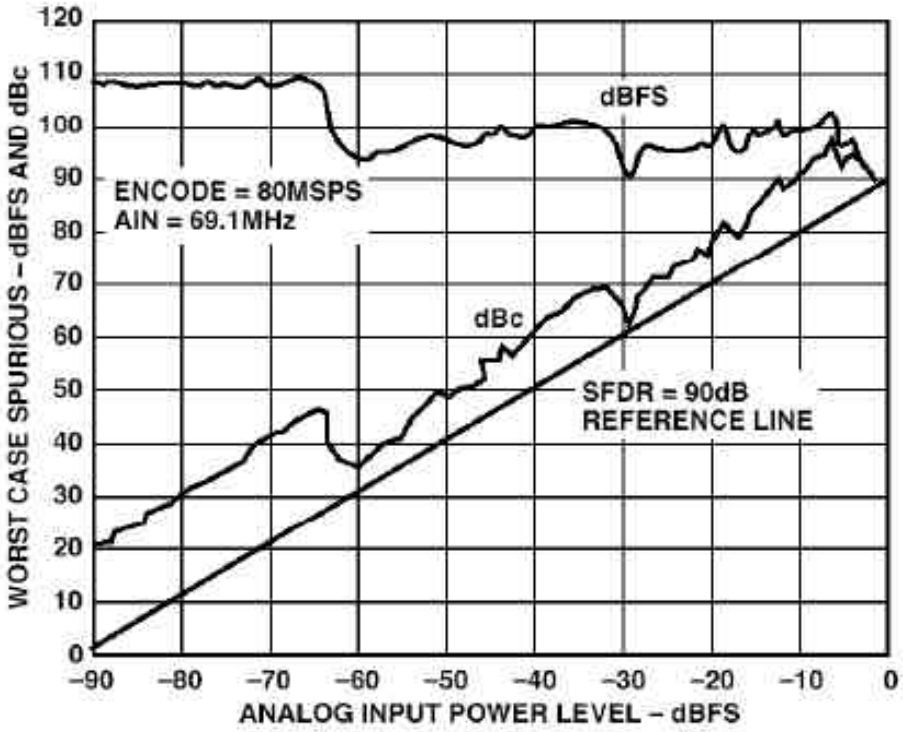


Figure 2.56: *AD6645 14-bit, 80-/105-MSPS ADC SFDR vs. Input Power Level for 69.1-MHz Input*

Notes

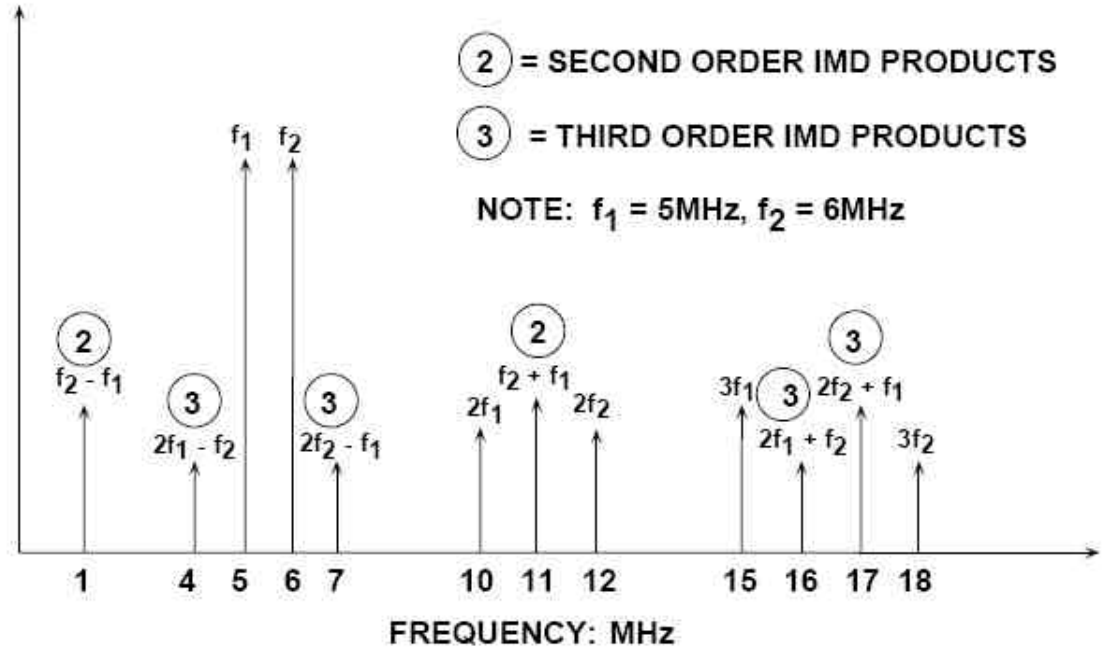


Figure 2.57: *Second and Third-Order Intermodulation Products for f_1 = 5 MHz, f_2 = 6 MHz*

Notes

Notes

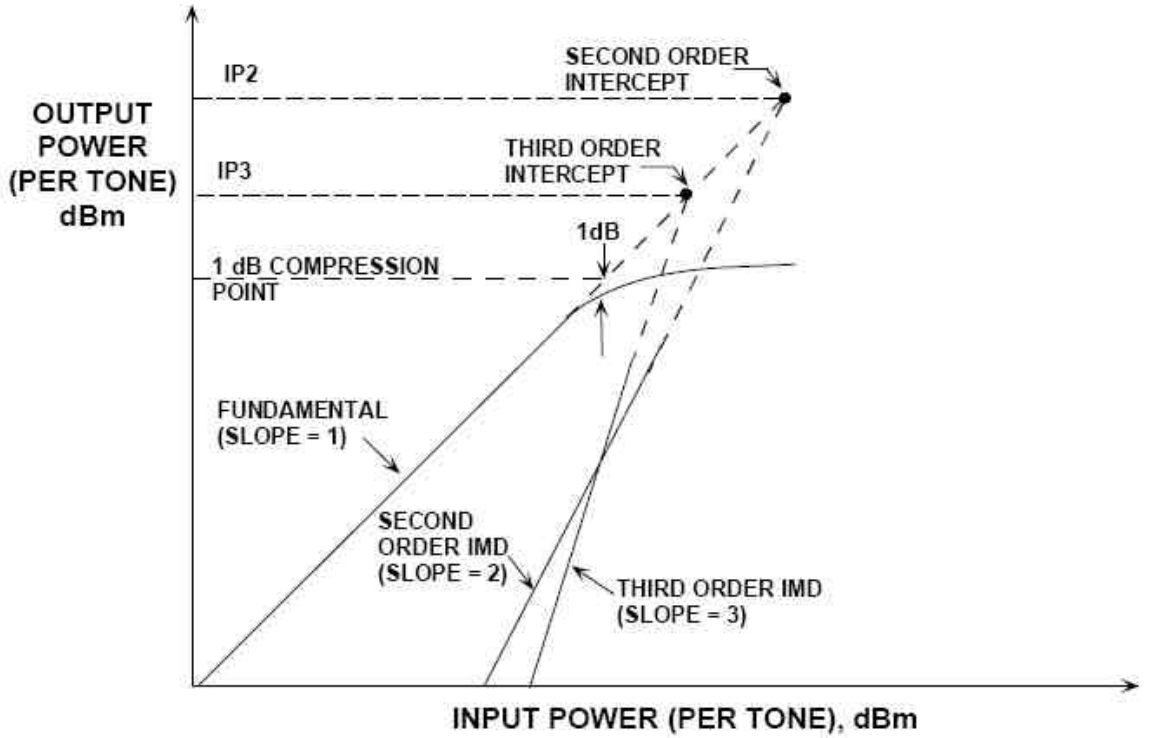


Figure 2.58: *Definition of Intercept Points and 1-dB Compression Points for Amplifiers*

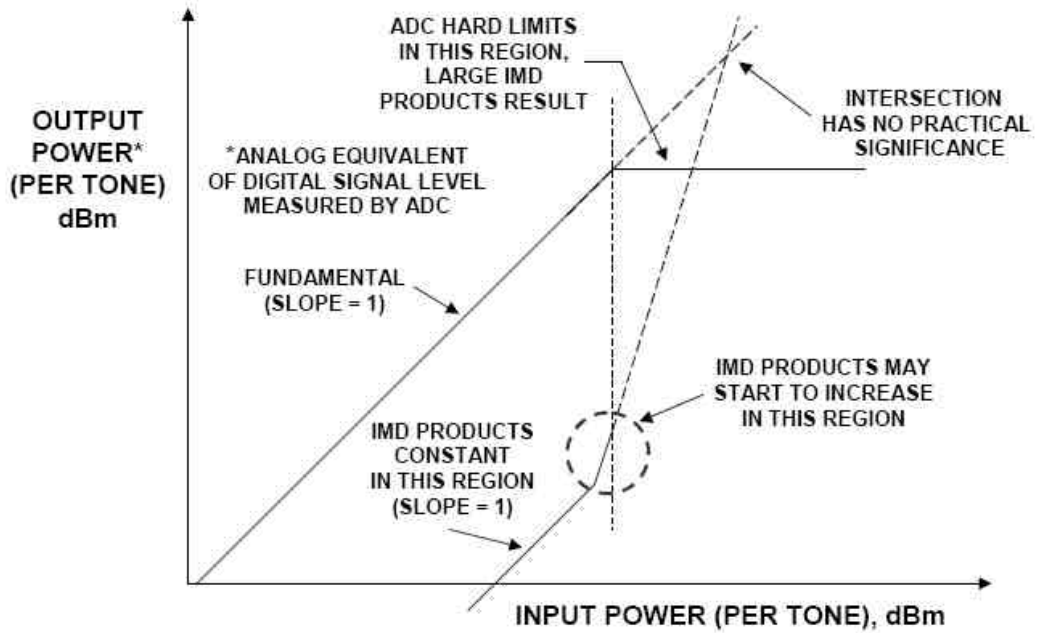


Figure 2.59: *Intercept Points for Data Converters Have No Practical Significance*

Notes

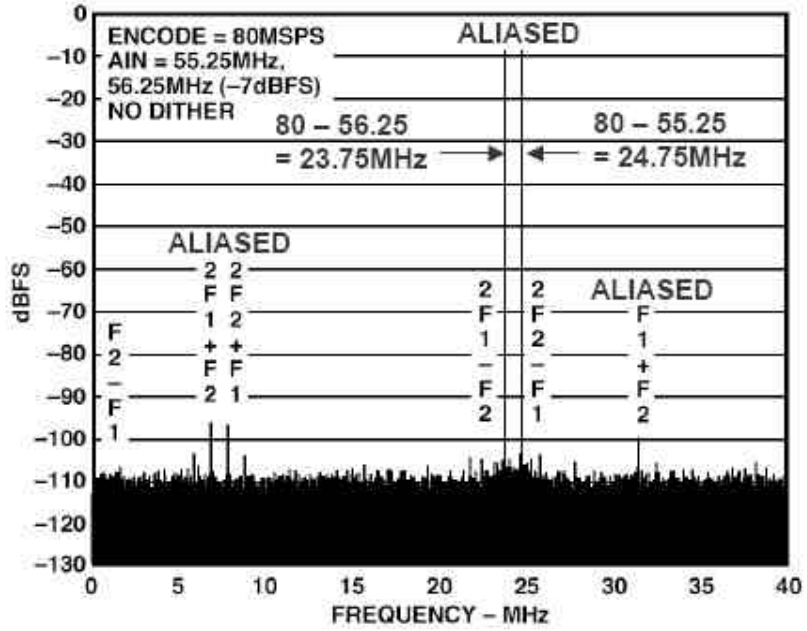


Figure 2.60: *Two-Tone SFDR for AD6645 14-bit, 80-/105-MSPS ADC, Input Tones: 55.25 MHz and 56.25 MHz*

Notes

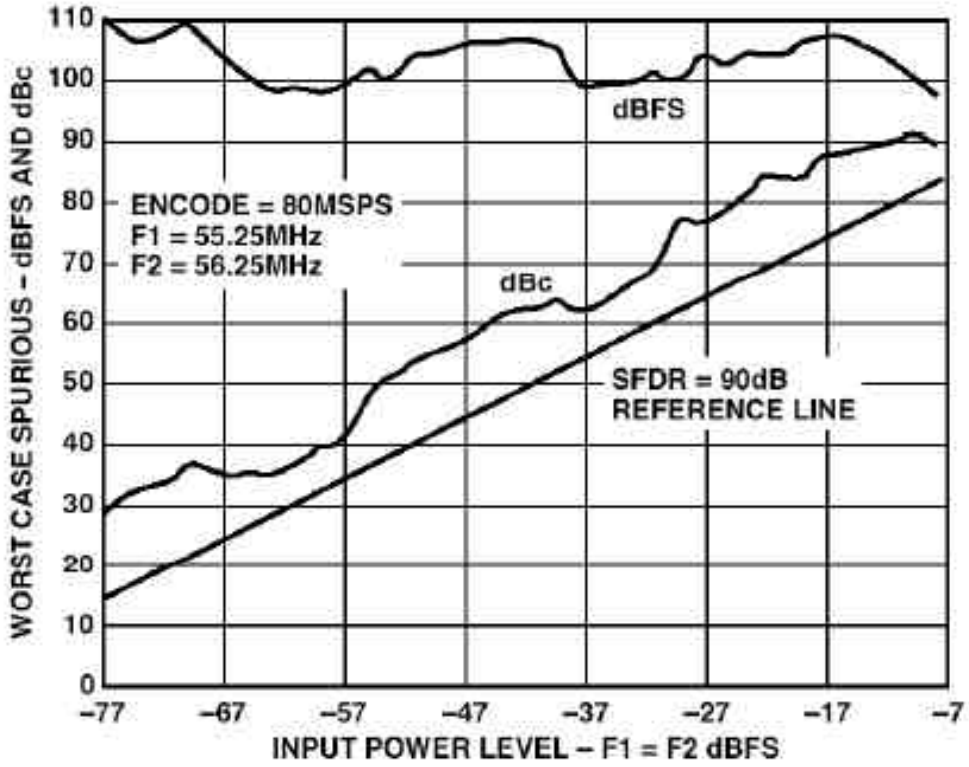


Figure 2.61: *Two-Tone SFDR vs. Input Amplitude for AD6645 14-bit, 80-/105-MSPS ADC*

Notes

Notes

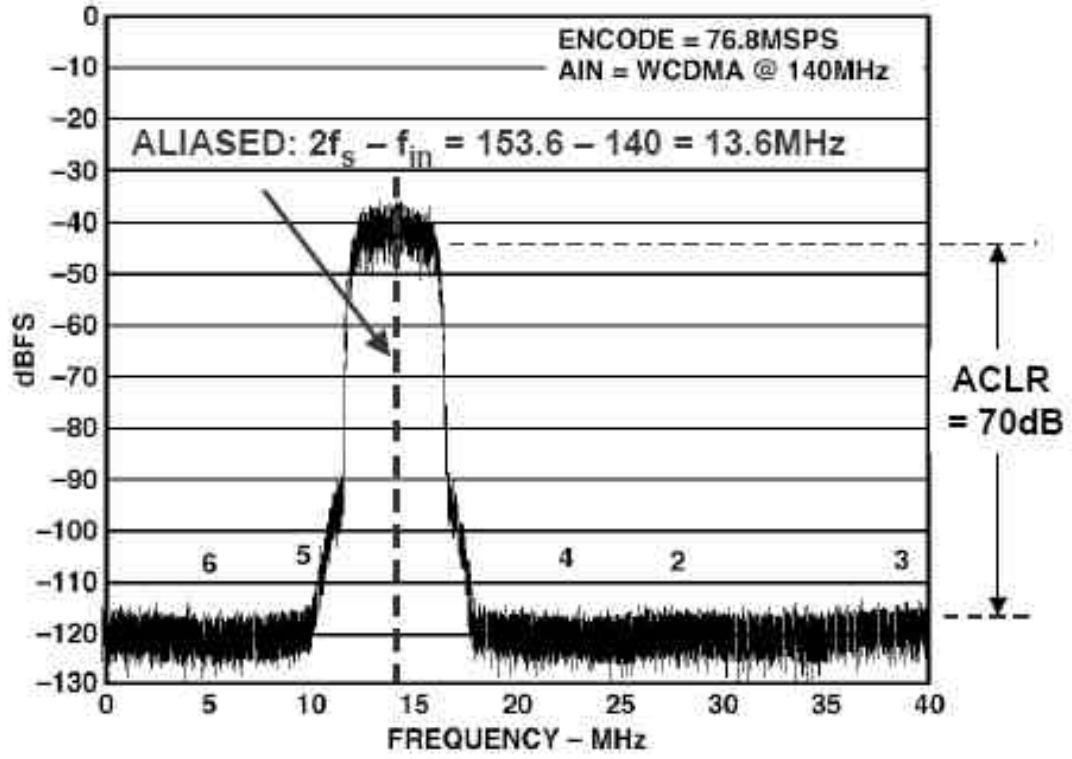


Figure 2.62: *Wideband CDMA (WCDMA) Adjacent Channel Leakage Ratio (ACLR)*

Notes

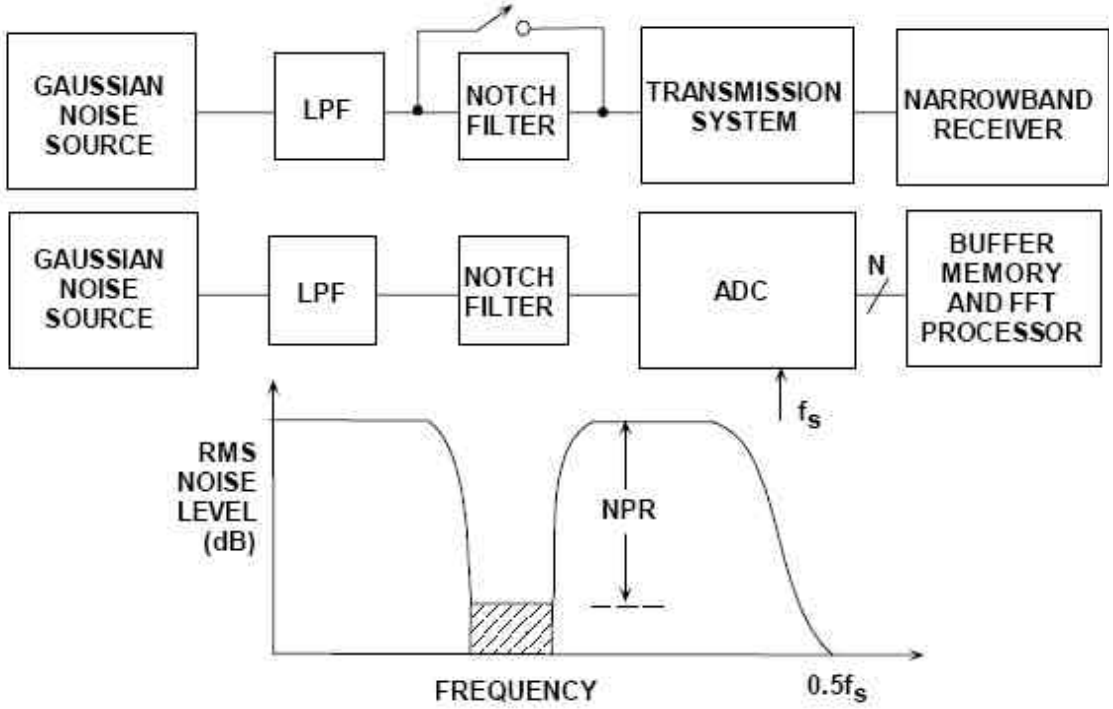


Figure 2.63: *Noise Power Ratio (NPR) Measurements*

Notes

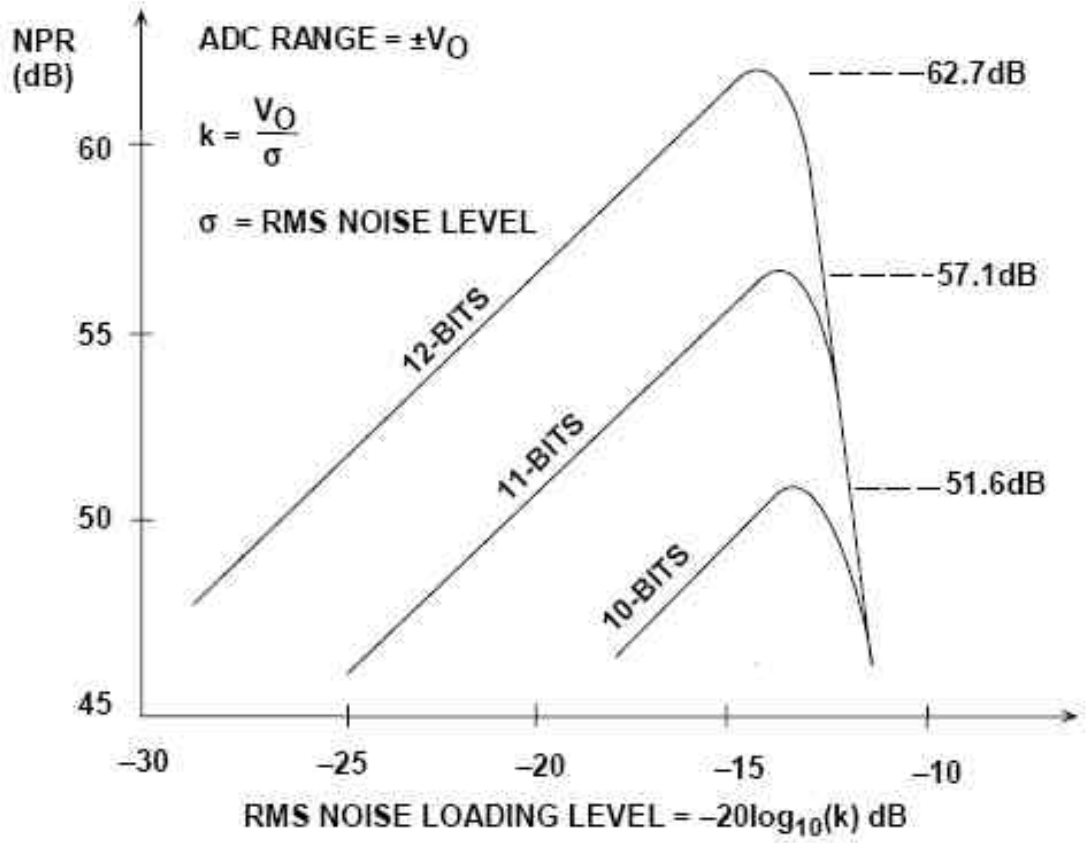


Figure 2.64: *Theoretical NPR for 10, 11, 12-bit ADCs*

BITS	k OPTIMUM	k(dB)	MAX NPR (dB)
8	3.92	11.87	40.60
9	4.22	12.50	46.05
10	4.50	13.06	51.56
11	4.76	13.55	57.12
12	5.01	14.00	62.71
13	5.26	14.41	68.35
14	5.49	14.79	74.01
15	5.72	15.15	79.70
16	5.94	15.47	85.40

ADC Range = $\pm V_o$
$k = V_o / \sigma$
σ = RMS Noise Level

Figure 2.65: *Theoretical Maximum NPR for 8 to 16-bit ADCs*

Notes

Notes

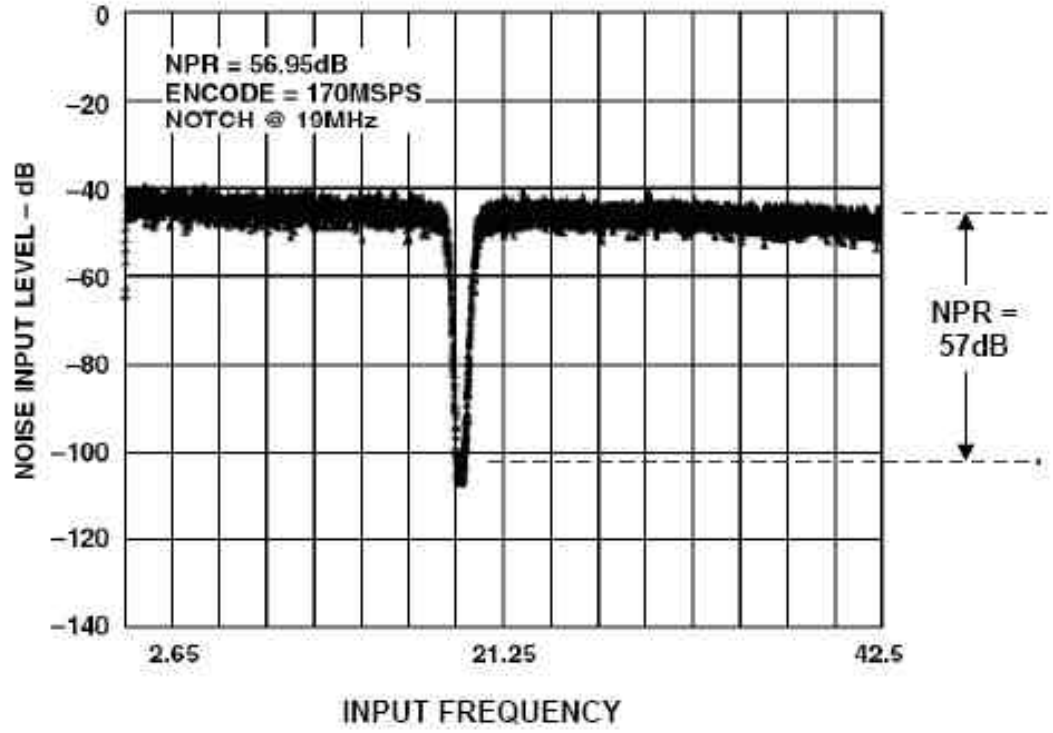
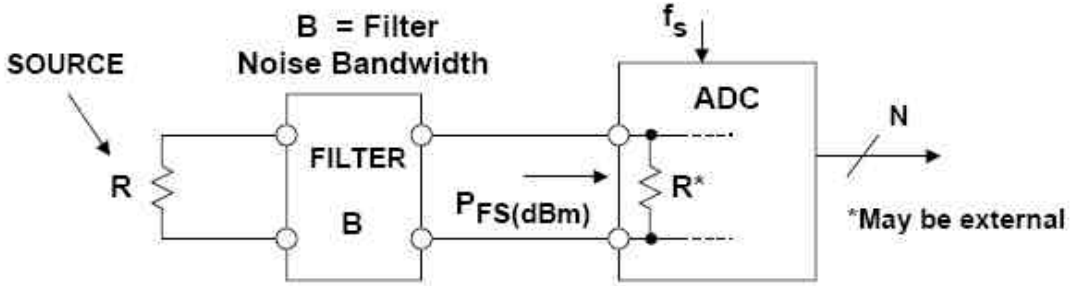


Figure 2.66: *AD9430 12-bit,170-/210-MSPS ADC NPR Measures 57 dB (62.7 dB Theoretical)*

Notes



$$\text{NOISE FACTOR (F)} = \frac{(\text{TOTAL EFFECTIVE INPUT NOISE})^2}{(\text{TOTAL INPUT NOISE DUE TO SOURCE R})^2}$$

$$\text{NOISE FIGURE (NF)} = 10\log_{10}\left[\frac{(\text{TOTAL EFFECTIVE INPUT NOISE})^2}{(\text{TOTAL INPUT NOISE DUE TO SOURCE R})^2}\right]$$

Note: Noise Must be Measured Over the Filter Noise Bandwidth, B

Figure 2.67: *Noise Figure for ADCs: Use with Caution!*

NUMBER OF POLES	NOISE BW / 3dB BW
1	1.57
2	1.11
3	1.05
4	1.03
5	1.02

Figure 2.68: *Relationship Between Noise Bandwidth and 3-dB Bandwidth for Butterworth Filter*

Notes

Notes

- Start with the SNR of the ADC measured at the carrier frequency (Note: this SNR value does not include the harmonics of the fundamental and is measured over the Nyquist bandwidth, dc to $f_s/2$)

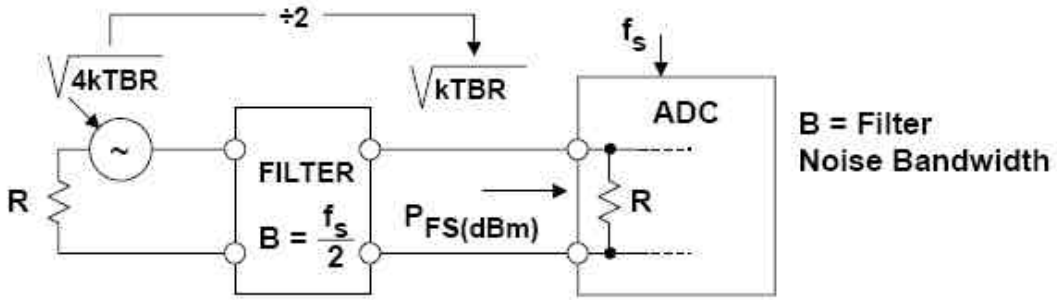
$$SNR = 20 \log_{10} \frac{V_{FS\text{-}RMS}}{V_{NOISE\text{-}RMS}}$$

$$V_{NOISE\text{-}RMS} = V_{FS\text{-}RMS}\, 10^{-SNR/20}$$

- This is the total ADC effective input noise at the carrier frequency measured over the Nyquist bandwidth, dc to $f_s/2$

Figure 2.69: *Calculating ADC Total Effective Input Noise from SNR*

Notes



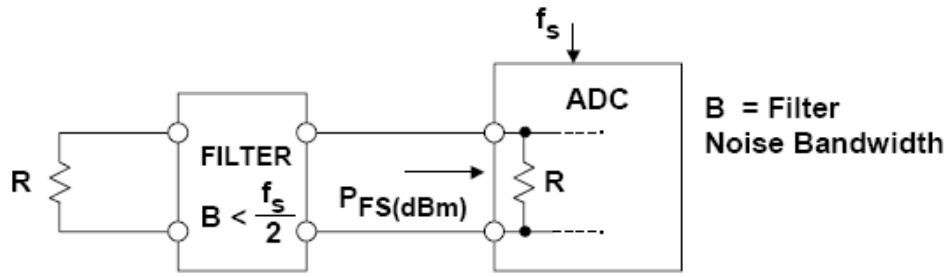
$$V_{NOISE\text{-}RMS} = V_{FS\text{-}RMS}\, 10^{-SNR/20}$$

$$F = \frac{V_{NOISE\text{-}RMS}^2}{kTRB} = \left[\frac{V_{FS\text{-}RMS}^2}{R}\right]\left[\frac{1}{kT}\right]\left[10^{-SNR/10}\right]\left[\frac{1}{B}\right]$$

$$NF = 10\log_{10}F = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B,$$

where SNR is in dB, B in Hz, $T = 300K$, $k = 1.38 \times 10^{-23}$ J/K

Figure 2.70: *ADC Noise Figure in Terms of SNR, Sampling Rate, and Input Power*



$$NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}\left[\frac{f_s/2}{B}\right] - 10\log_{10}B,$$

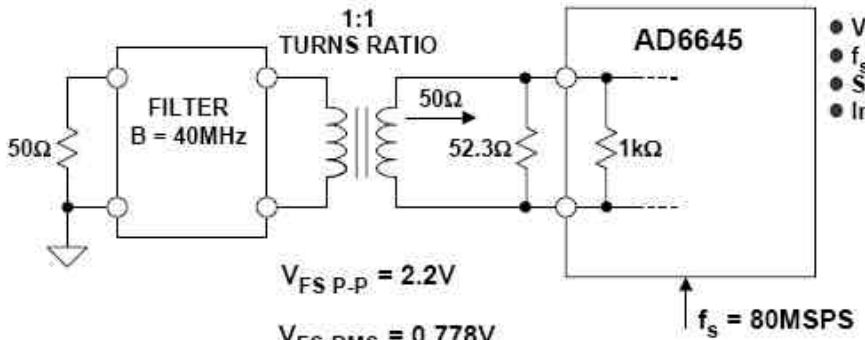
Measured DC to $f_s/2$ — Process Gain

where SNR is in dB, B in Hz, T = 300K, $k = 1.38 \times 10^{-23}$ J/K

Figure 2.71: *Effect of Oversampling and Process Gain on ADC Noise Figure*

Notes

Notes



$V_{FS\ P-P} = 2.2V$

$V_{FS\text{-}RMS} = 0.778V$

$$P_{FS} = \frac{(0.778)^2}{50} = 12.1mW$$

$P_{FS(dBm)} = +10.8dBm$

$$NF = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B$$

$$= +10.8dBm + 174dBm - 74dB - 10\log_{10}(40 \times 10^6)$$

$$= 34.8dB$$

Figure 2.72: *Example Calculation of Noise Figure Under Nyquist Conditions for AD6645*

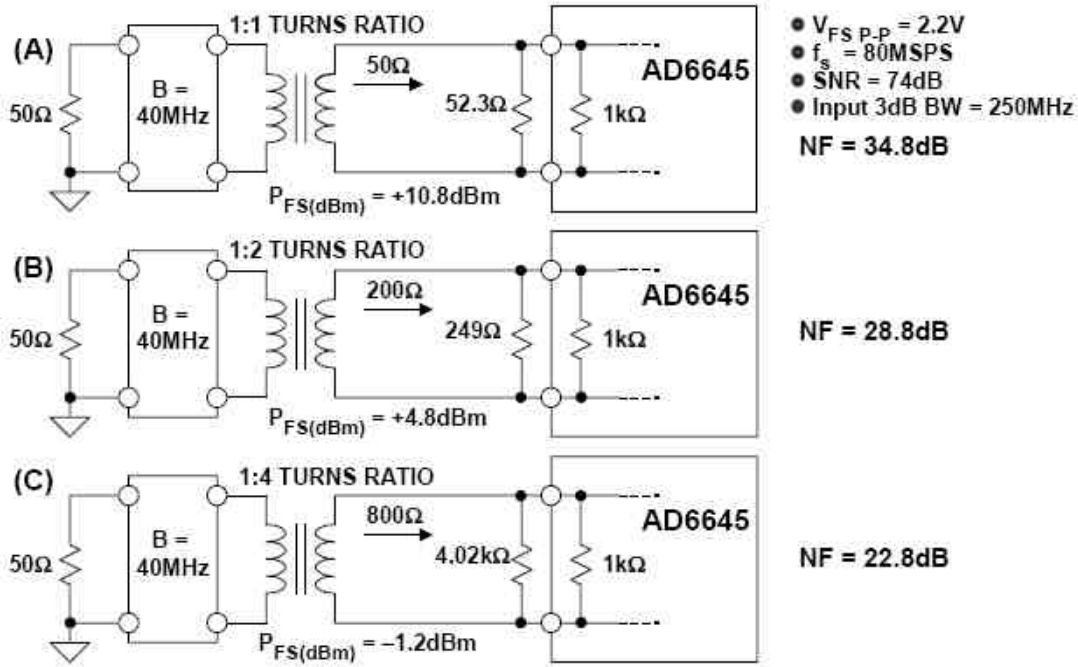


Figure 2.73: *Using RF Transformers to Improve Overall ADC Noise Figure*

Notes

Notes

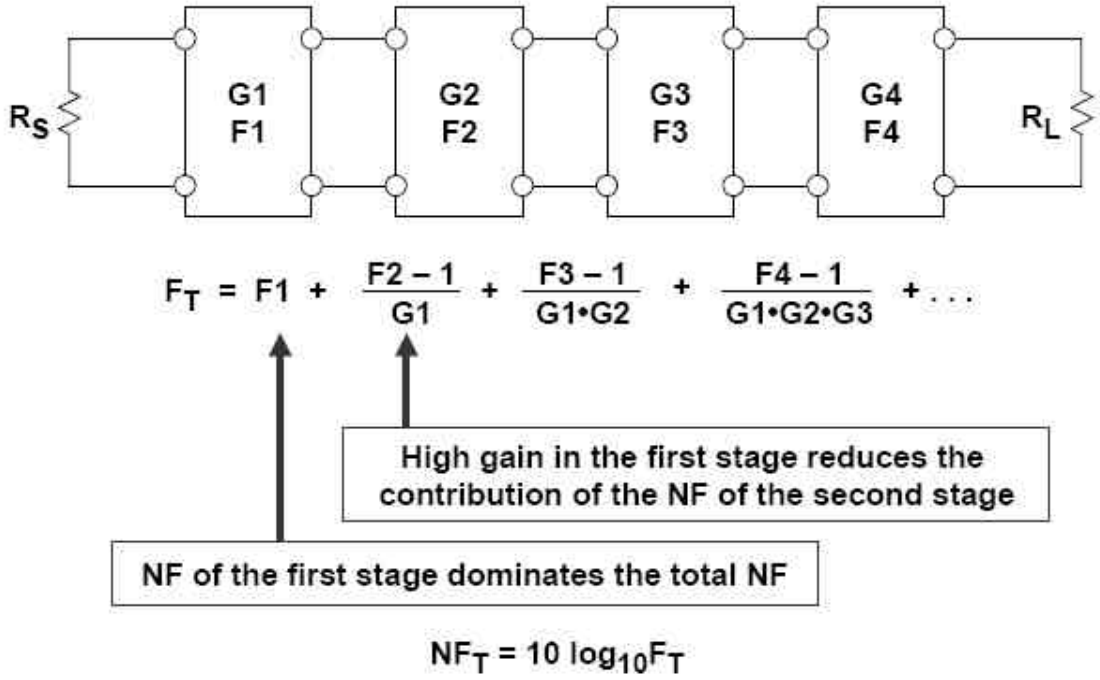
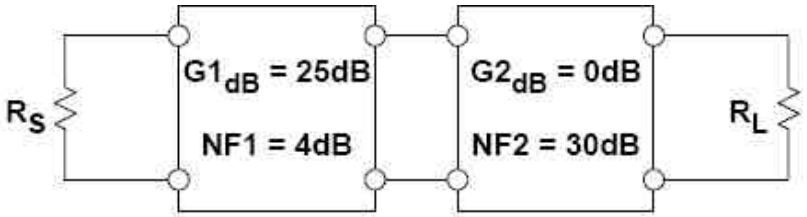


Figure 2.74: *Cascaded Noise Figure Using the Friis Equation*



$G1 = 10^{25/10} = 10^{2.5} = 316$, $F1 = 10^{4/10} = 10^{0.4} = 2.51$

$G2 = 1$, $F2 = 10^{30/10} = 10^{3} = 1000$

$$F_T = F1 + \frac{F2 - 1}{G1} = 2.51 + \frac{1000 - 1}{316} = 2.51 + 3.16 = 5.67$$

$$NF_T = 10 \log_{10} 5.67 = 7.53dB$$

- The first stage dominates the overall NF
- It should have the highest gain possible with the lowest NF possible

Figure 2.75: *Example of Two-Stage Cascaded Network*

Notes

- NF decreases with increasing source resistance.
- NF decreases with increasing ADC input bandwidth if there is no input filtering.
- In both cases, the circuit noise increases, and the NF decreases.
- The reason NF decreases is that the source noise makes up a larger component of the total noise (which remains relatively constant because the ADC noise is much greater than the source noise).
- In practice, input filtering is used to limit the input noise bandwidth and reduce overall system noise.
- ADCs have relatively high NF compared to other RF parts. In the system the ADC should be preceded with low-noise gain blocks.
- Exercise caution when using NF!

Figure 2.76: *Noise Figure Considerations for ADCs: Summary and Caution*

Notes

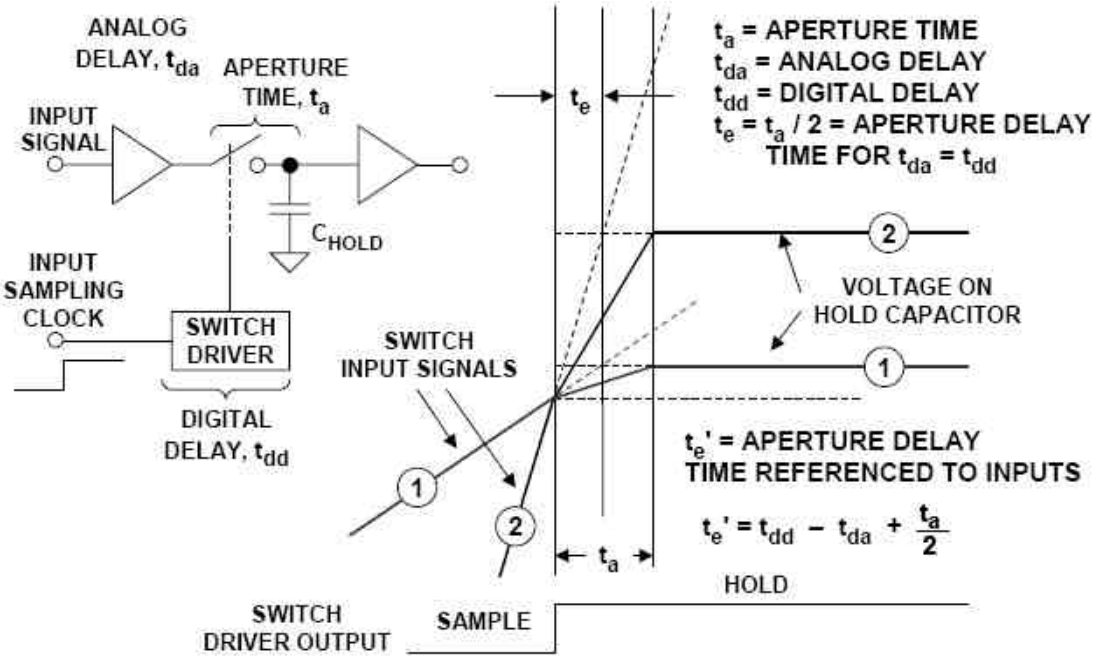


Figure 2.77: *Sample-and-Hold Waveforms and Definitions*

Notes

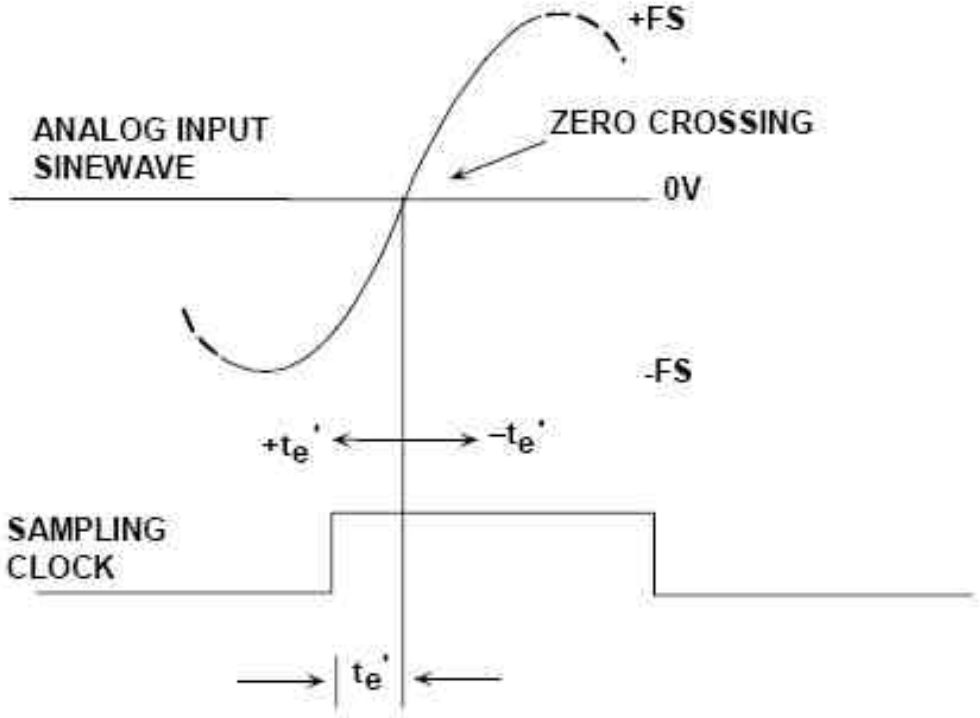


Figure 2.78: *Effective Aperture Delay Time Measured with Respect to ADC Input*

Notes

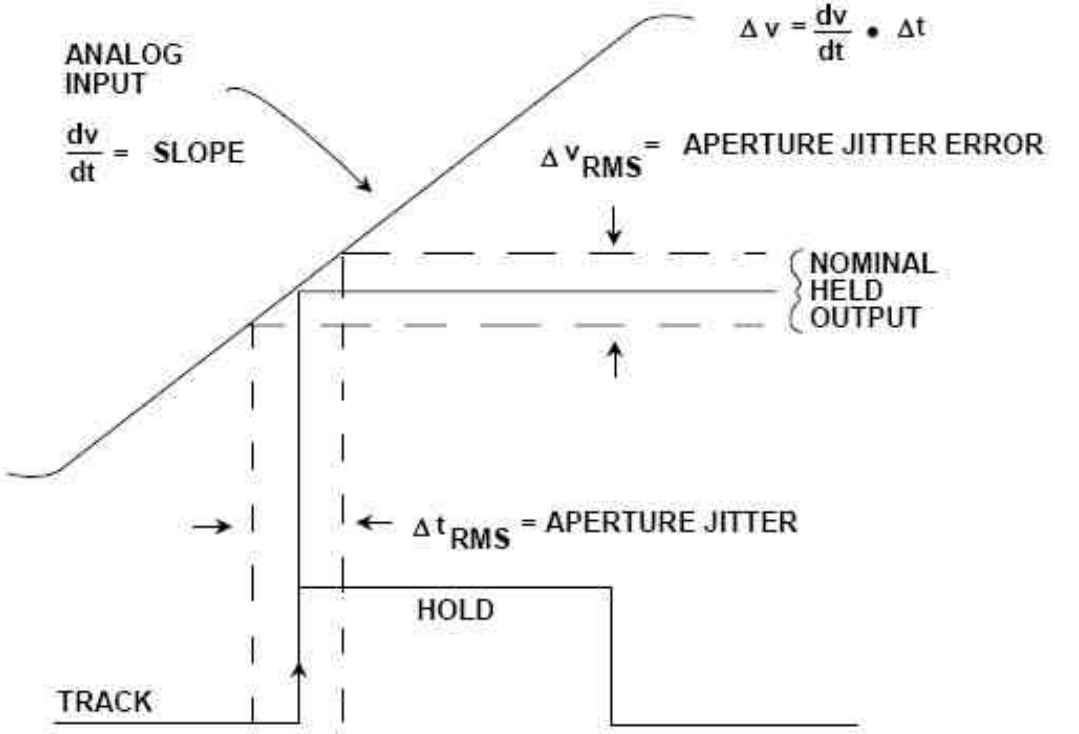


Figure 2.79: *Effects of Aperture Jitter and Sampling Clock Jitter*

Notes

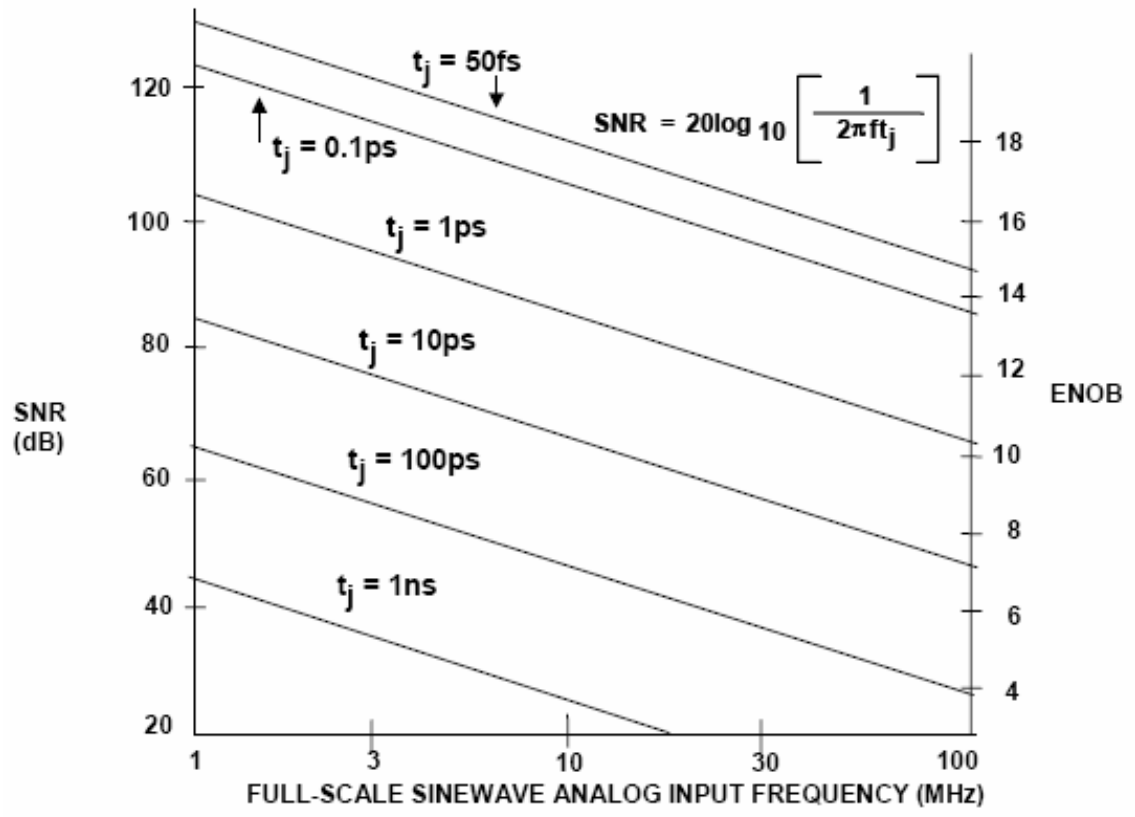
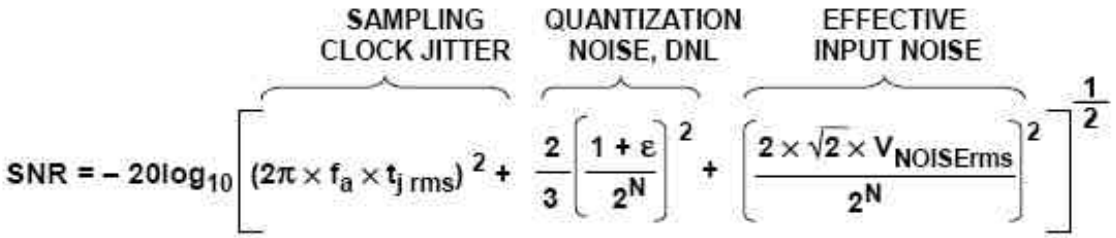


Figure 2.80: *Theoretical SNR and ENOB Due to Jitter vs. Fullscale Sinewave Input Frequency*

Notes

Notes



f_a = Analog input frequency of fullscale input sinewave

$t_{j\,rms}$ = Combined rms jitter of internal ADC and external clock

ε = Average DNL of the ADC (typically 0.41 LSB for AD6645)

N = Number of bits in the ADC

$V_{NOISErms}$ = Effective input noise of ADC (typically 0.9LSB rms for AD6645)

If $t_j = 0$, $\varepsilon = 0$, and $V_{NOISErms} = 0$, the above equation reduces to the familiar:

$$SNR = 6.02\,N + 1.76dB$$

Figure 2.81: *Relationship Between SNR, Sampling Clock Jitter, Quantization Noise, DNL, and Input Noise*

Notes

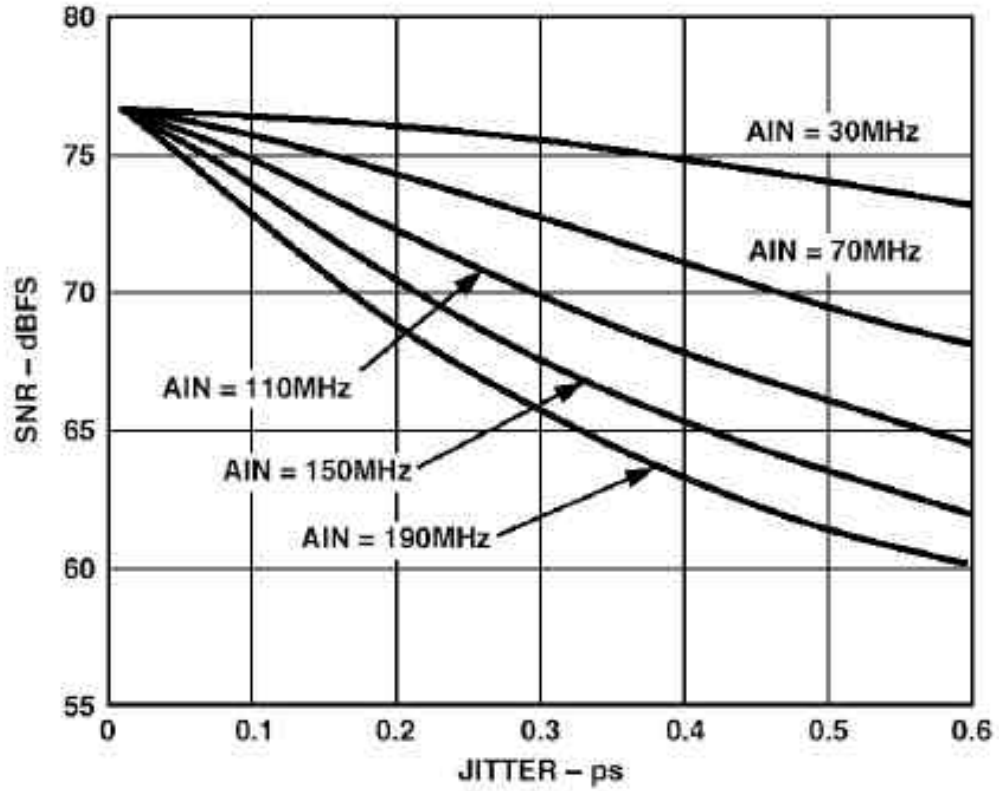


Figure 2.82: *AD6645 SNR Versus Jitter*

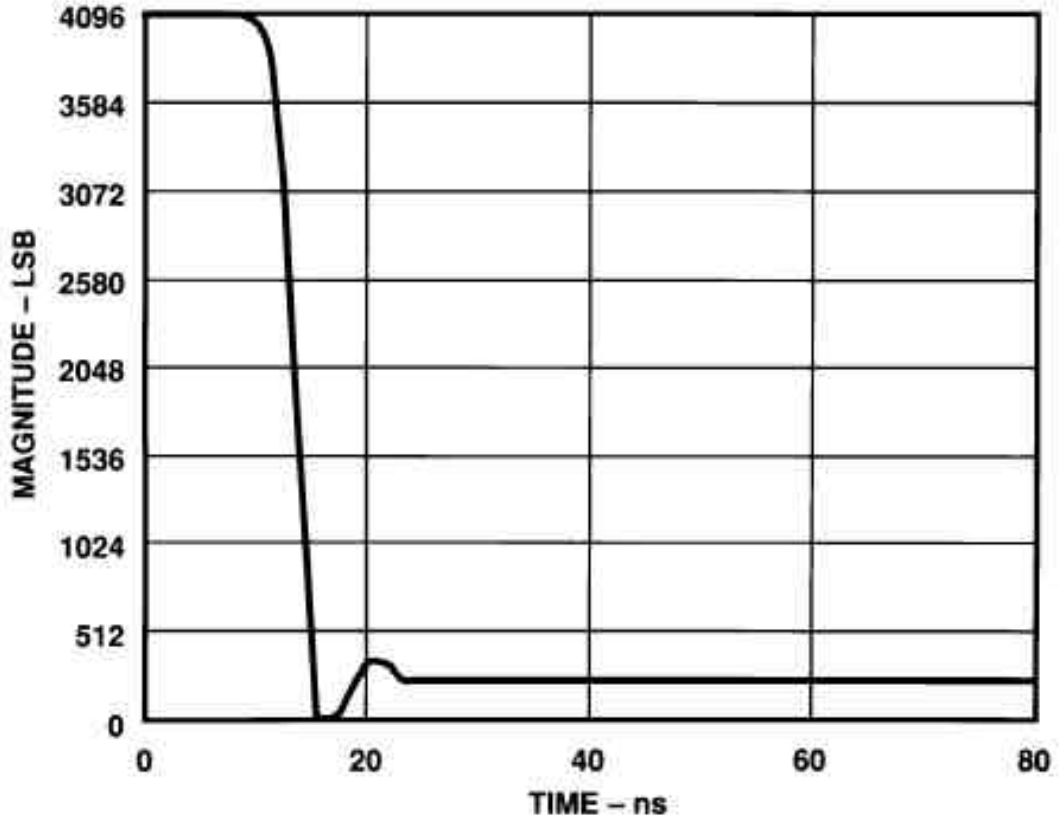


Figure 2.83: *ADC Transient Response (Settling Time)*

Notes

Notes

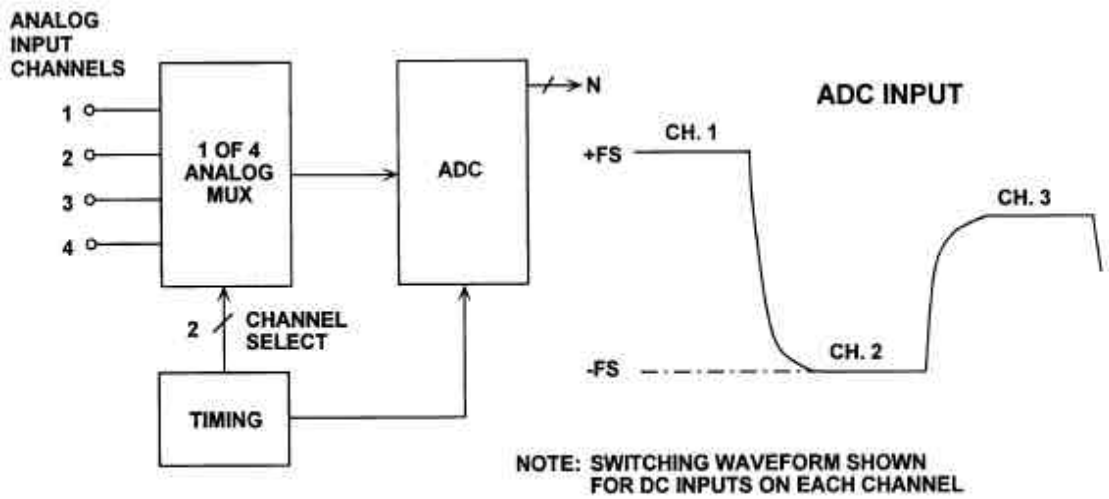


Figure 2.84: *Settling Time is Critical in Multiplexed Applications*

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Figure 2.85: *Settling Time as a Function of Time Constant for Various Resolutions*

Notes

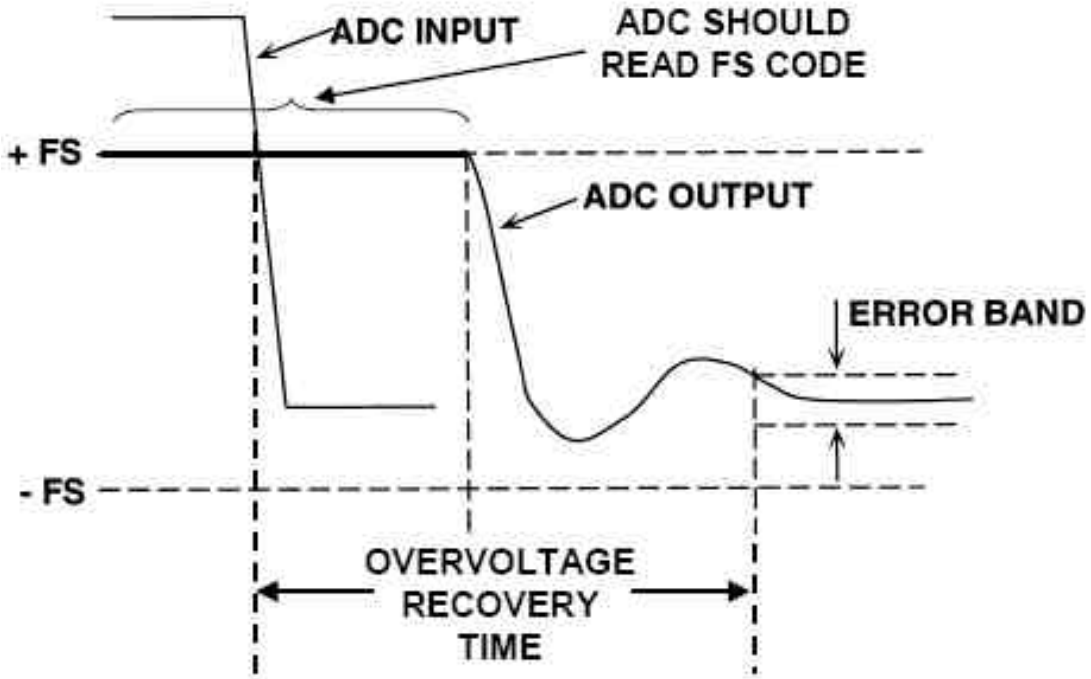


Figure 2.86: *Overvoltage Recovery Time*

Notes

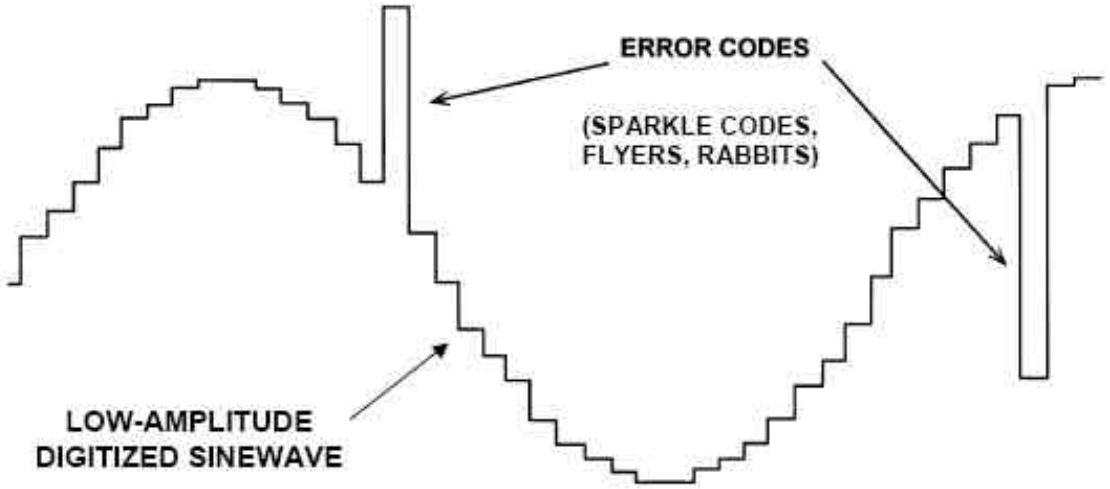


Figure 2.87: *Exaggerated Output of ADC Showing Error Codes*

Notes

Notes

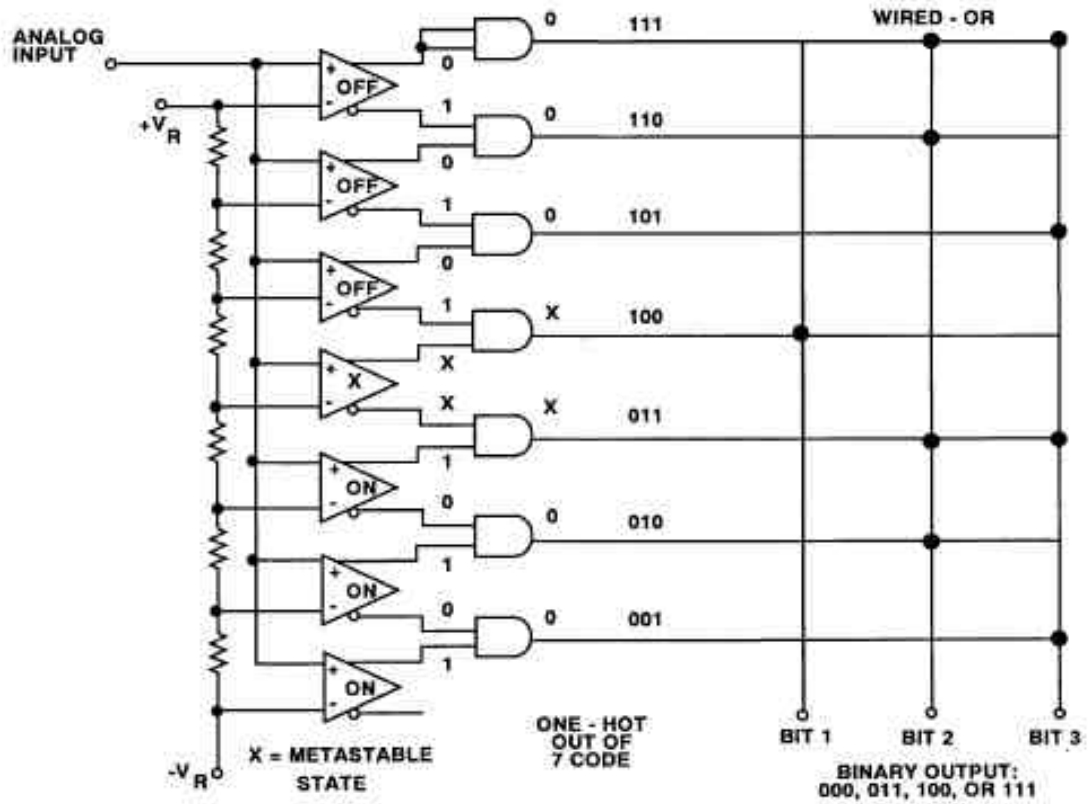


Figure 2.88: *Metastable Comparator Output States May Cause Error Codes in Data Converters*

Notes

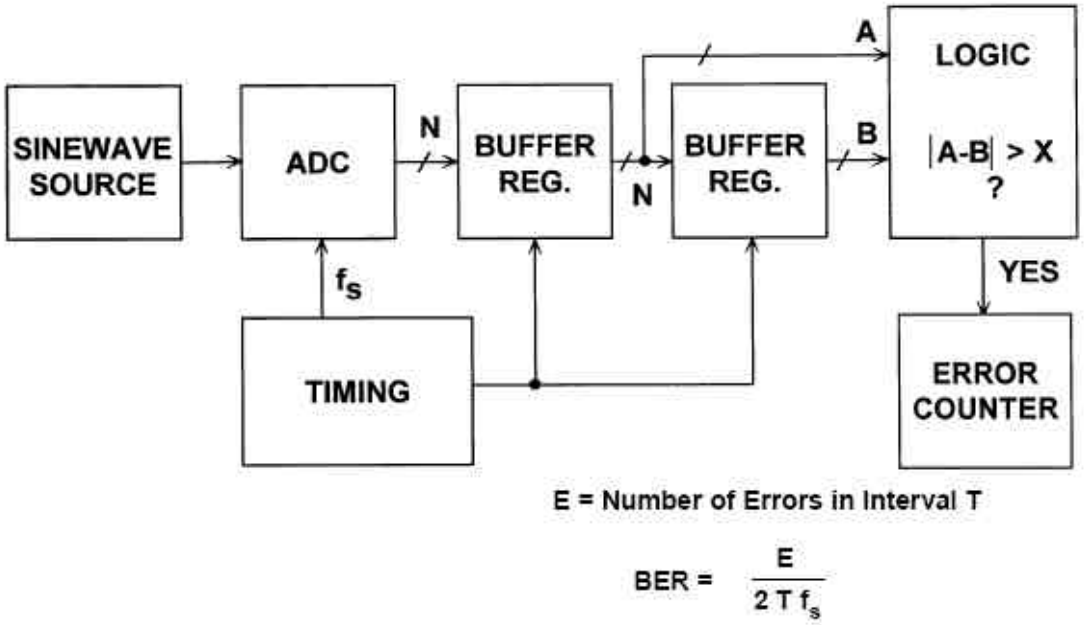


Figure 2.89: *ADC Bit Error Rate Test Setup*

Notes

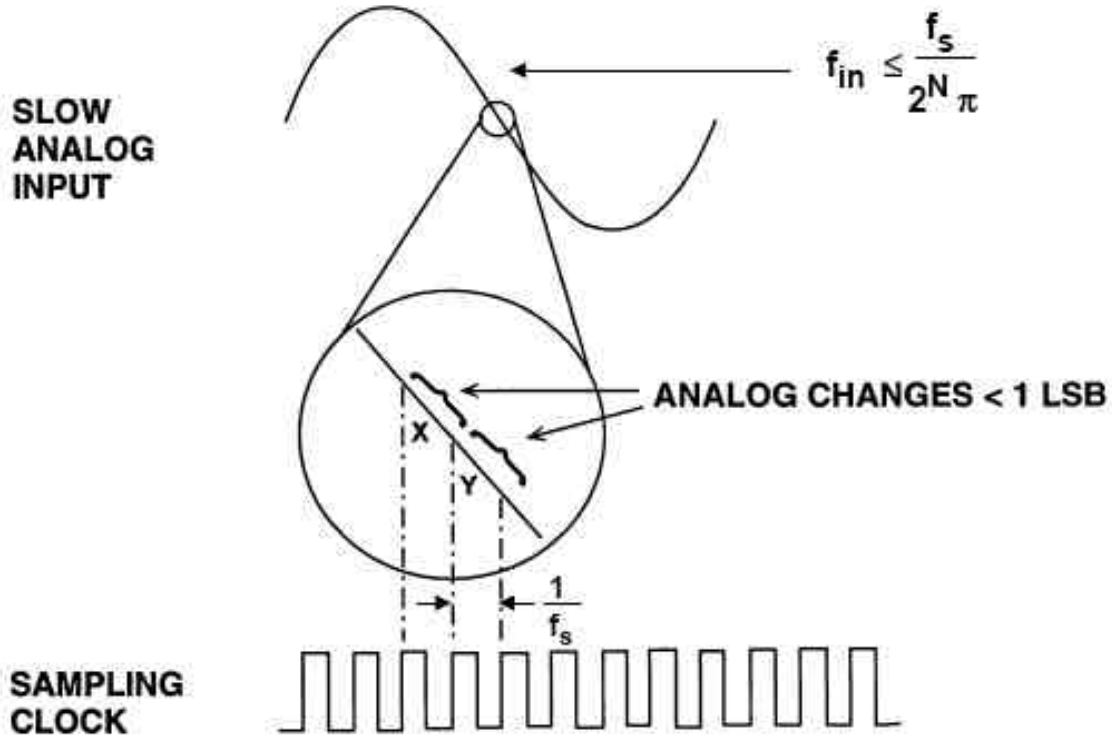


Figure 2.90: *ADC Analog Signal for Low Frequency BER Test*

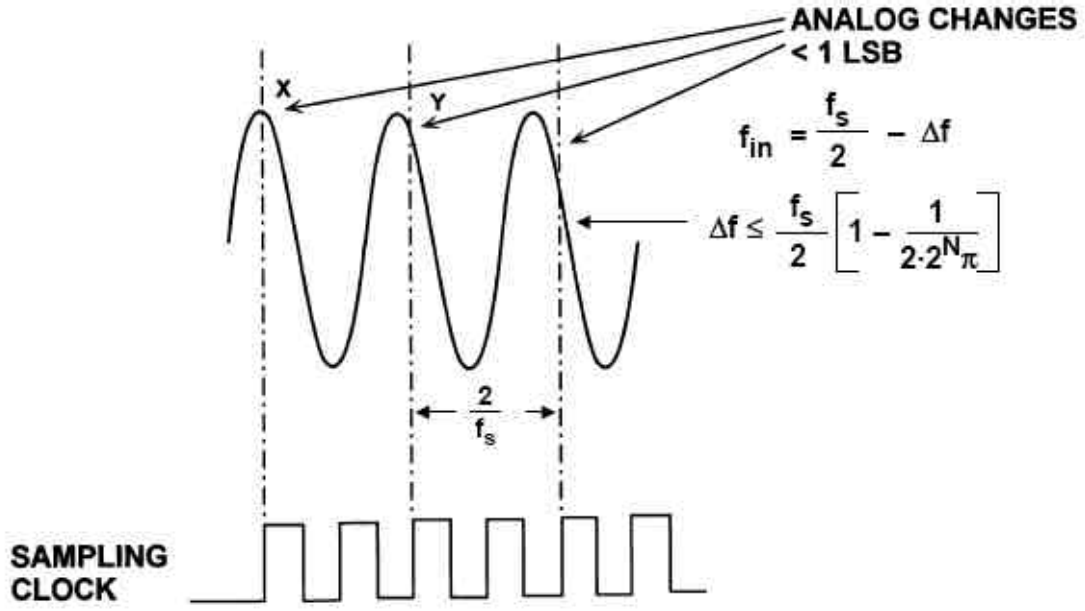


Figure 2.91: *ADC Analog Input for High Frequency BER Test*

Notes

Bit Error Rate (BER)	Average Time Between Errors
1×10^{-8}	1.3 seconds
1×10^{-9}	13.3 seconds
1×10^{-10}	2.2 minutes
1×10^{-11}	22 minutes
1×10^{-12}	3.7 hours
1×10^{-13}	1.5 days
1×10^{-14}	15 days

Figure 2.92: *Average Time Between Errors Versus BER when Sampling at 75 MSPS*

Notes

Notes

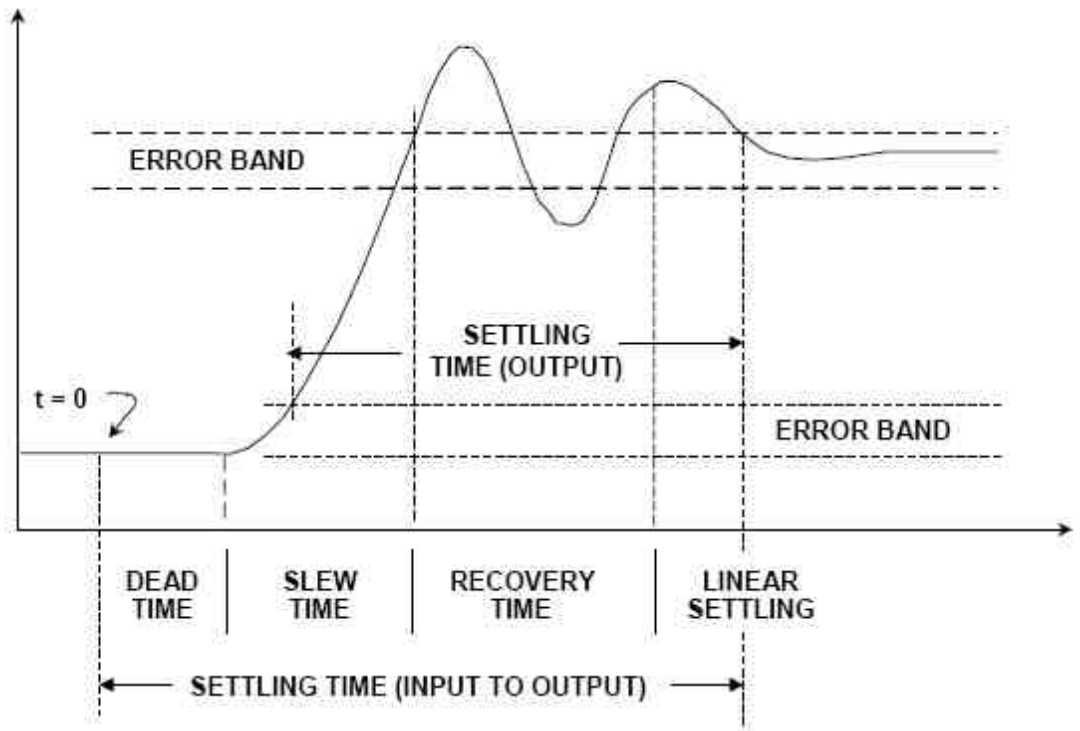


Figure 2.93: *DAC Settling Time*

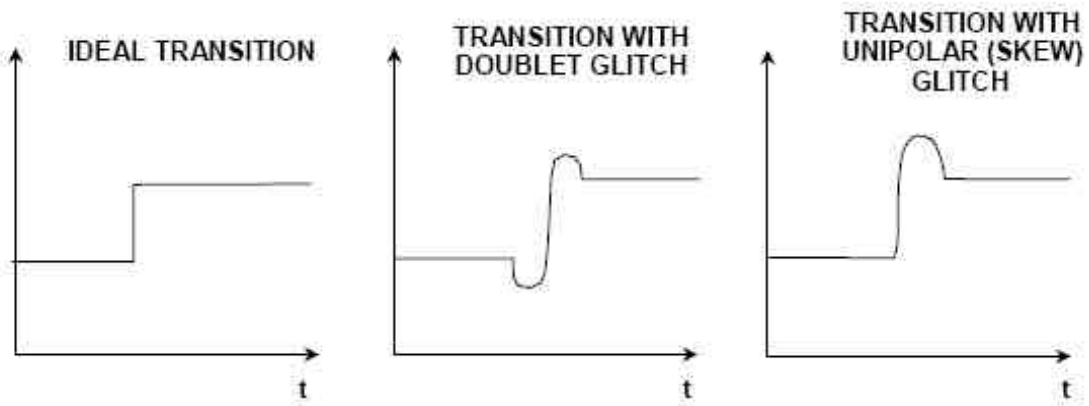
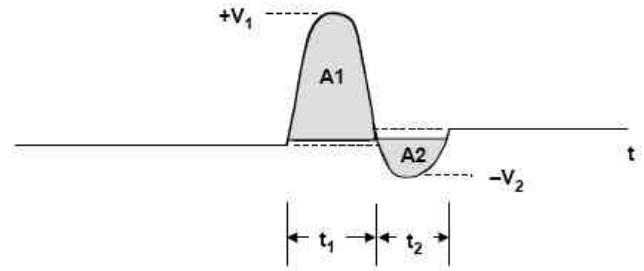


Figure 2.94: *DAC Transitions (Showing Glitch)*

Notes



- PEAK GLITCH IMPULSE AREA = A1 $\approx \frac{V_1 \cdot t_1}{2}$
- NET GLITCH IMPULSE AREA = A1 – A2 $\approx \frac{V_1 \cdot t_1}{2} - \frac{V_2 \cdot t_2}{2}$

Figure 2.95: *Calculating Net Glitch Impulse Area*

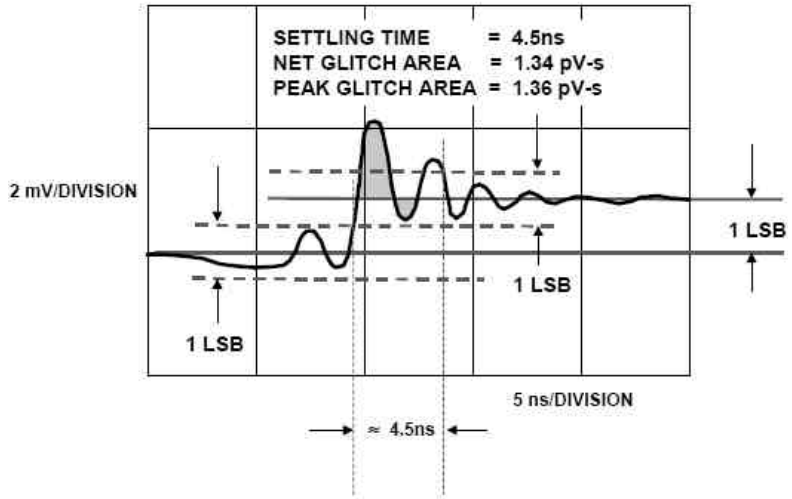


Figure 2.96: *DAC Mid-scale Glitch Shows 1.34pV-s Net Impulse Area and Settling Time of 4.5ns*

Notes

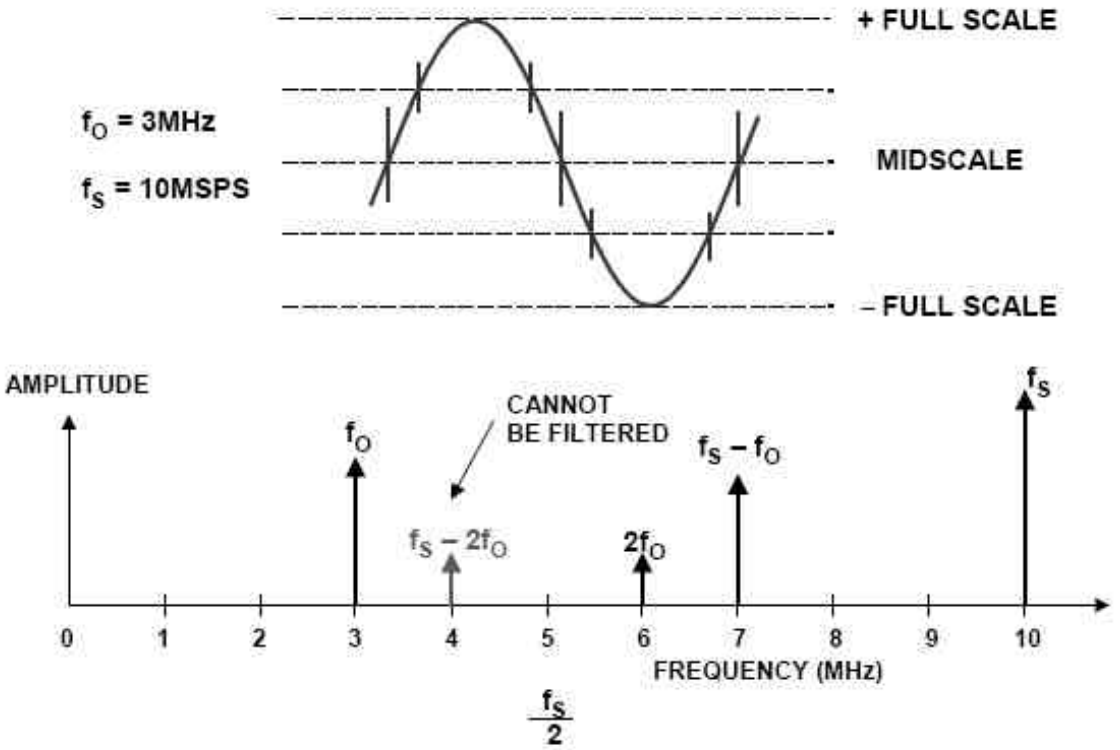


Figure 2.97: *Effect of Code-Dependent Glitches on Spectral Output*

Notes

- Resolution
- Integral Non-Linearity
- Differential Non-Linearity
- Code-Dependent Glitches
- Ratio of Clock Frequency to Output Frequency (Even in an Ideal DAC)
- Mathematical Analysis is Difficult !

Figure 2.98: *Contributors to DDS DAC Distortion*

Notes

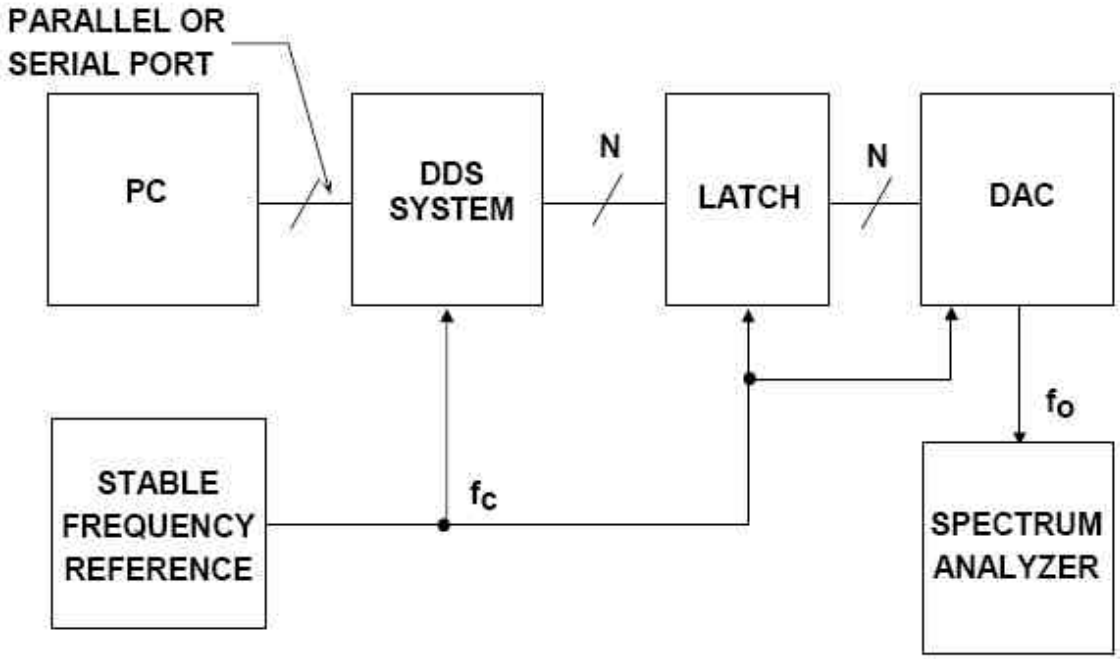


Figure 2.99: *Test Setup for Measuring DAC SFDR*

Notes

Notes

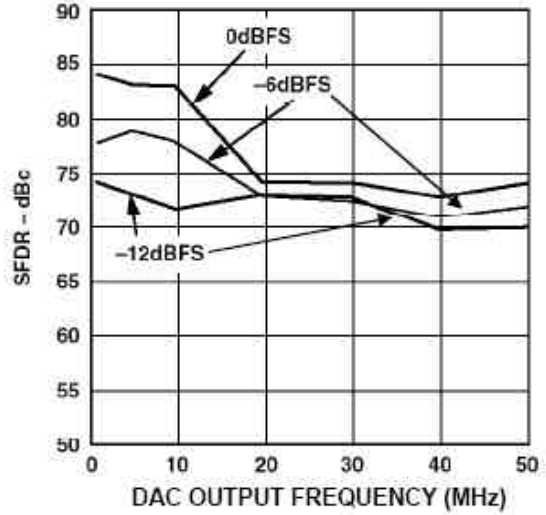
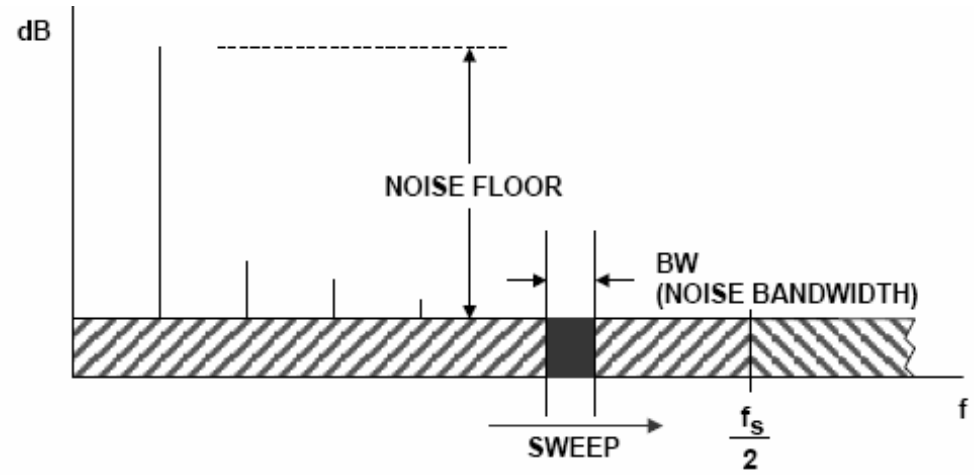


Figure 2.100: *AD9777 16-bit TxDAC® SFDR, Data Update Rate = 160 MSPS*



- BW = ANALYZER RESOLUTION NOISE BANDWIDTH
- SNR = NOISE FLOOR – $10 \log_{10}\left[\frac{f_s/2}{BW}\right]$

Figure 2.101: *Measuring DAC SNR with an Analog Spectrum Analyzer*

Notes

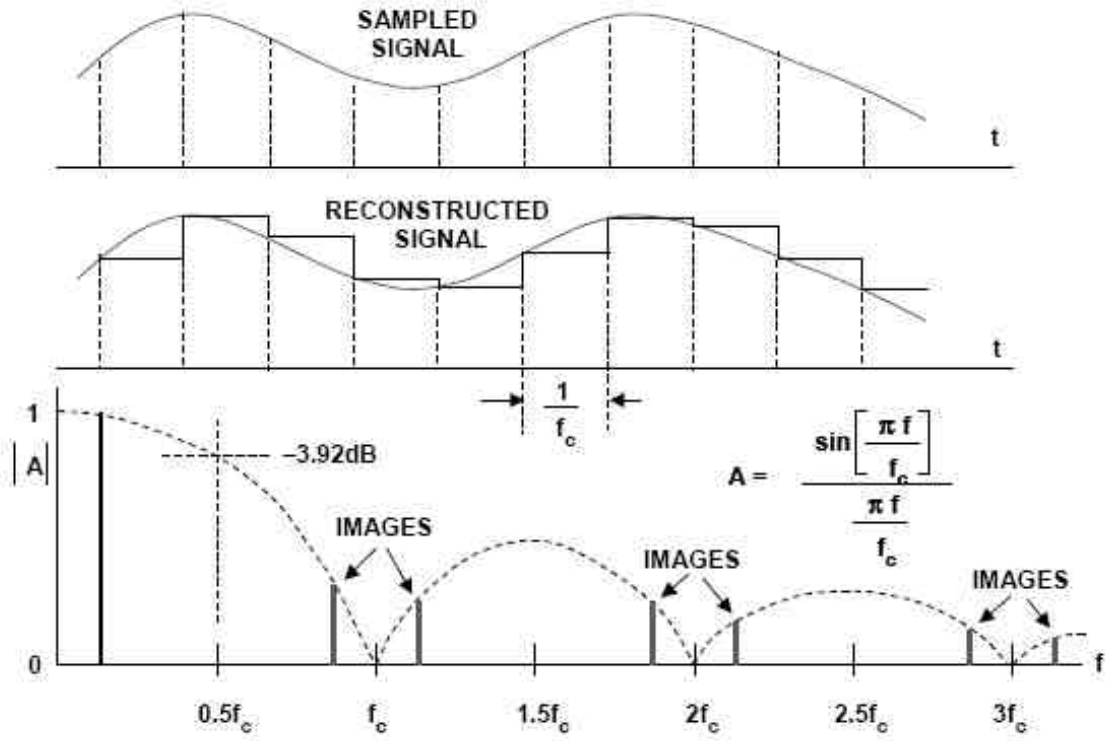


Figure 2.102: *DAC sin x/x Roll Off (Amplitude Normalized)*

Notes

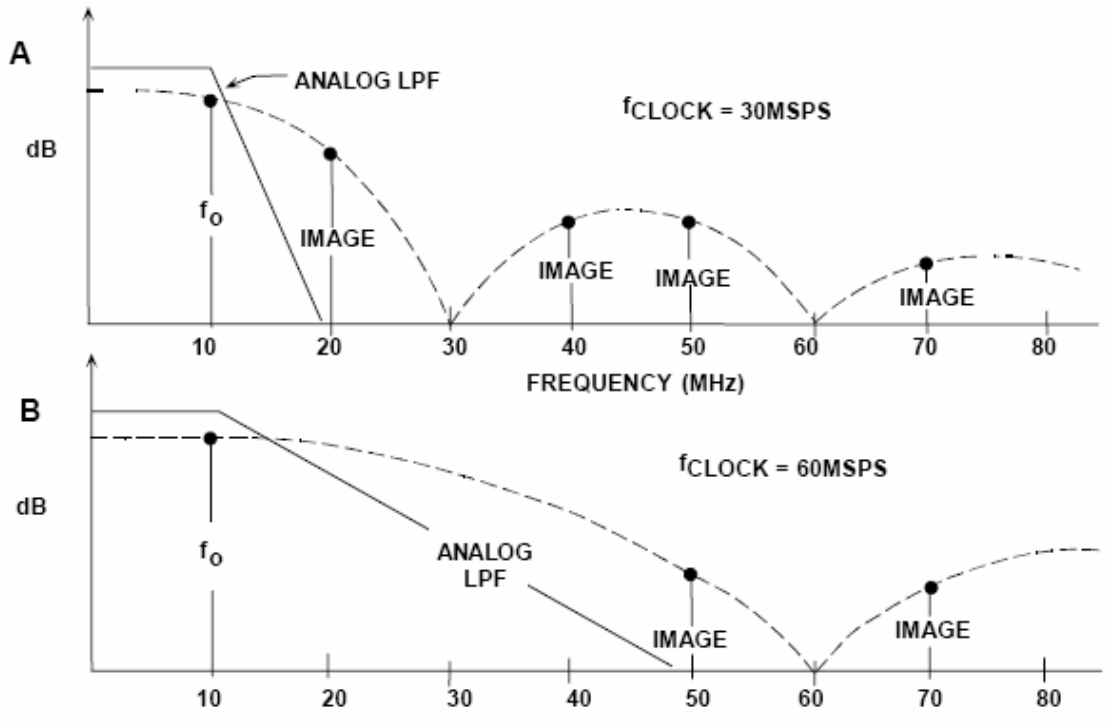


Figure 2.103: *Analog Filter Requirements for f_o = 10 MHz: (A) f_c = 30 MSPS, and (B) f_c = 60 MSPS*

Notes

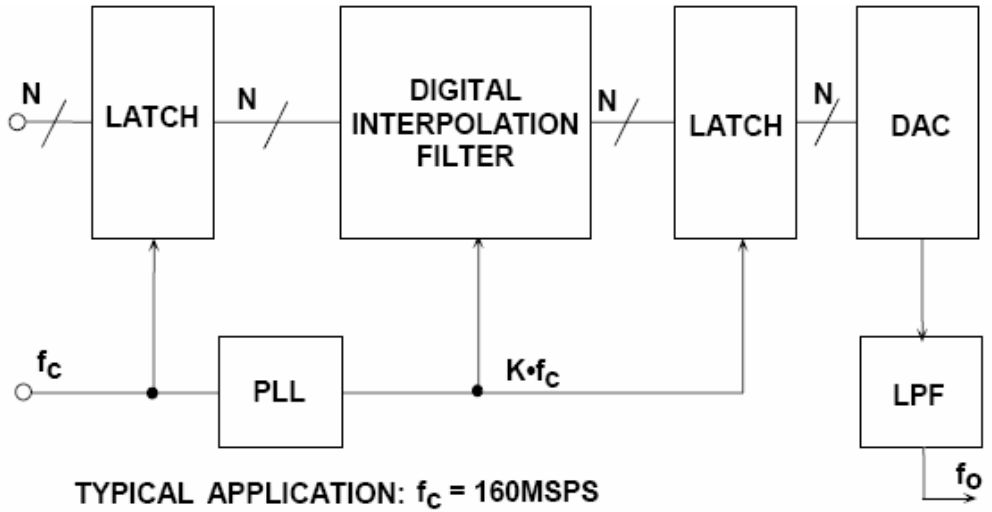


Figure 2.104: *Oversampling Interpolating TxDAC® Simplified Block Diagram*

Notes