Notes

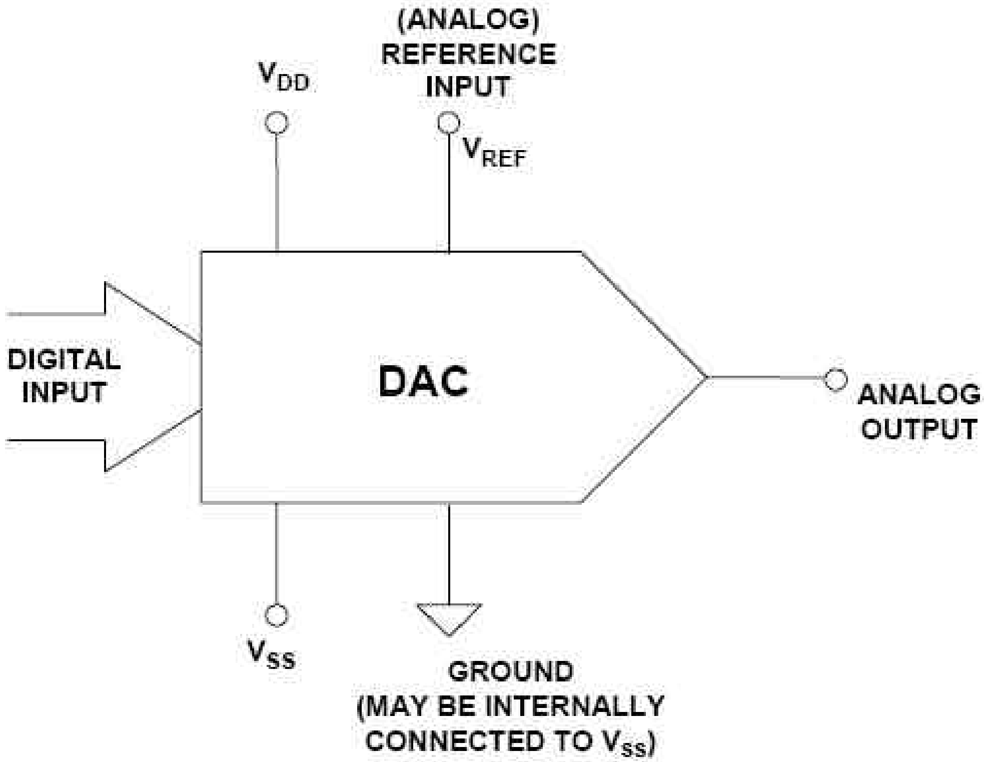


Figure 3.1: *Basic DAC with External Reference*

Notes

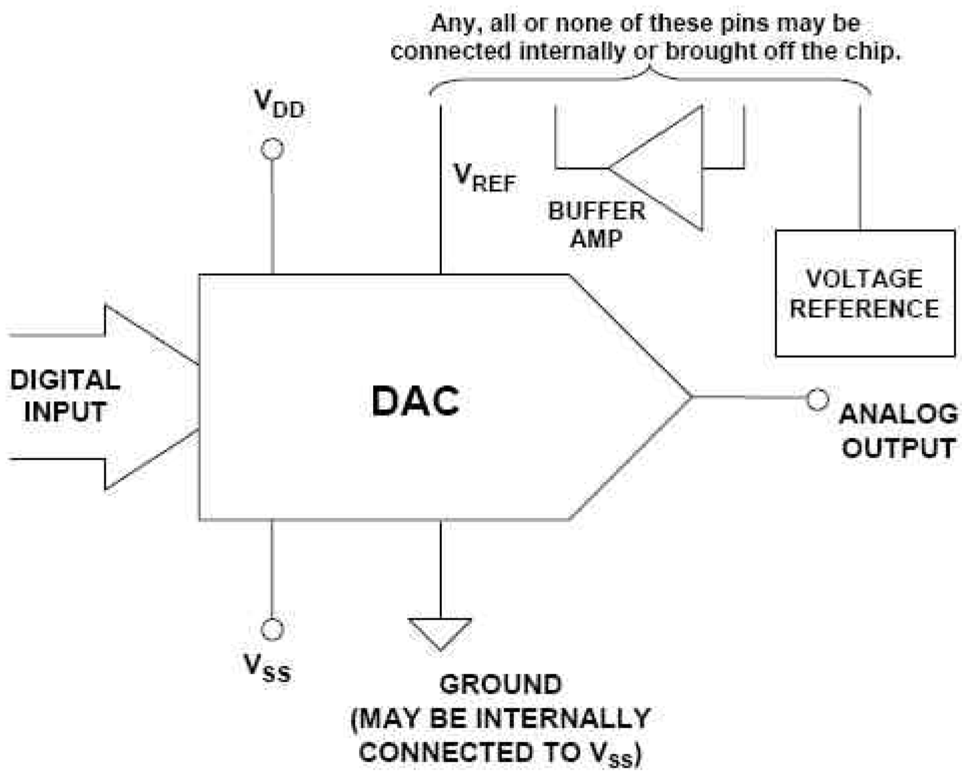


Figure 3.2: *DAC with Reference and Buffer*

Figures from Chapter 3: Data Converter Architectures in *Analog-Digital Conversion* by Walt Kester, Analog Devices Inc.

Notes

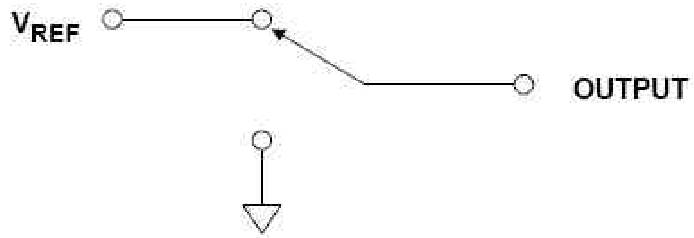


Figure 3.3: *1-Bit DAC: Changeover Switch (Single-Pole, Double Throw, SPDT)*

Notes

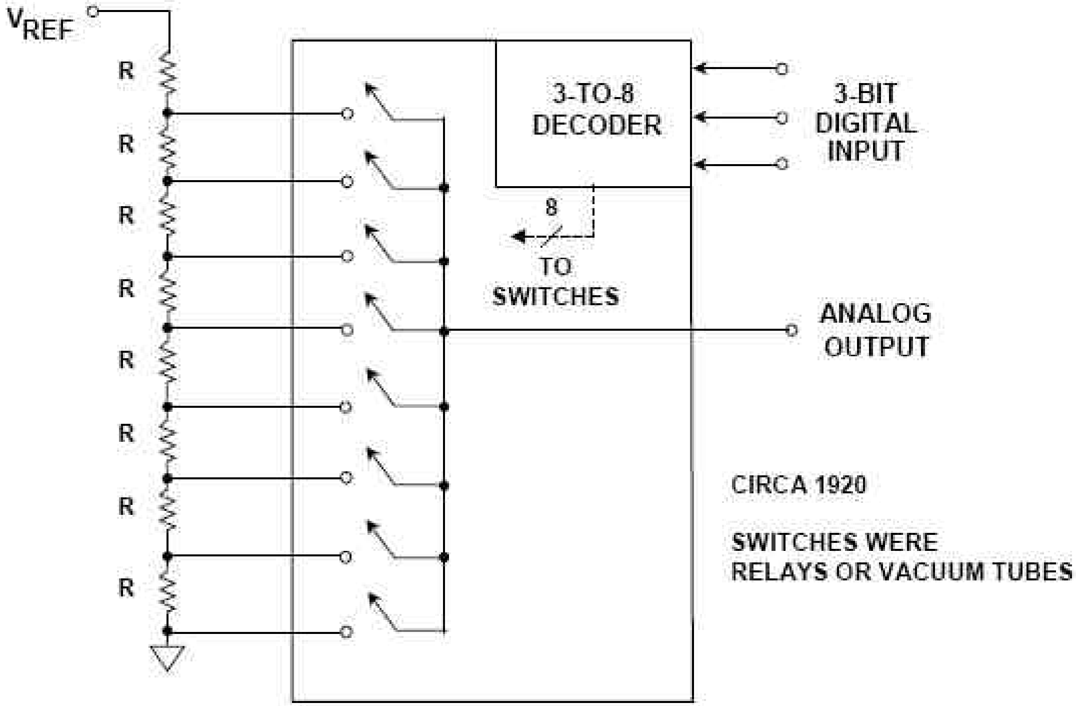


Figure 3.4: *Simplest Voltage-Output Thermometer DAC: The Kelvin Divider ("String DAC")*

Notes

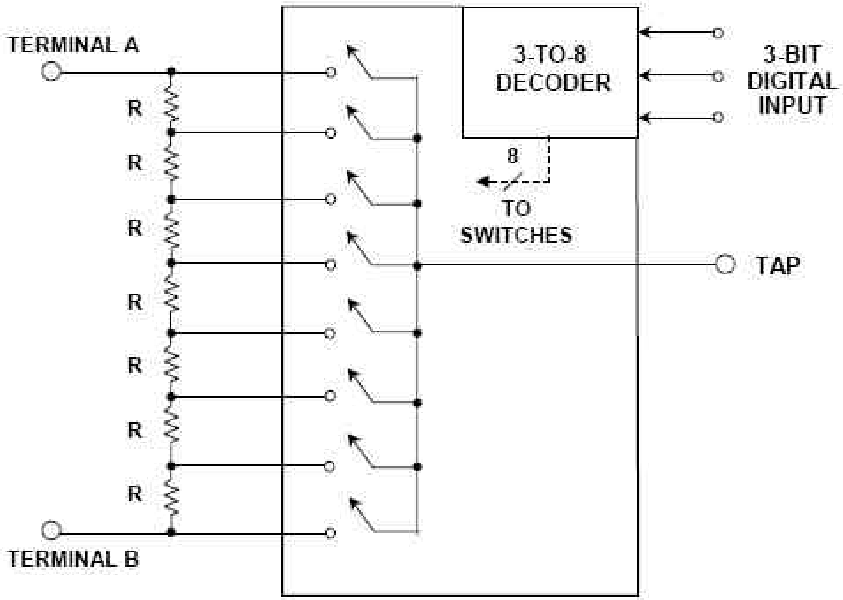


Figure 3.5: *A Slight Modification to a String DAC Yields a "Digital Potentiometer"*

Notes

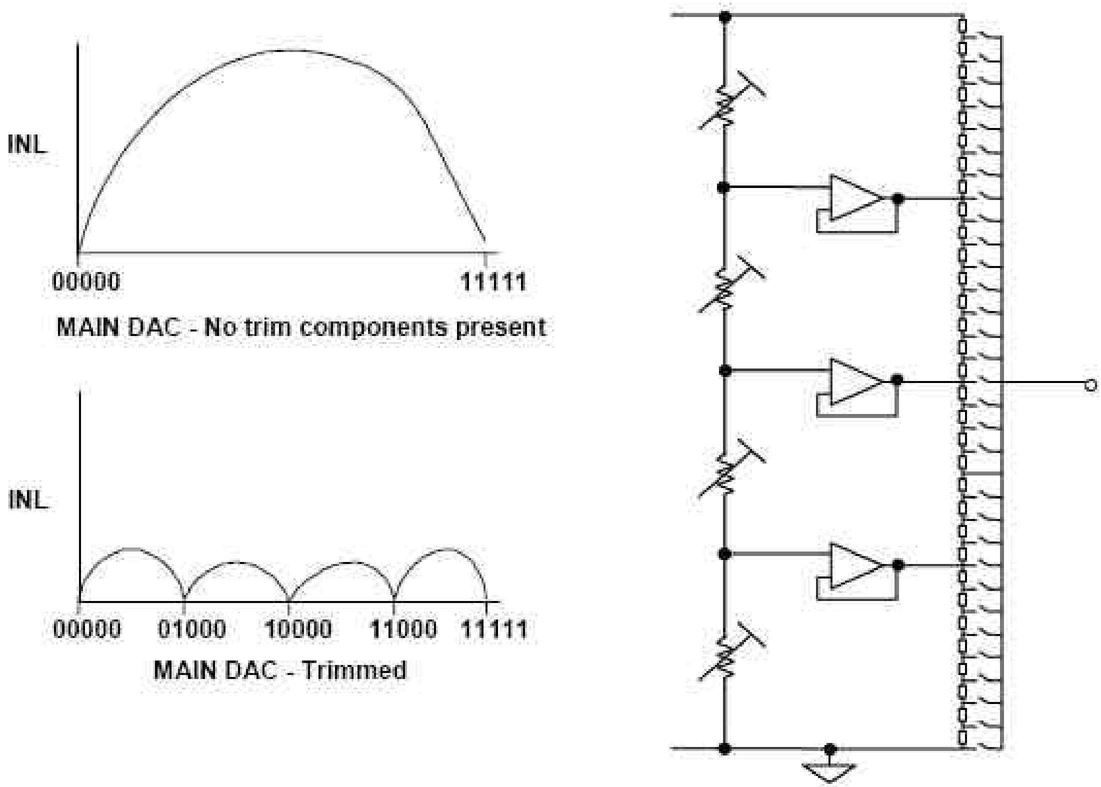


Figure 3.6: *Trimming the INL of a String DAC (If Required)*

Notes

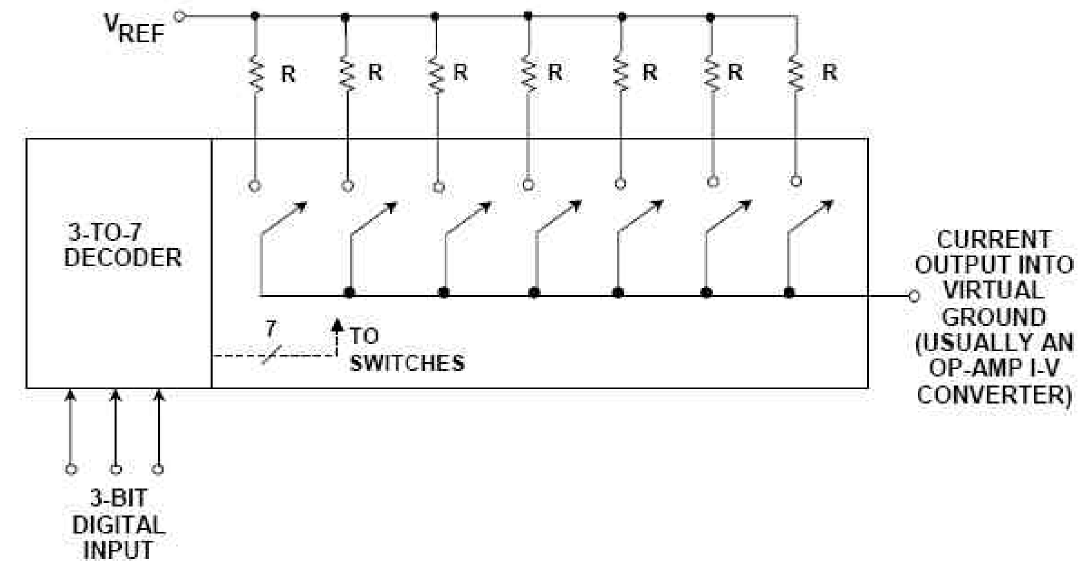


Figure 3.7: *The Simplest Current-Output Thermometer (Fully-Decoded) DAC*

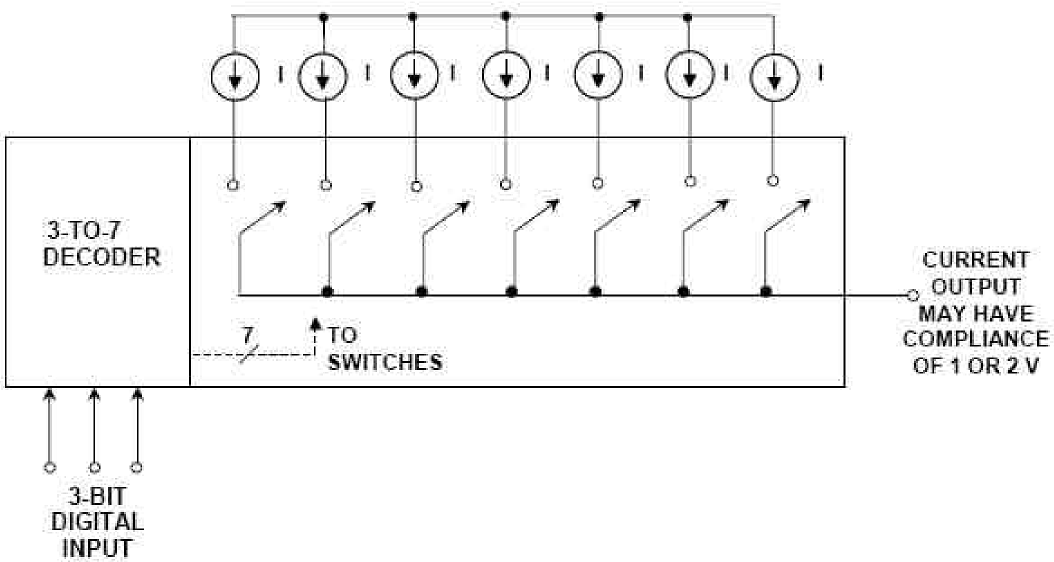


Figure 3.8: *Current Sources Improve the Basic Current-Output Thermometer DAC*

Notes

Notes

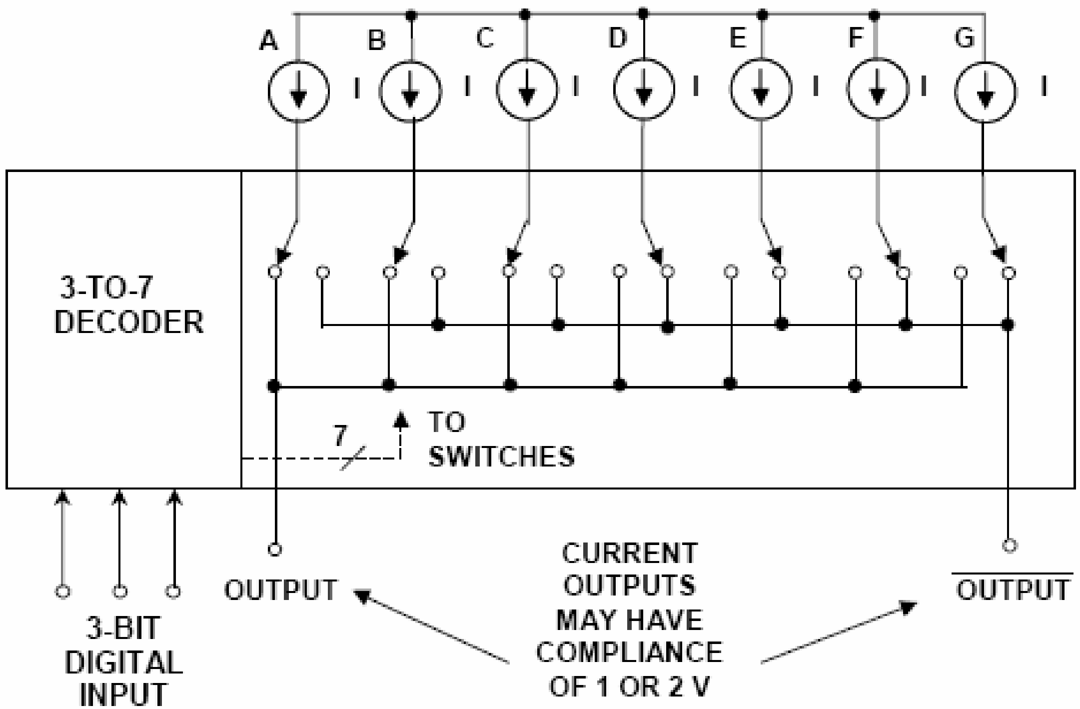
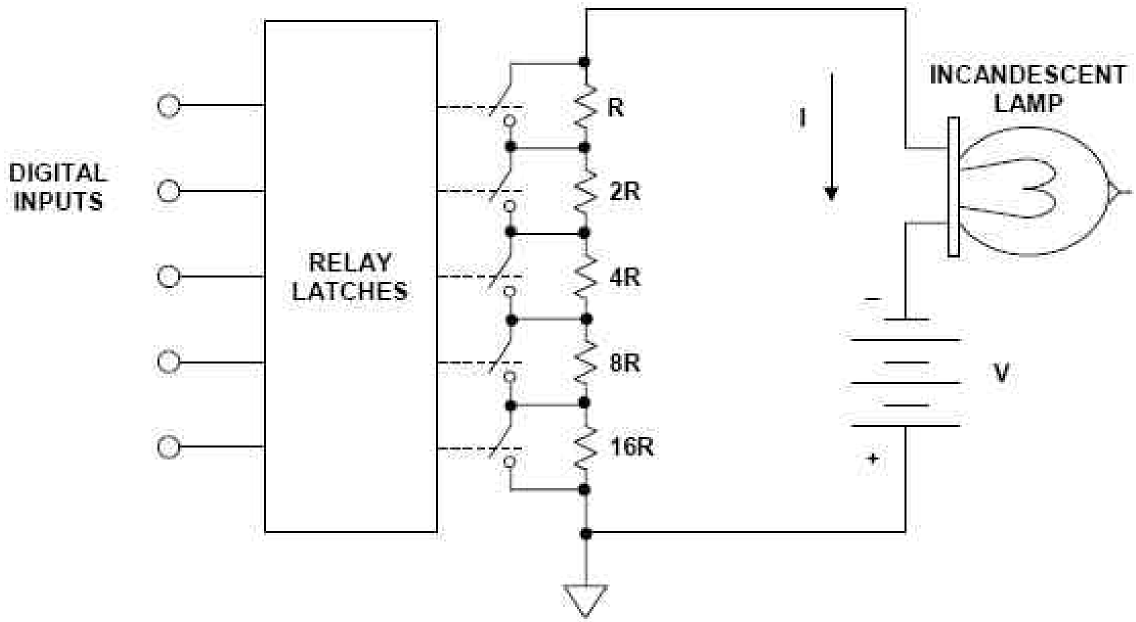


Figure 3.9: *High Speed Thermometer DAC with Complementary Current Outputs*

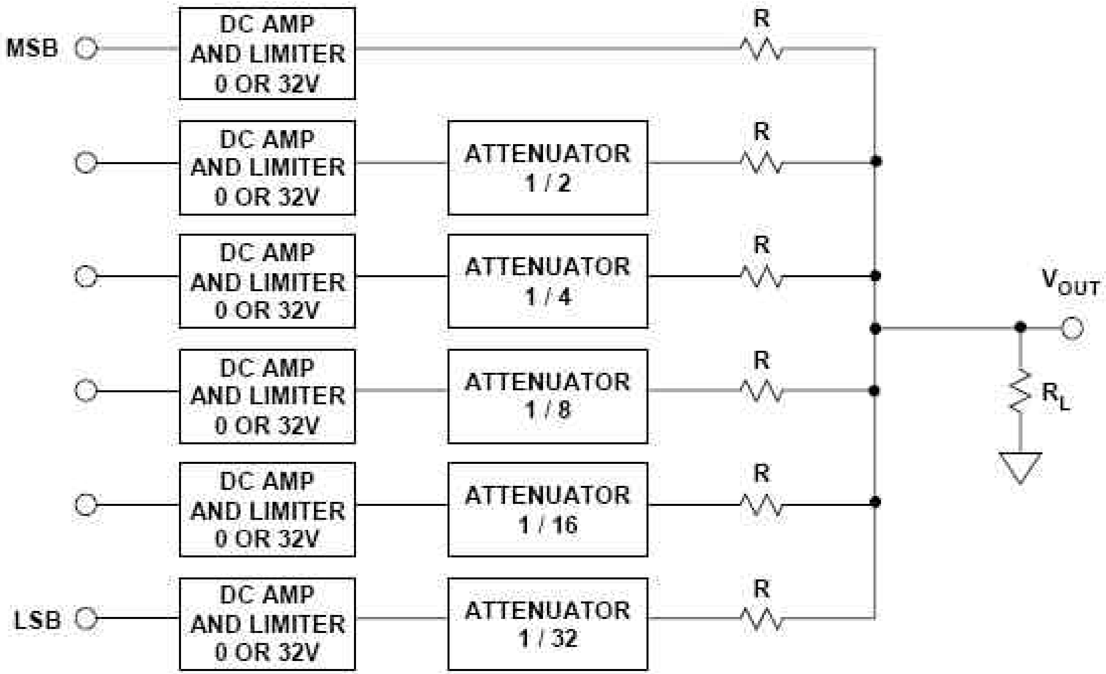


Adapted from: Paul M. Rainey, "Facsimile Telegraph System,"
U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926

Figure 3.10: *Paul M. Rainey's 5-Bit Binary-Weighted DAC*

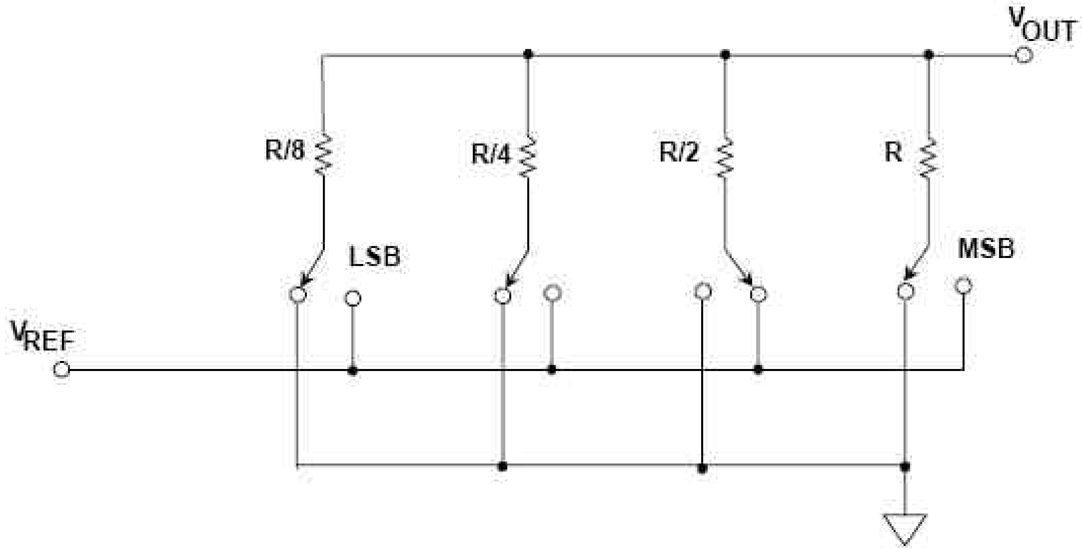
Notes

Notes



Adapted from: John C. Schelleng, "Code Modulation Communication System," U.S. Patent 2,453,461, Filed June 19, 1946, Issued November 9, 1948

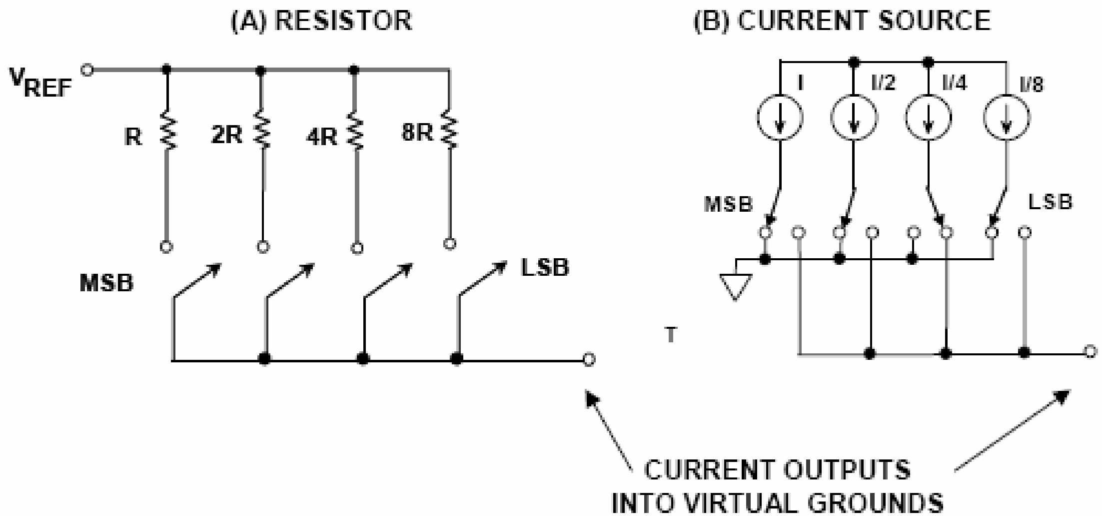
Figure 3.11: *John Schelleng's 6-Bit Binary-Weighted DAC*



Adapted from: B. D. Smith, "Coding by Feedback Methods," Proceedings of the I. R. E., Vol. 41, August 1953, pp. 1053-1058

Figure 3.12: *Voltage-mode Binary-Weighted Resistor DAC*

Notes



◆ DIFFICULT TO FABRICATE IN IC FORM DUE TO LARGE RESISTOR OR CURRENT RATIOS FOR HIGH RESOLUTIONS

Figure 3.13: *Current-Mode Binary-Weighted DACs*

Notes

Notes

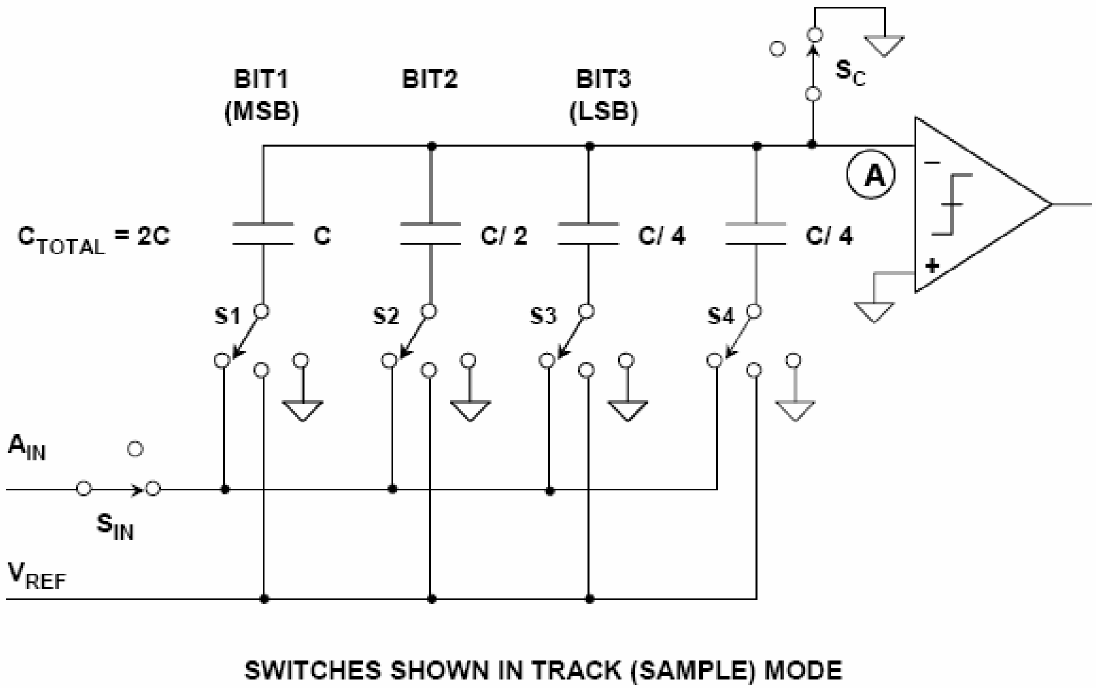


Figure 3.14: *Capacitive Binary-Weighted DAC in Successive Approximation ADC*

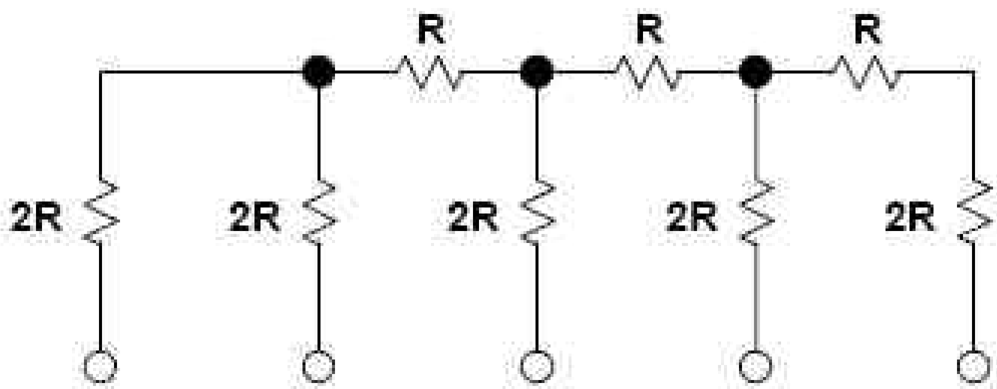
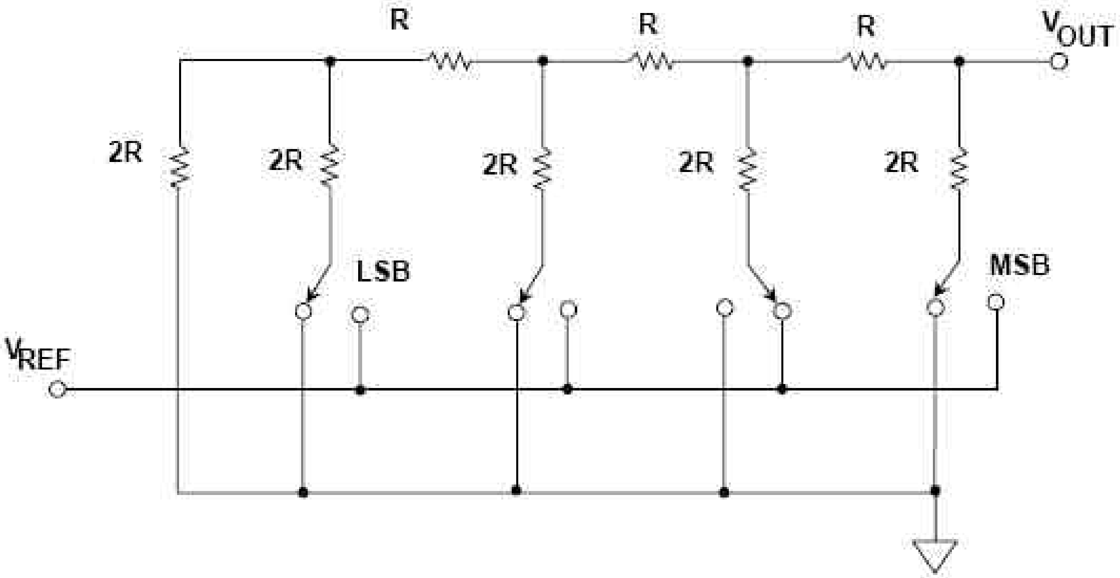


Figure 3.15: *4-Bit R-2R Ladder Network*

Notes

Notes



Adapted from: B. D. Smith, "Coding by Feedback Methods," Proceedings of the I. R. E., Vol. 41, August 1953, pp. 1053-1058

Figure 3.16: *Voltage-Mode R-2R Ladder Network DAC*

Notes

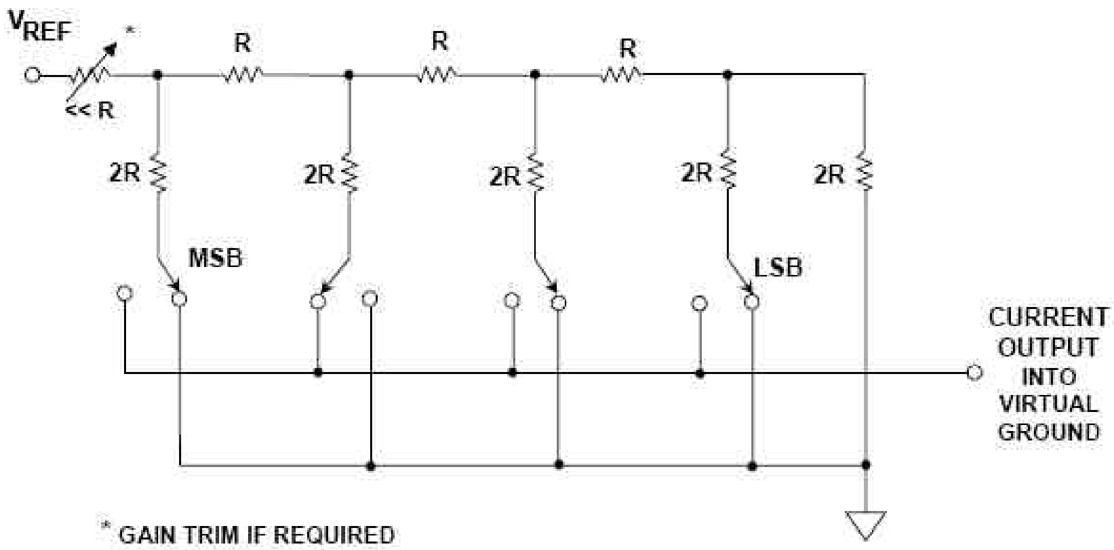
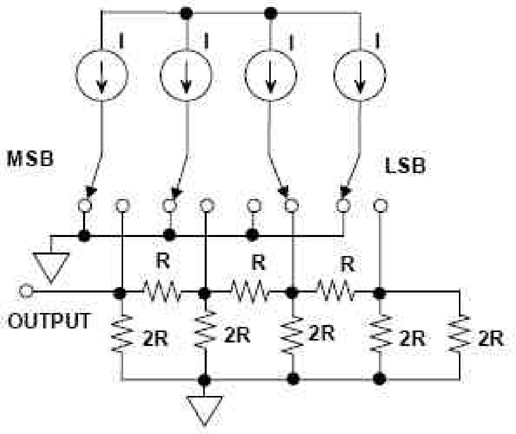


Figure 3.17: *Current-Mode R-2R Ladder Network DAC*

Notes



Adapted from: Bernard M. Gordon and Robert P. Talambiras, "Signal Conversion Apparatus," U.S. Patent 3,108,266, filed July 22, 1955, issued October 22, 1963

Figure 3.18: *Equal Current Sources Switched into an R-2R Ladder Network*

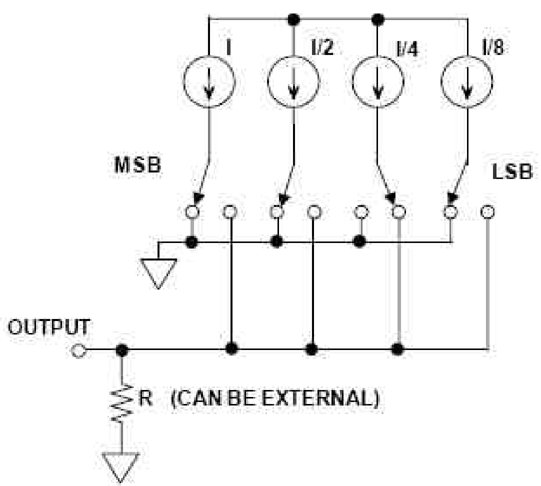


Figure 3.19: *Binary-Weighted Current Sources Switched into a Load*

Notes

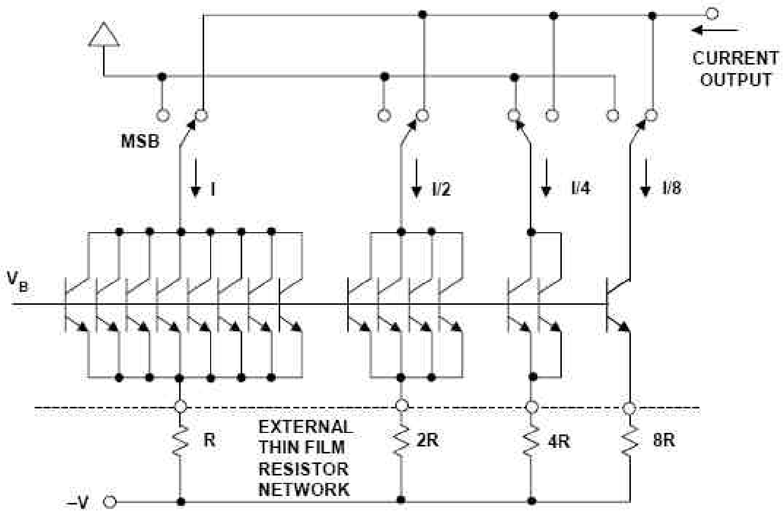


Figure 3.20: *Binary-Weighted 4-Bit DAC, the AD550 "µDAC" Quad Switch*

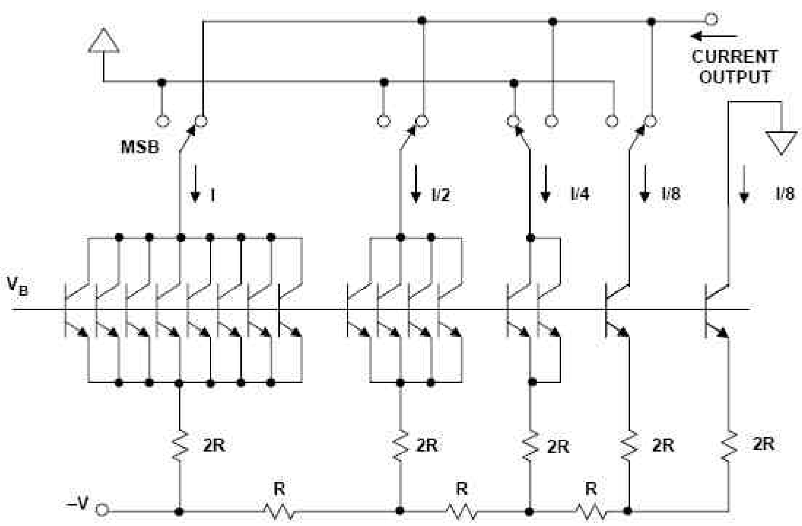


Figure 3.21: *Binary-Weighted 4-Bit DAC:*
R/2R Ladder Network Current Setting Resistors

Notes

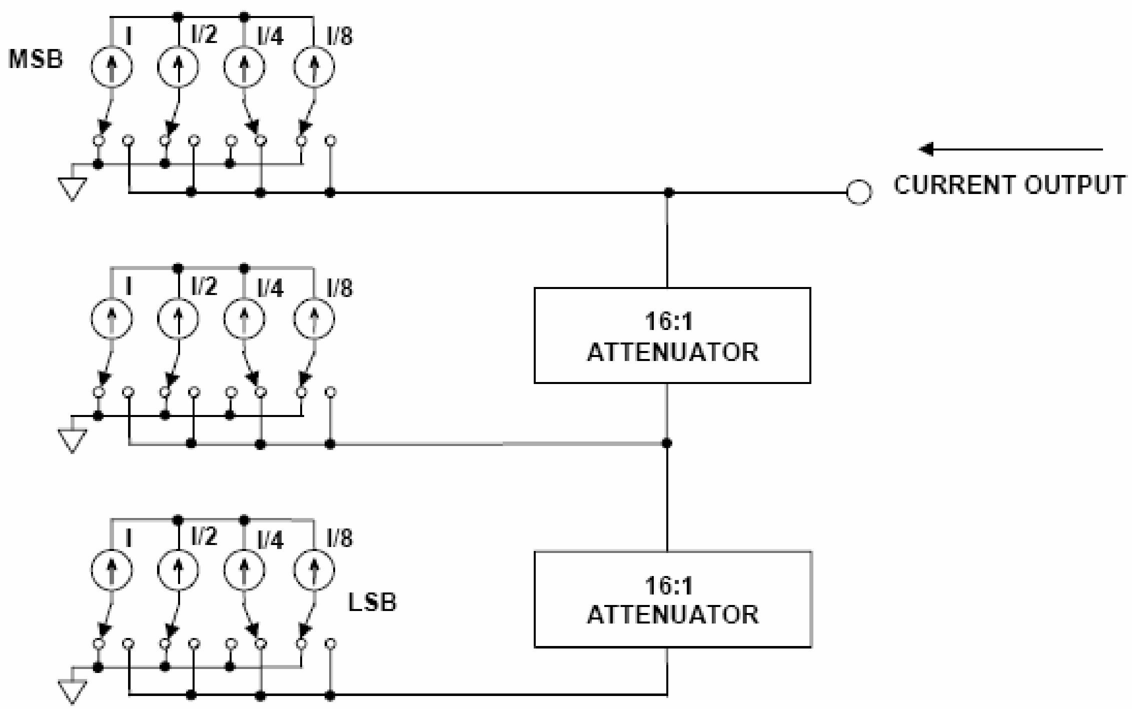
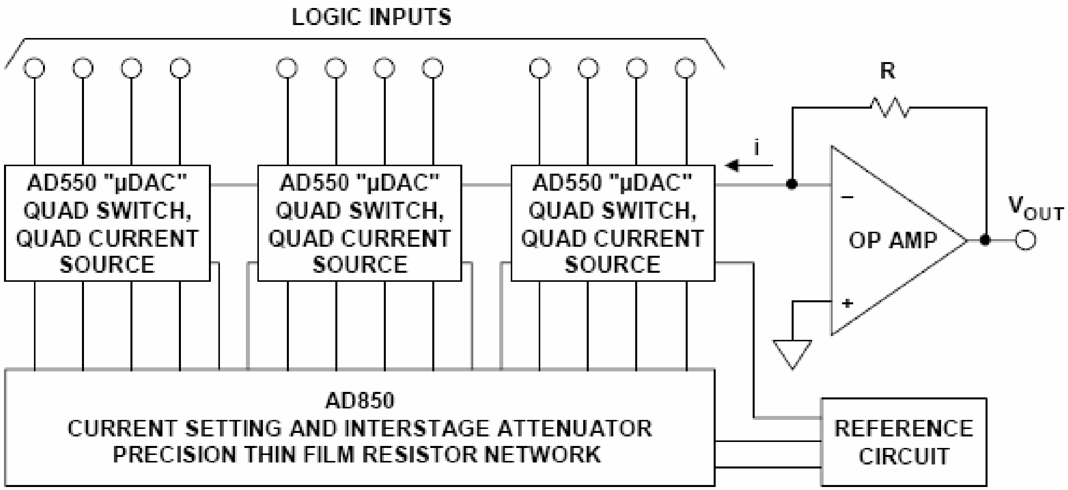


Figure 3.22: *12-Bit Current-Output DAC Using Cascaded Binary "Quad Switches"*



James J. Pastoriza, "Solid State Digital-to-Analog Converter,"
U.S. Patent 3,747,088, filed December 30, 1970, issued July 17, 1973

Figure 3.23: *A 1970 Vintage 12-Bit DAC Using Quad Current Switches, Thin Film Resistor Network, Op Amp, and Zener Diode Voltage Reference*

Notes

Notes

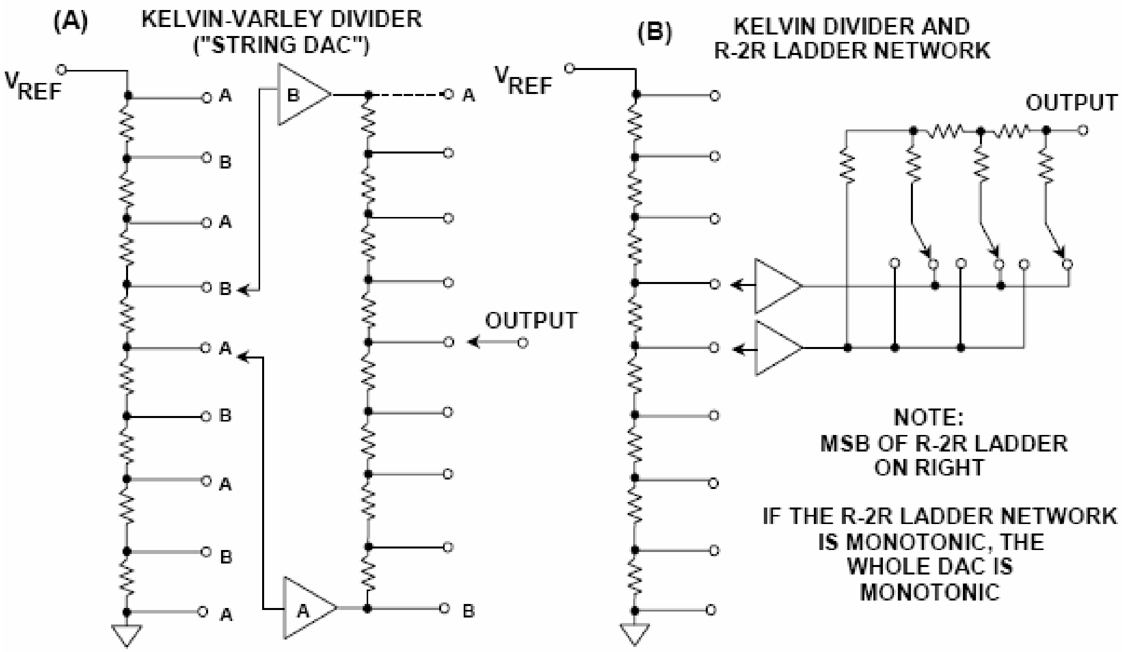
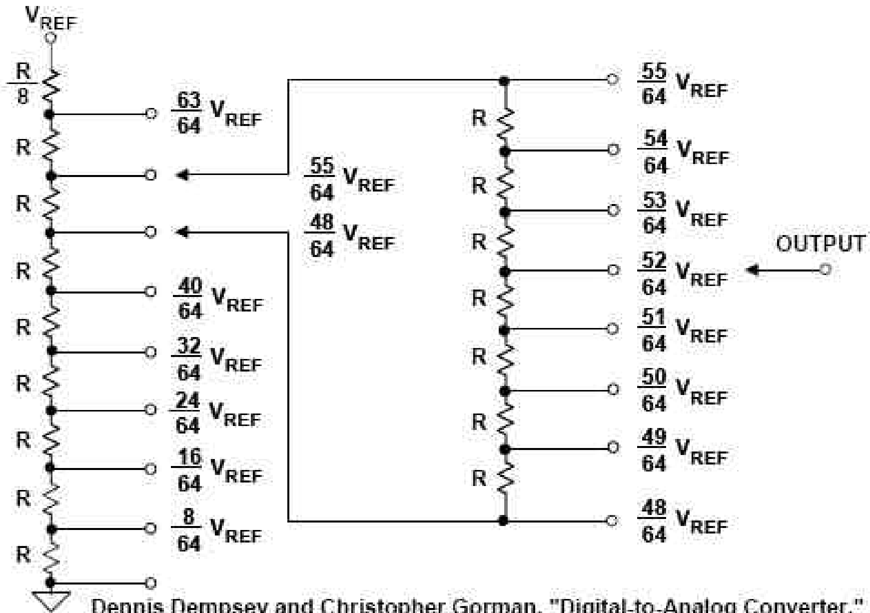


Figure 3.24: *Segmented Voltage-Output DACs*

Notes



Dennis Dempsey and Christopher Gorman, "Digital-to-Analog Converter," U.S. Patent 5,969,657, filed July 27, 1997, issued October 19, 1999.

Figure 3.25: *Segmented Unbuffered String DACs Use Patented Architecture*

Notes

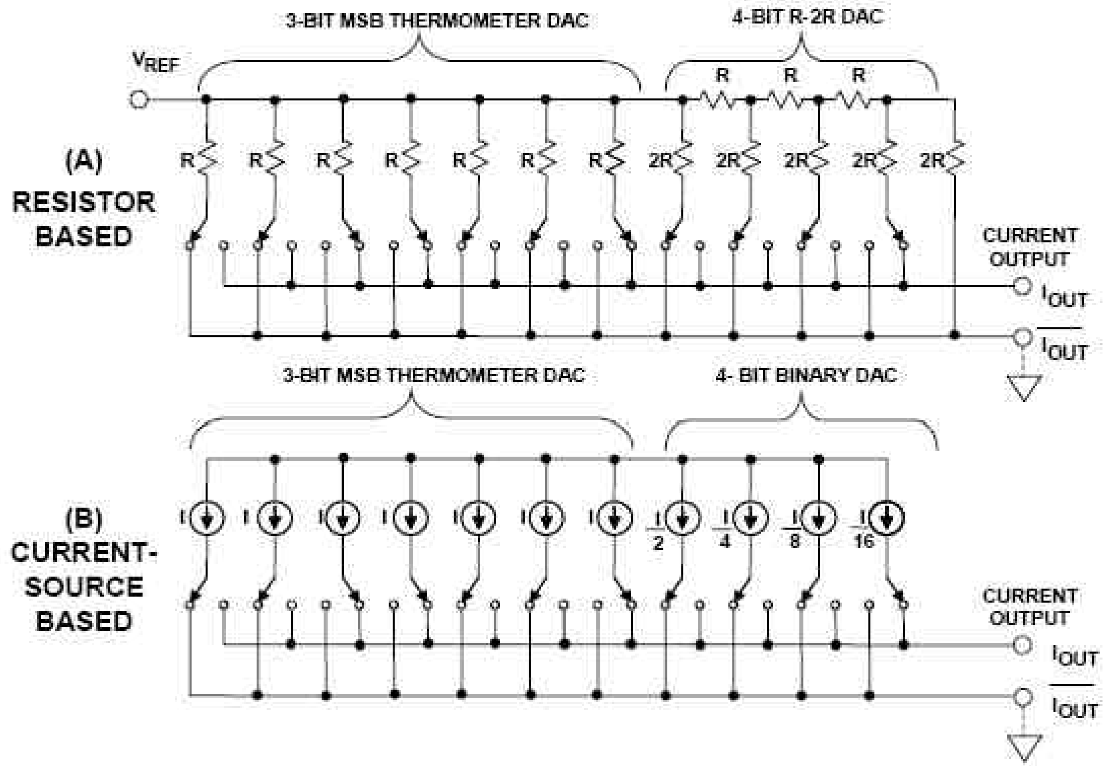


Figure 3.26: *Segmented Current-Output DACs: (A) Resistor-Based, (B) Current-source based*

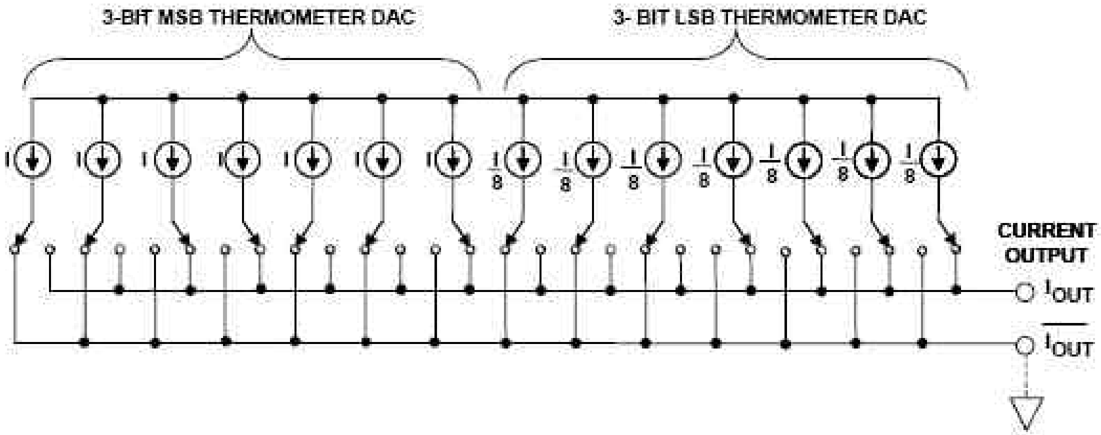


Figure 3.27: *6-Bit Current-Output Segmented DAC Based on Two 3-Bit Thermometer DACs*

Notes

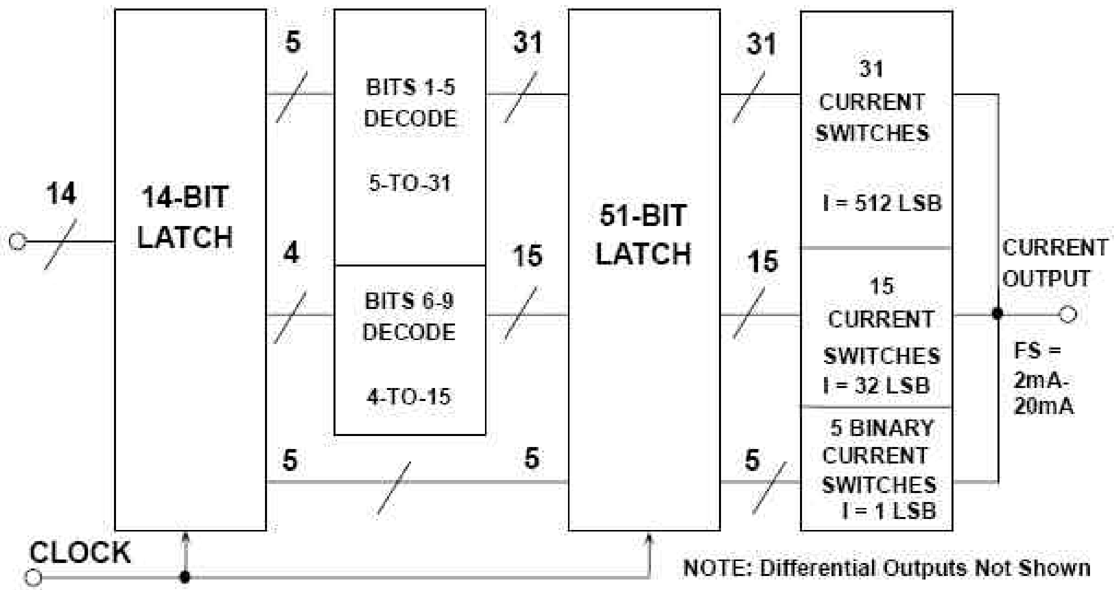


Figure 3.28: *AD9775 TxDAC® 14-Bit CMOS DAC Core*

Notes

Notes

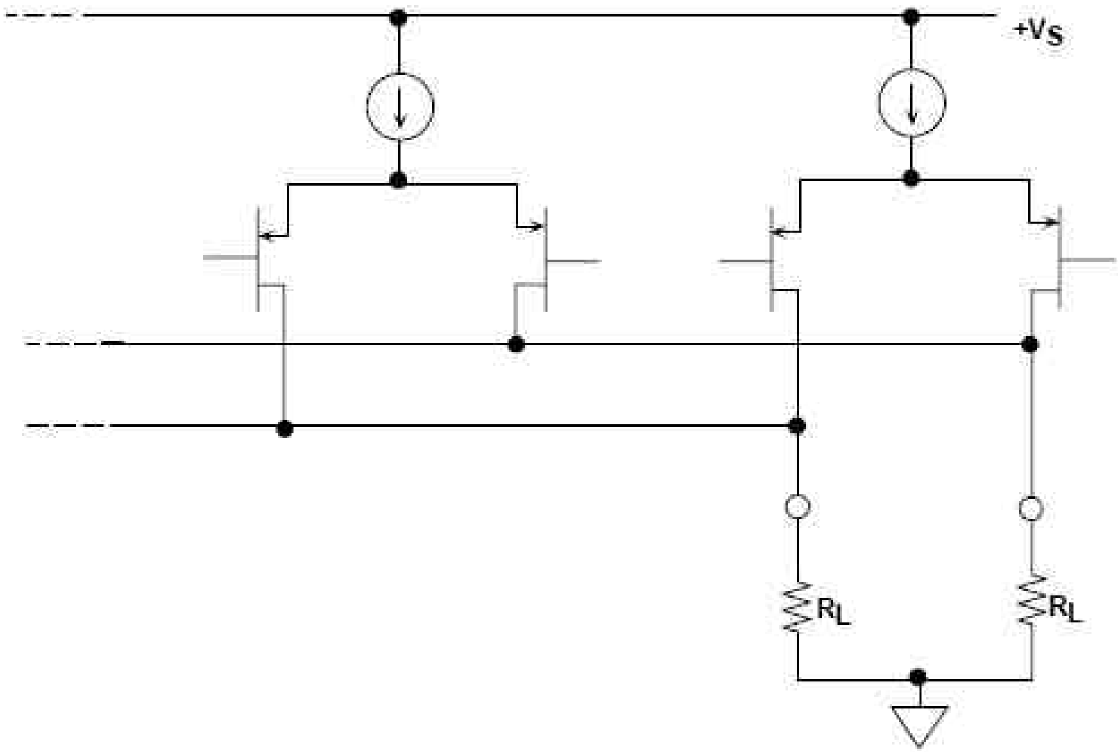


Figure 3.29: *PMOS Transistor Current Switches*

Notes

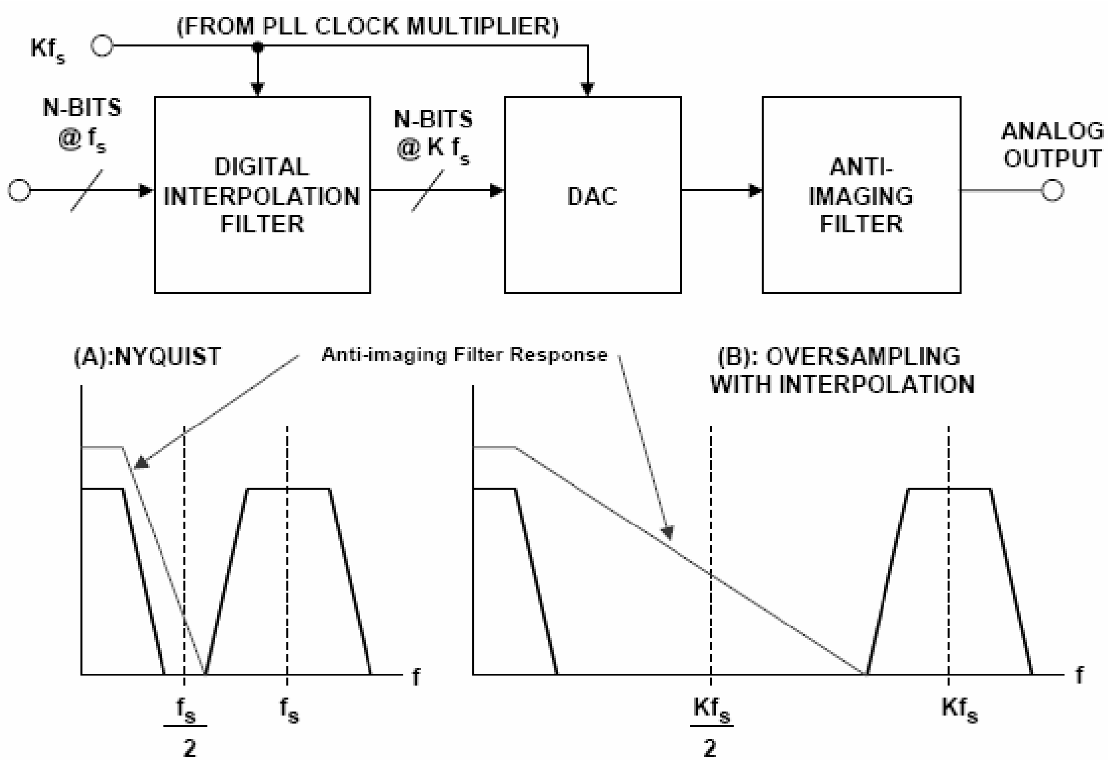
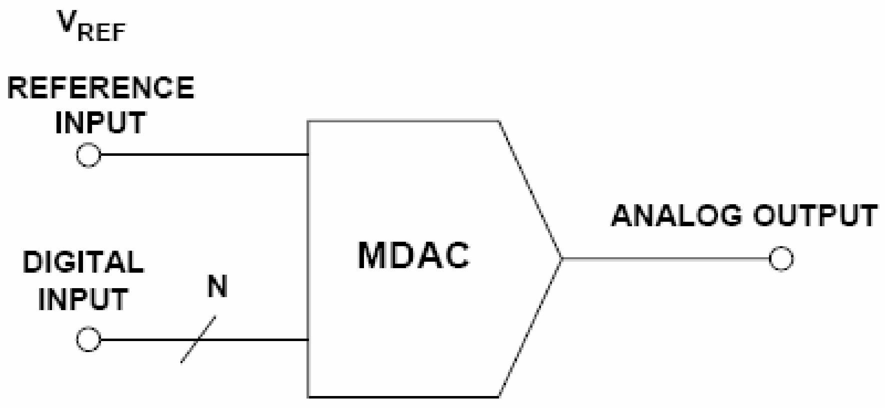


Figure 3.30: *Oversampling Interpolating DAC*

Notes



ANALOG OUPTUT = V_{REF} × DIGITAL INPUT × CONSTANT

DIFFICULT TO MAINTAIN DIFFERENTIAL LINEARITY AS V_{REF} APPROACHES ZERO

Figure 3.31: *Multiplying DAC ("MDAC")*

Notes

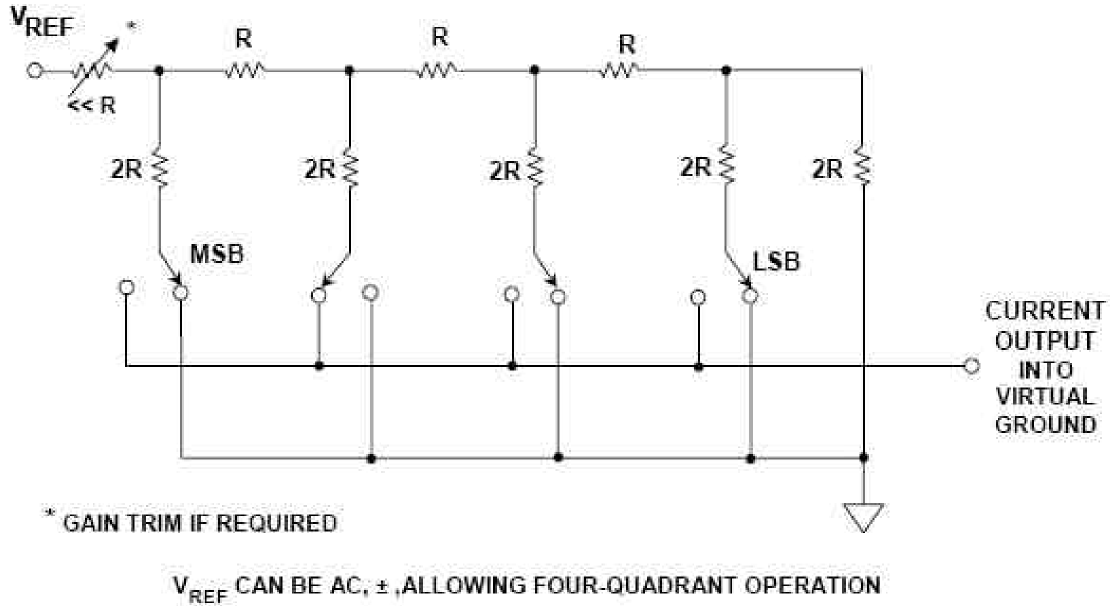


Figure 3.32: *Multiplying DAC Using Current-Mode R-2R Ladder Network and CMOS switches.*

Notes

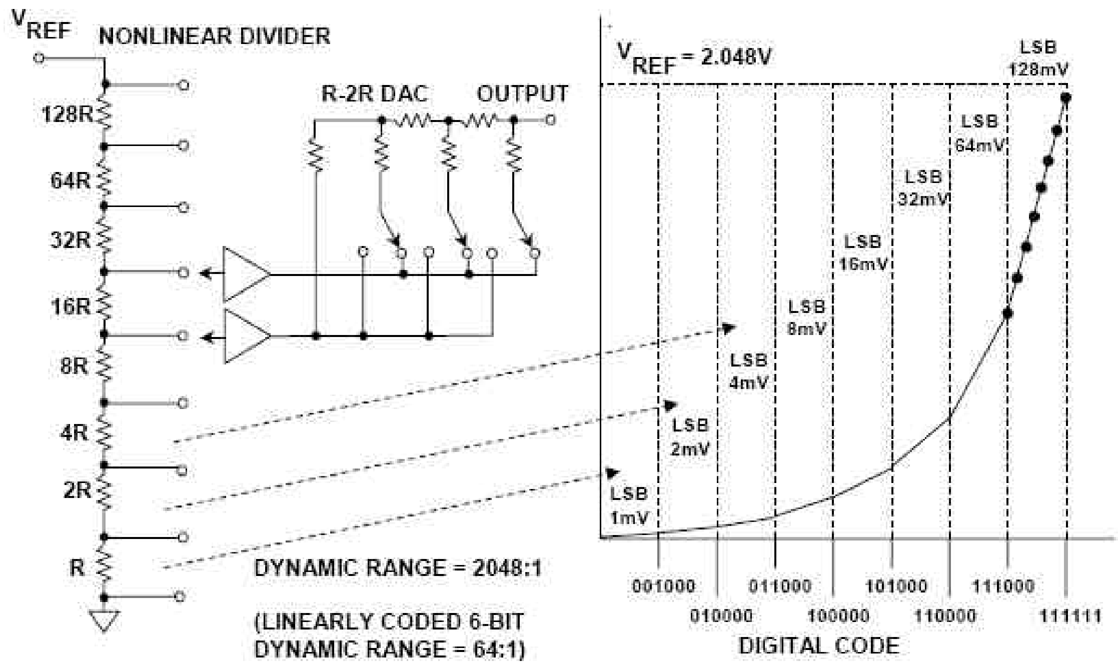


Figure 3.33: *Nonlinear 6-Bit Segmented DAC*

Notes

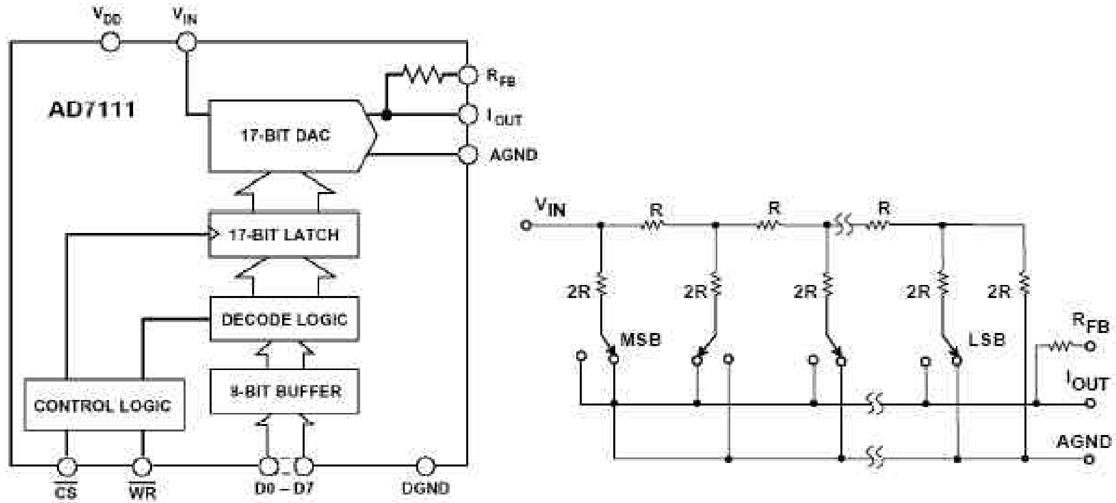


Figure 3.34: *AD7111 LOGDAC® (Released 1982)*

Notes

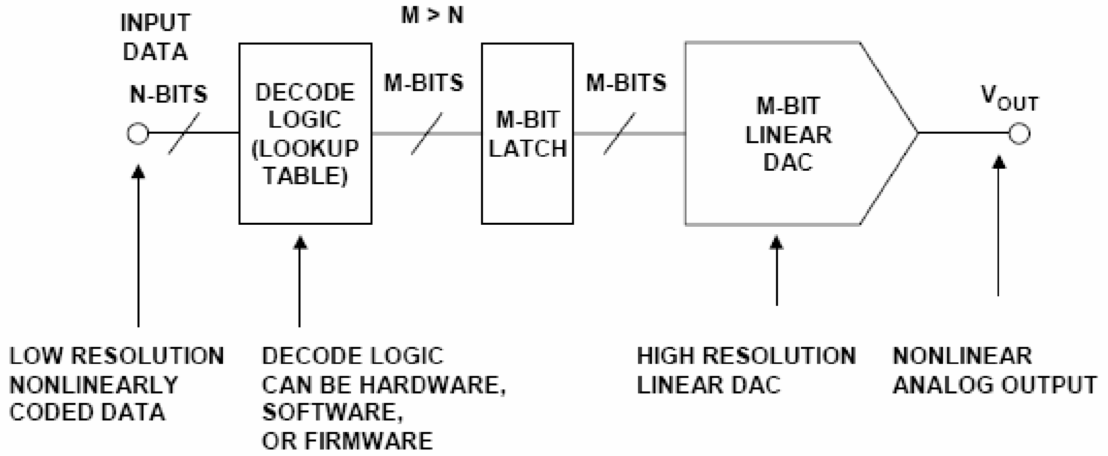


Figure 3.35: *General Nonlinear DAC*

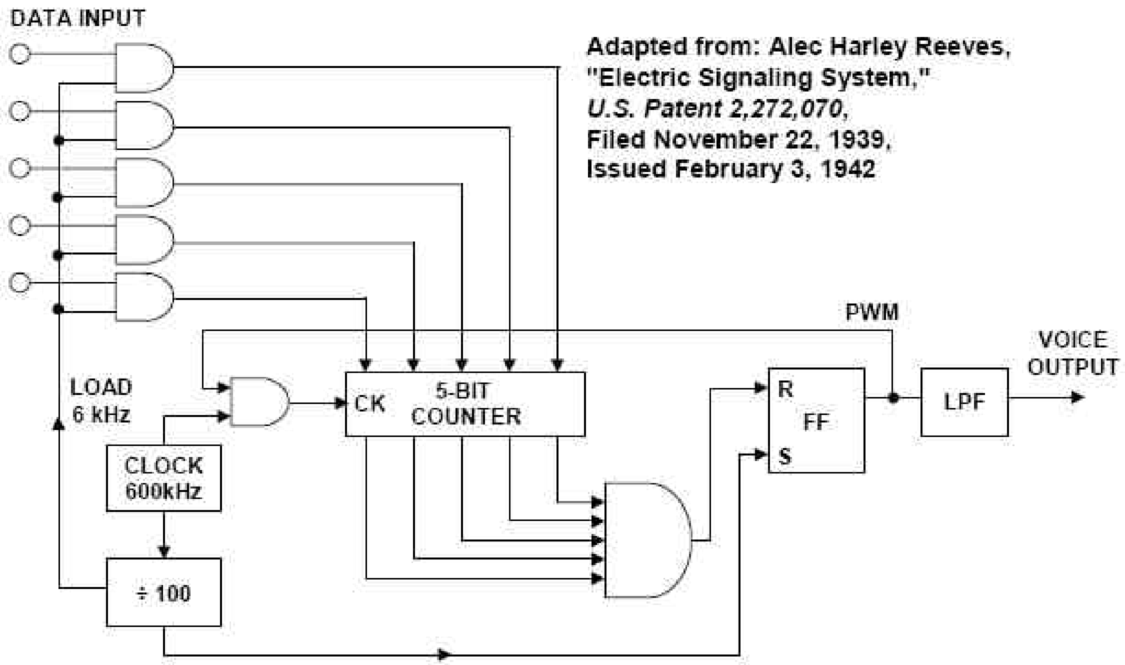


Figure 3.36: *A.H. Reeves' 5-Bit Counting DAC*

Notes

Notes

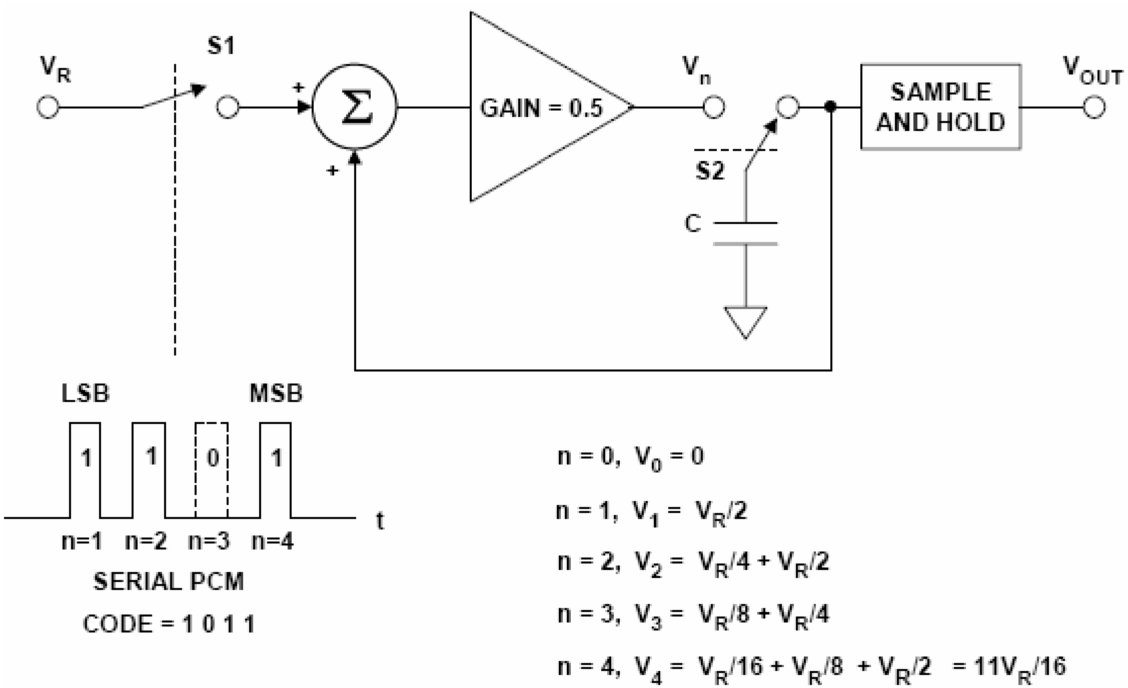


Figure 3.37: *4-Bit Cyclic Serial DAC*

Notes

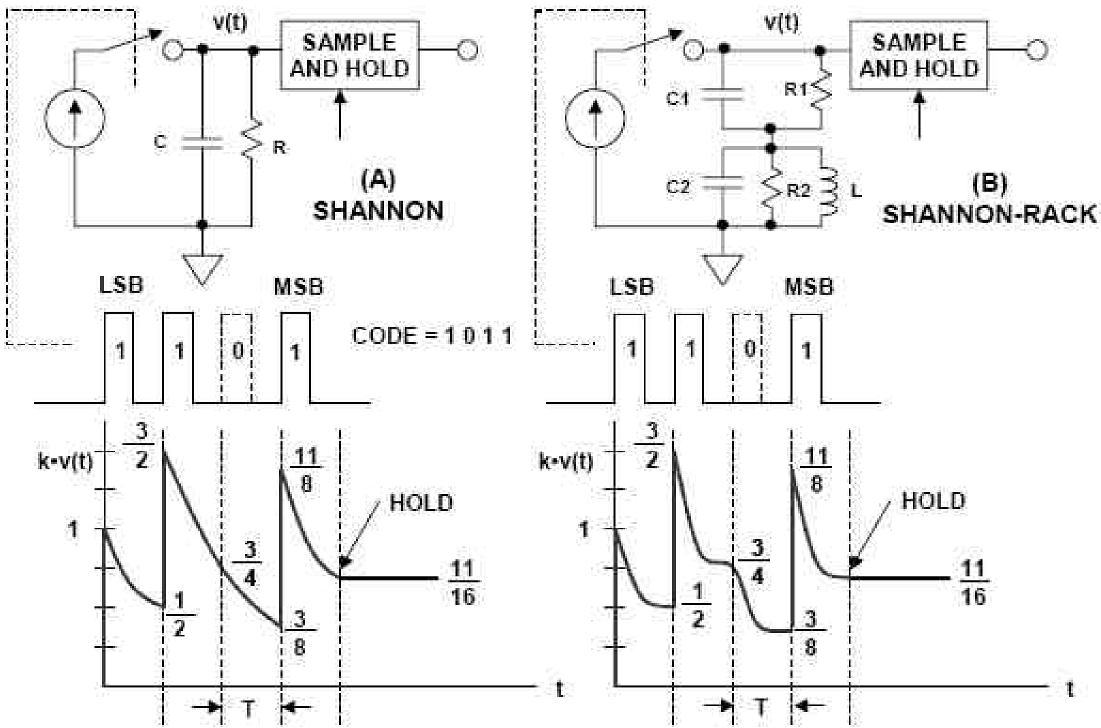


Figure 3.38: *Shannon and Shannon-Rack Decoder*

Notes

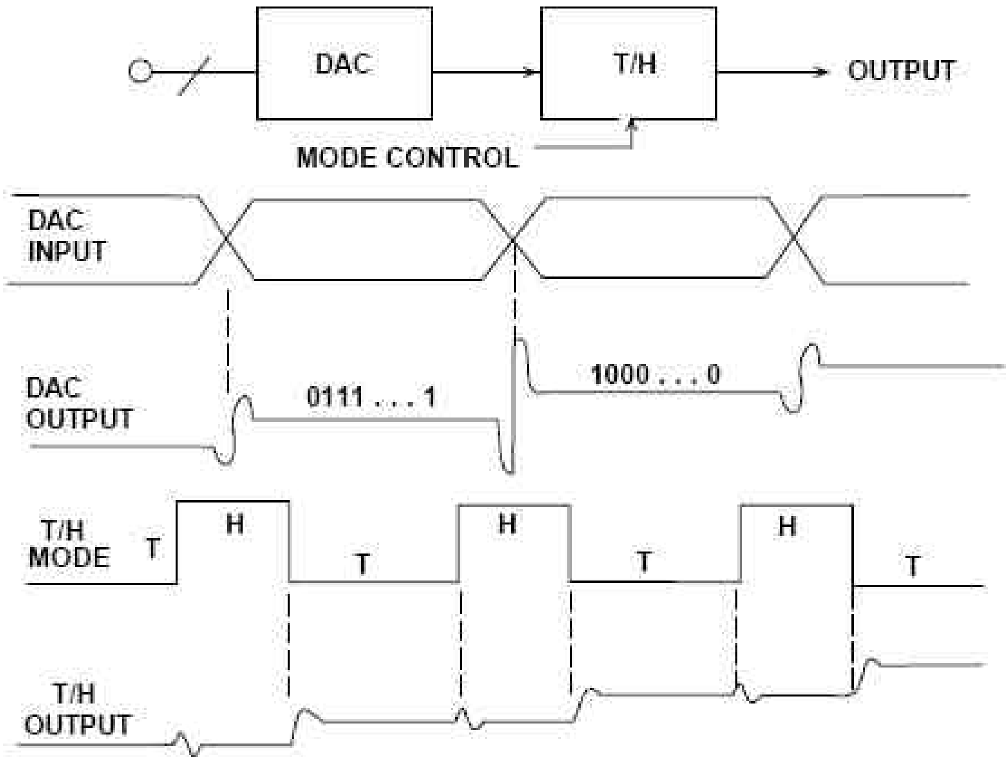
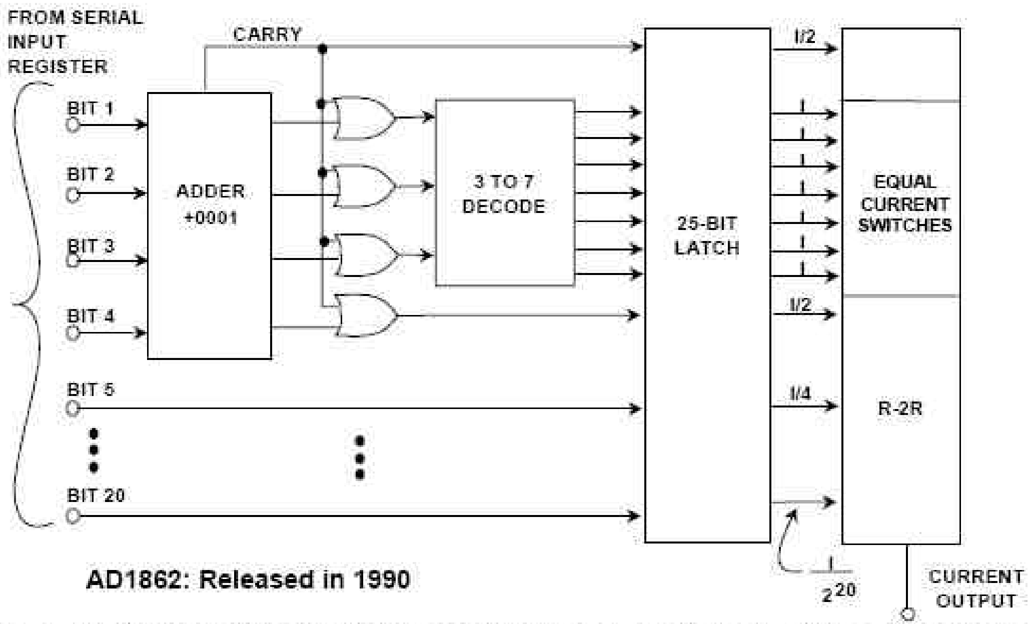


Figure 3.39: *Deglitching DAC Outputs Using a Track-and-Hold*

Notes



AD1862: Released in 1990

Figure 3.40: *Digital Offset Minimizes Mid-Scale Distortion of Small Signals*

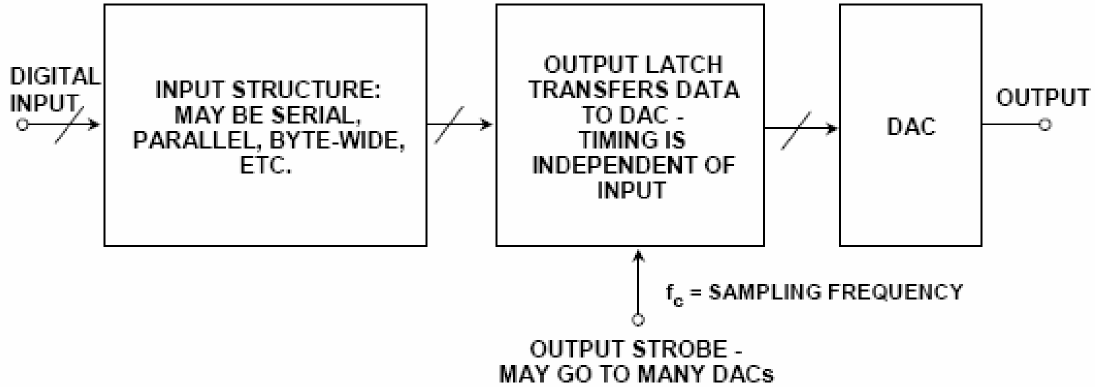


Figure 3.41: *Double-Buffered DAC Permits Complex Input Structures and Simultaneous Update*

Notes

Notes

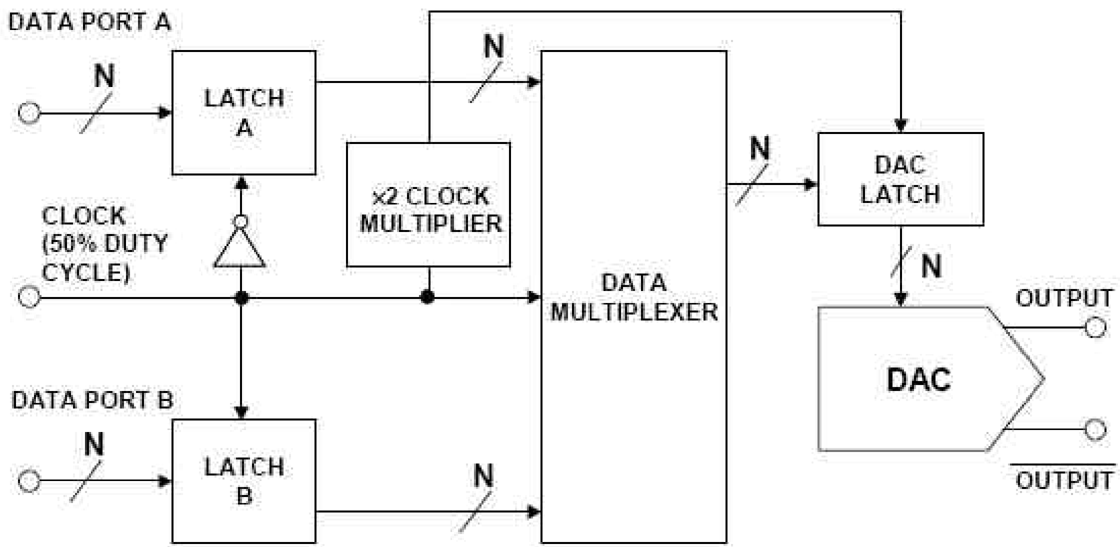


Figure 3.42: *Alternate Loading (Ping-Pong) High Speed DAC*

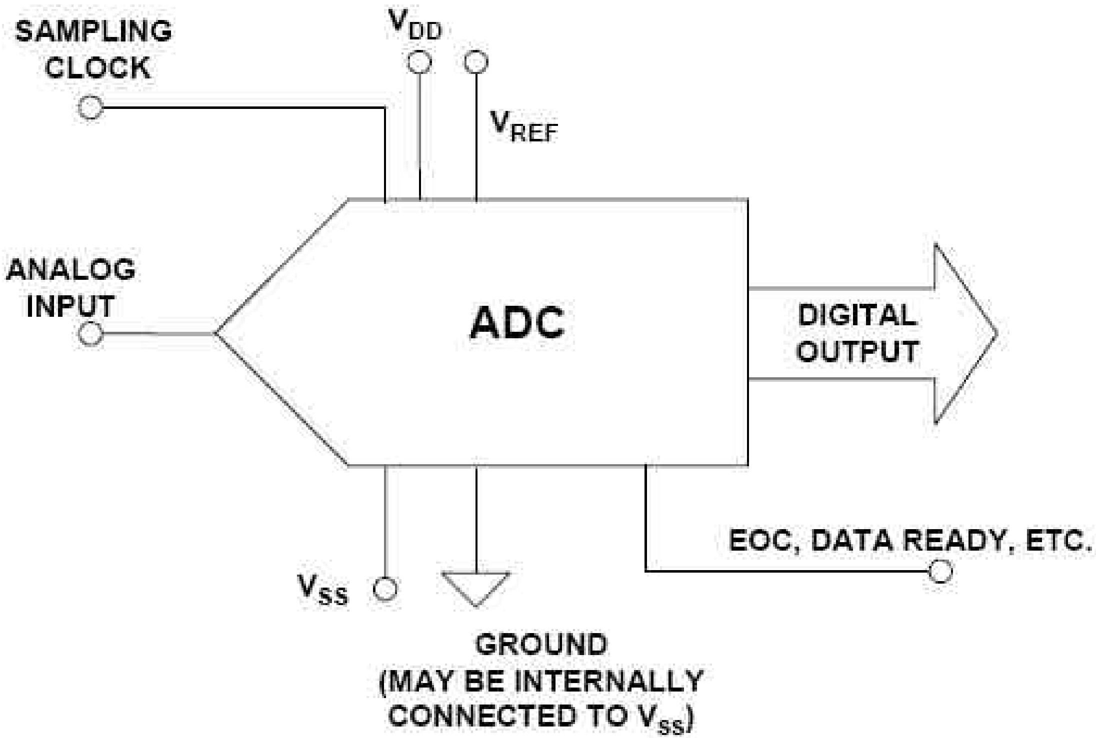


Figure 3.43: *Basic ADC with External Reference*

Notes

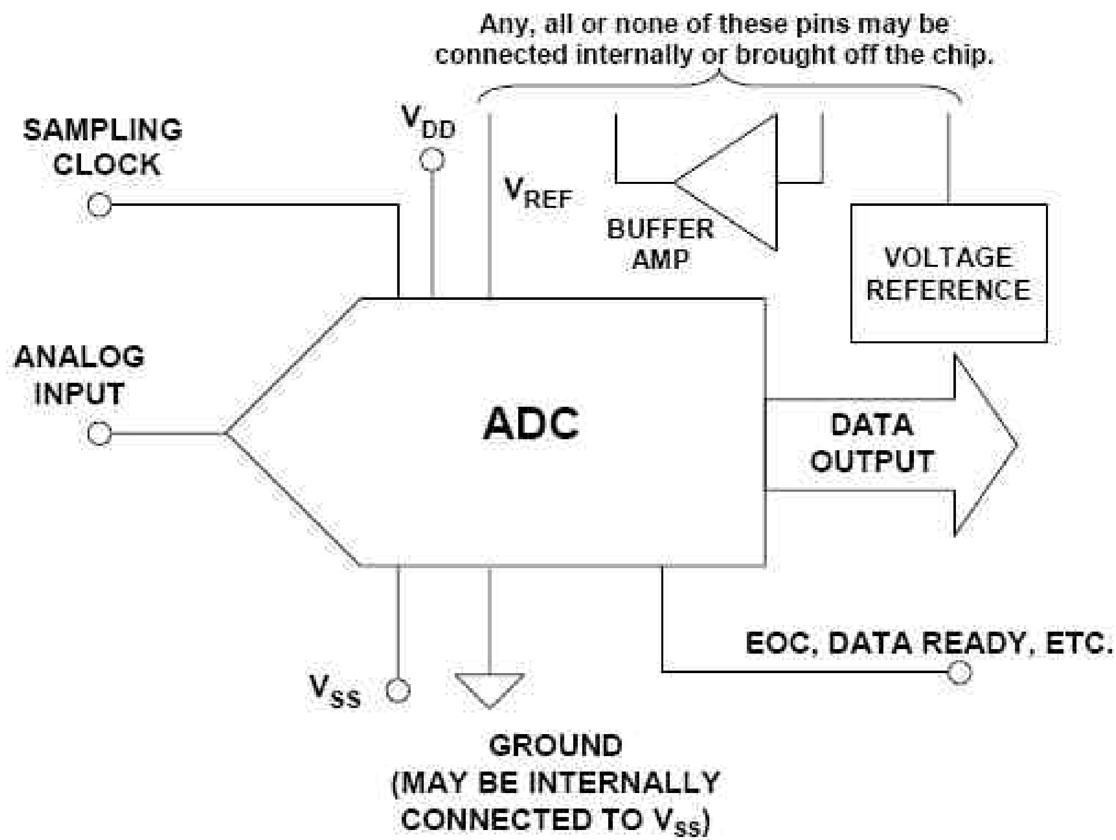


Figure 3.44: *ADC with Reference and Buffer*

Notes

Figures from Chapter 3: Data Converter Architectures in *Analog-Digital Conversion* by Walt Kester, Analog Devices Inc.

Notes

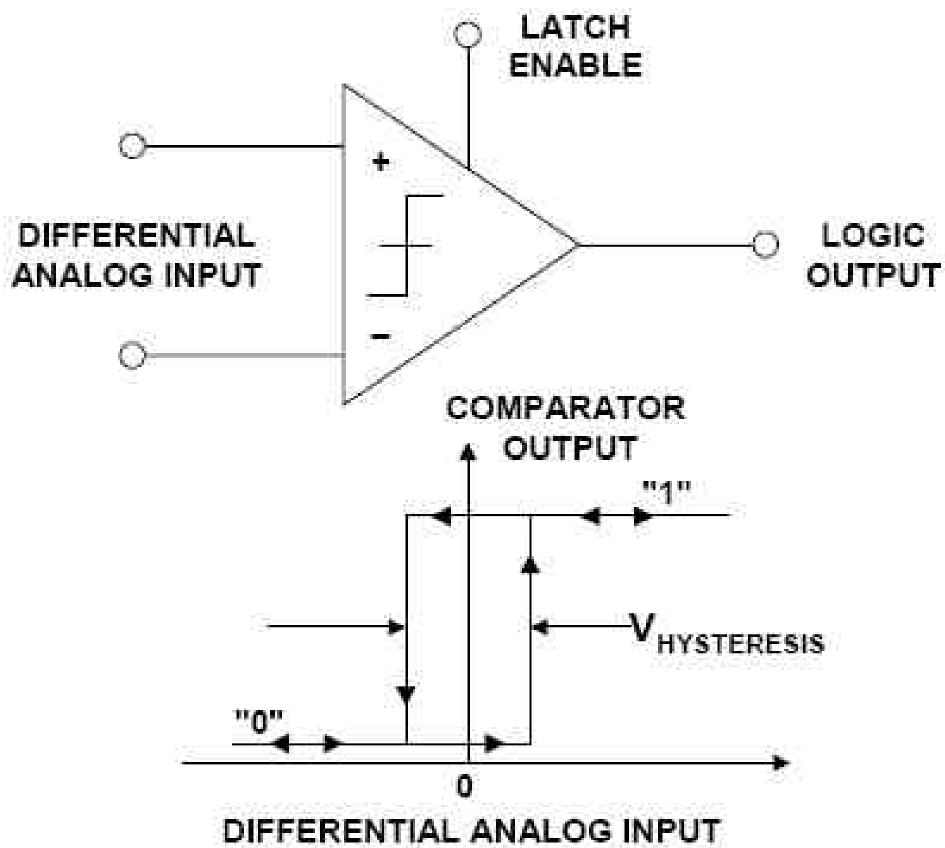
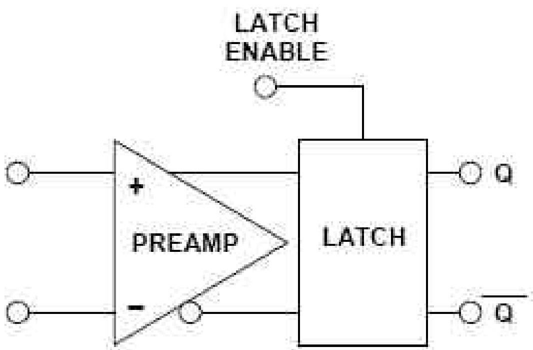
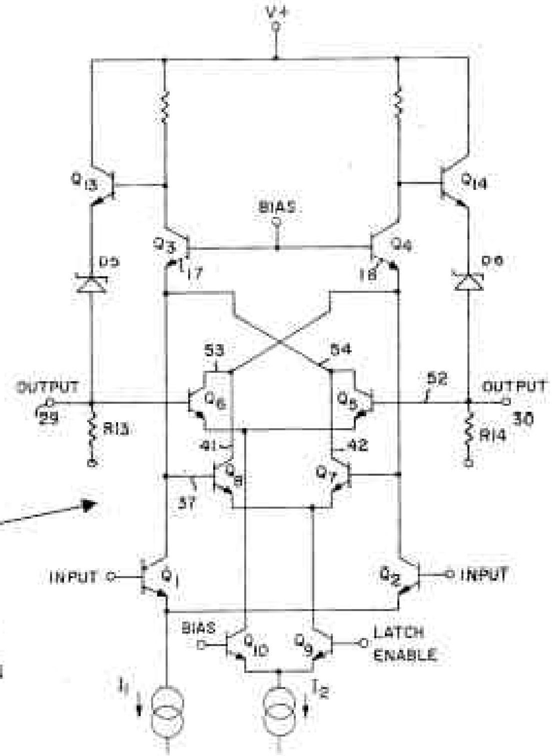


Figure 3.45: *The Comparator: A 1-Bit ADC*

Notes





From James N. Giles, "High Speed Transistor Difference Amplifier," U.S. Patent 3,843,934, filed January 31 1973, issued October 22, 1974

Figure 3.46: *The AM685 ECL Comparator (1972)*

Notes

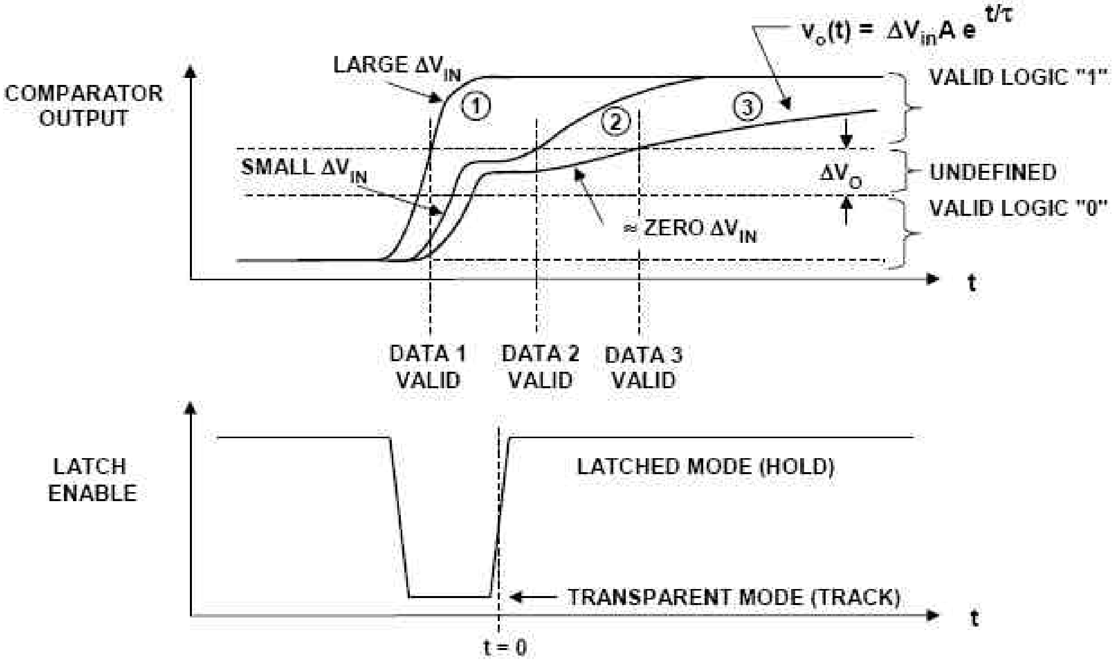


Figure 3.47: *Comparator Metastable State Errors*

Notes

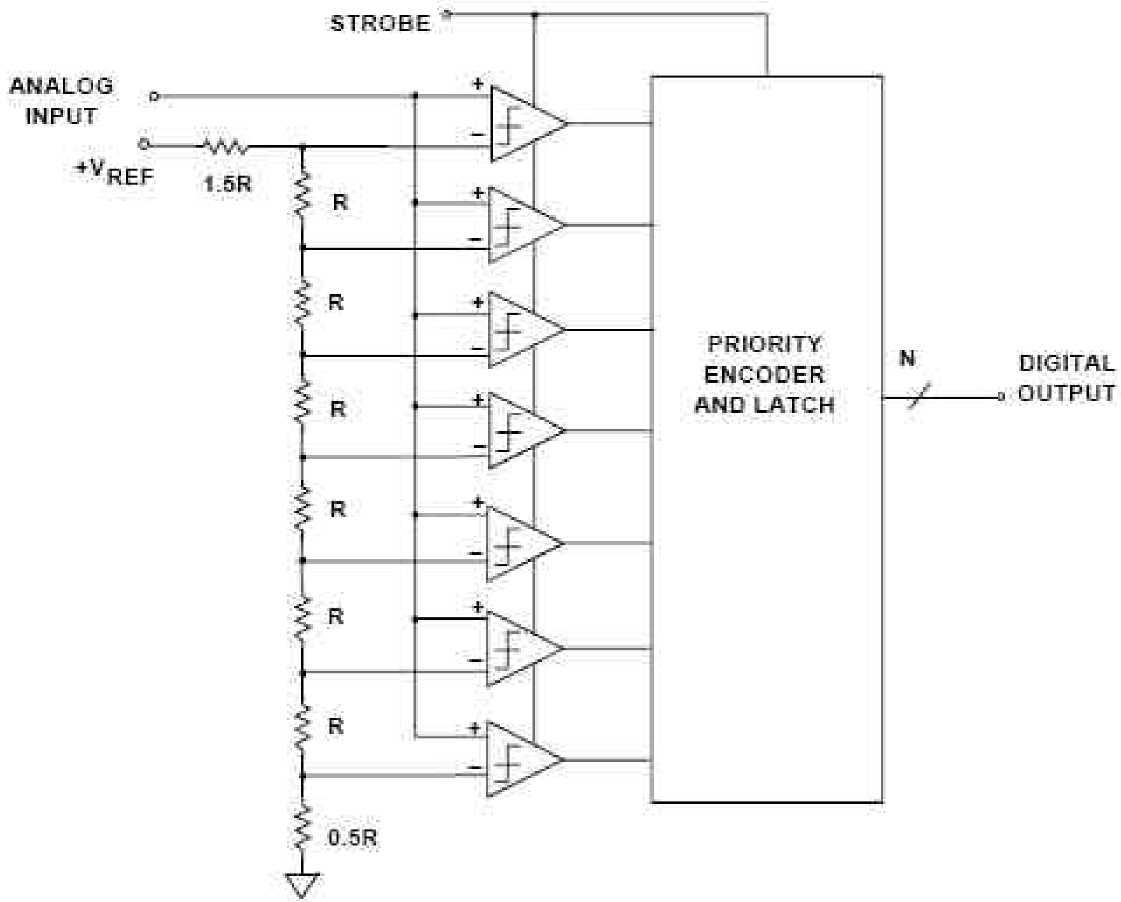


Figure 3.48: *3-bit All-Parallel (Flash) Converter*

Notes

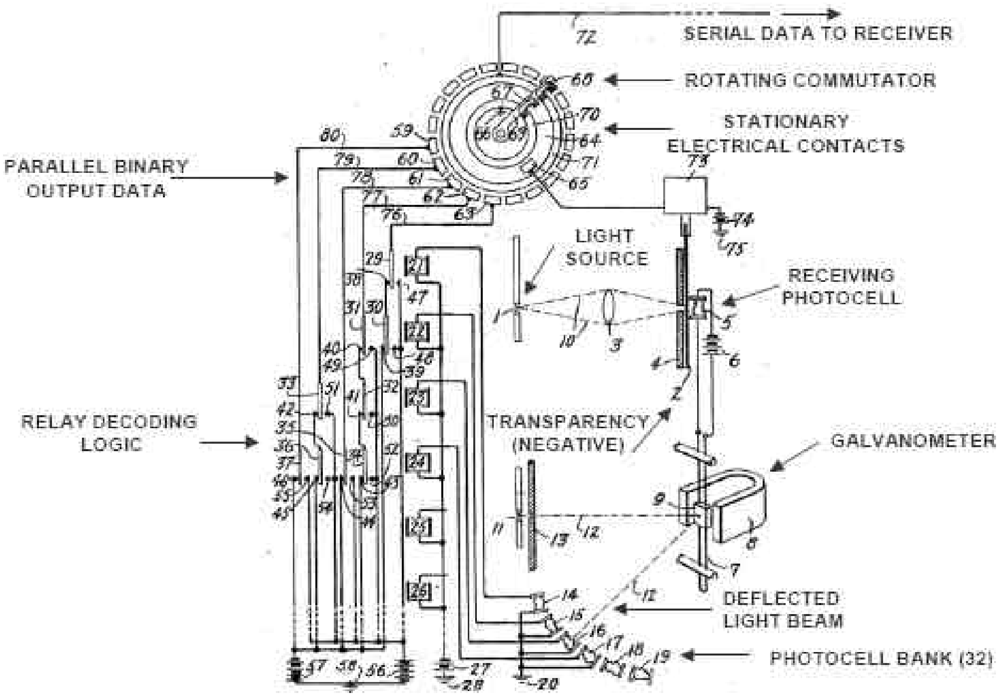


Figure 3.49: *A 5-Bit Flash ADC Proposed by Paul Rainey Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926*

Notes

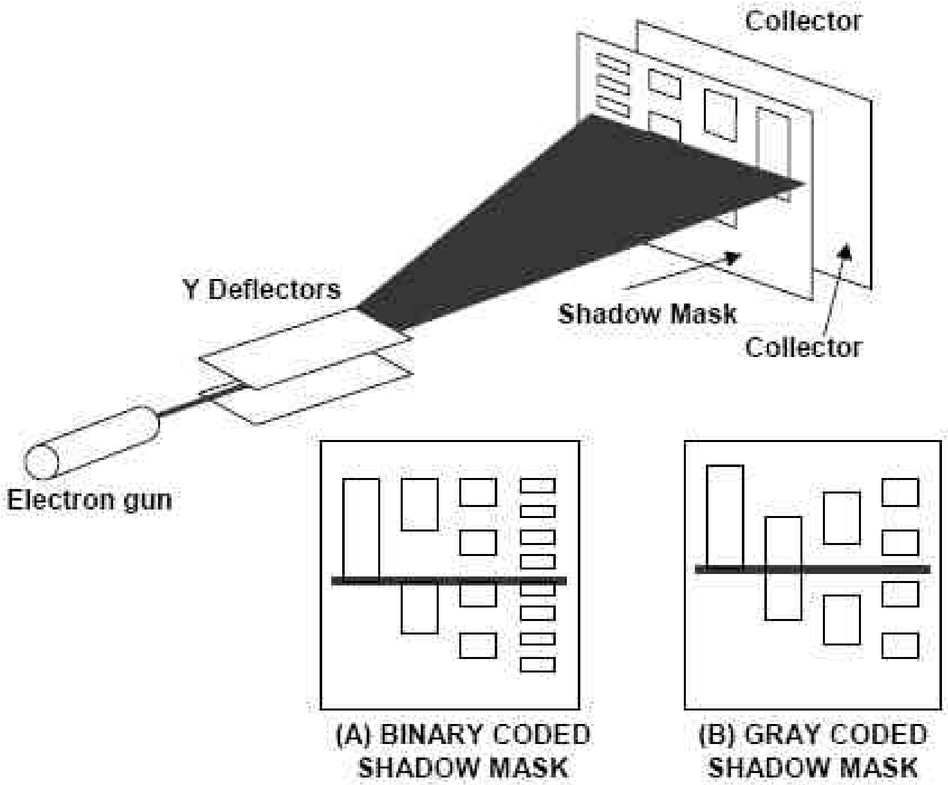


Figure 3.50: *The Electron Beam Coder from Bell Labs (1948)*

Notes

19" × 17" × 7"

VHS-630
- 6-Bits, 30 MSPS
- 32 dual MC1650 MECL III Comparators
- 100 watts (linear power supplies included)

VHS-675
- 6-Bits, 75 MSPS
- 64 AM685 Comparators
- 130 watts (linear power supplies included)

Figure 3.51: *VHS-Series ADCs from Computer Labs, Inc. VHS-630 (1970), VHS-675 (1975)*

Notes

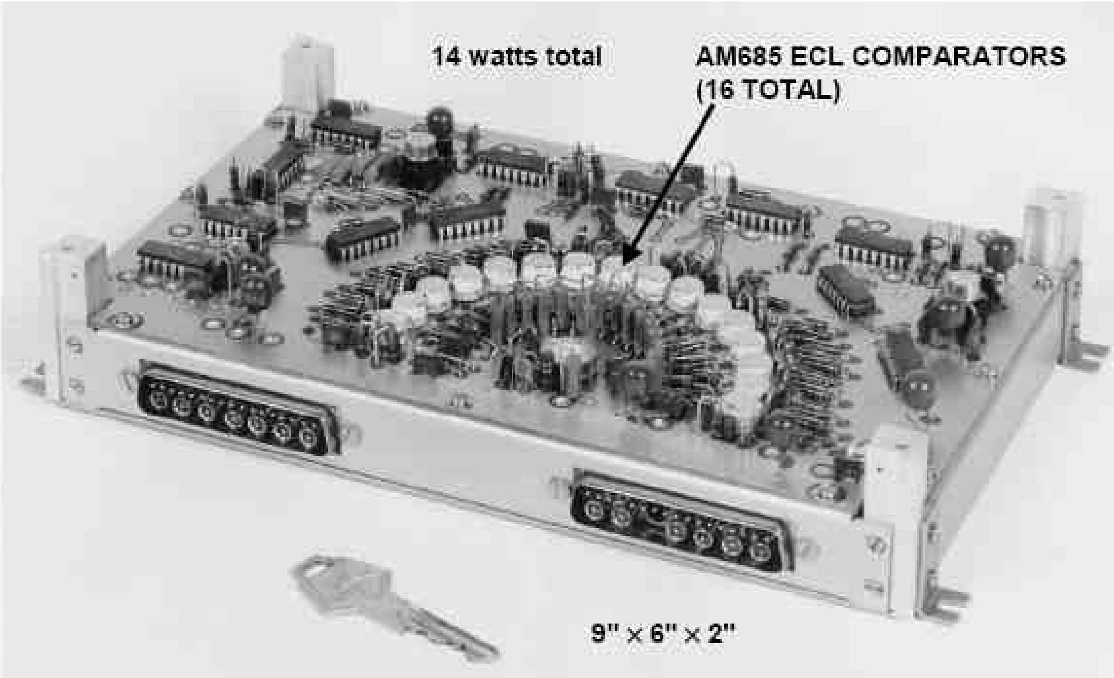


Figure 3.52: *MOD-4100 4-Bit, 100-MSPS Flash Converter, Computer Labs, 1975*

Notes

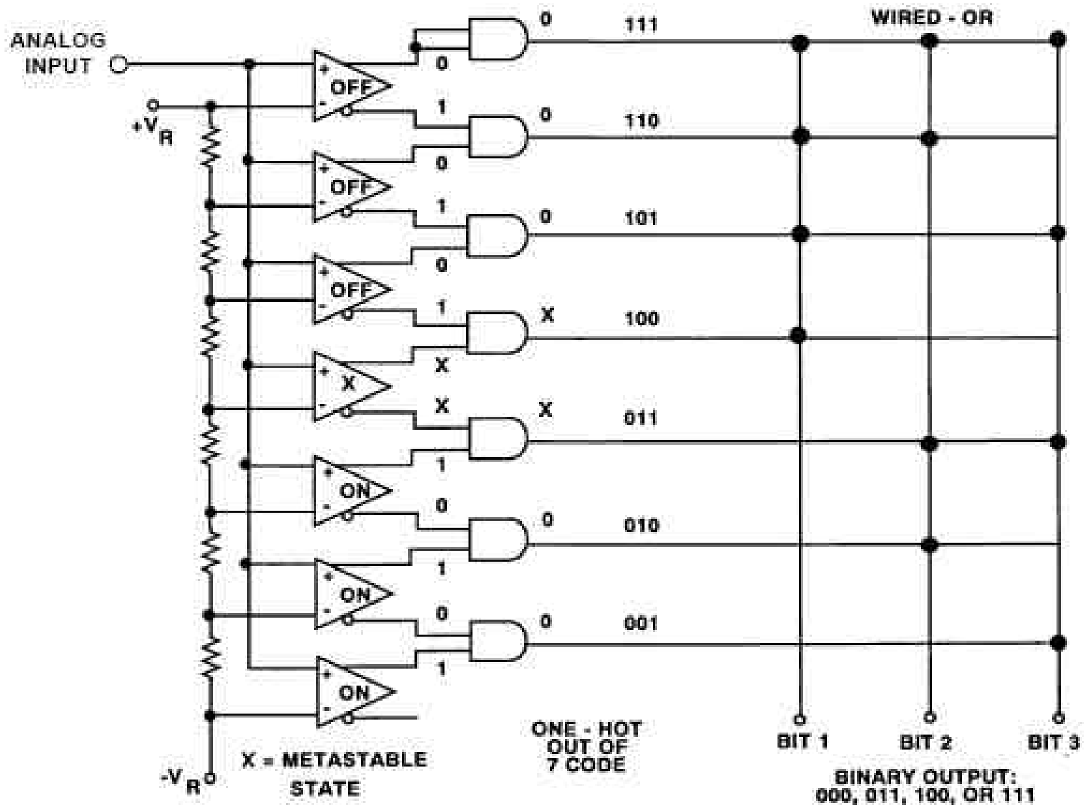


Figure 3.53: *Metastable Comparator Output States May Cause Error Codes in Data Converters*

Notes

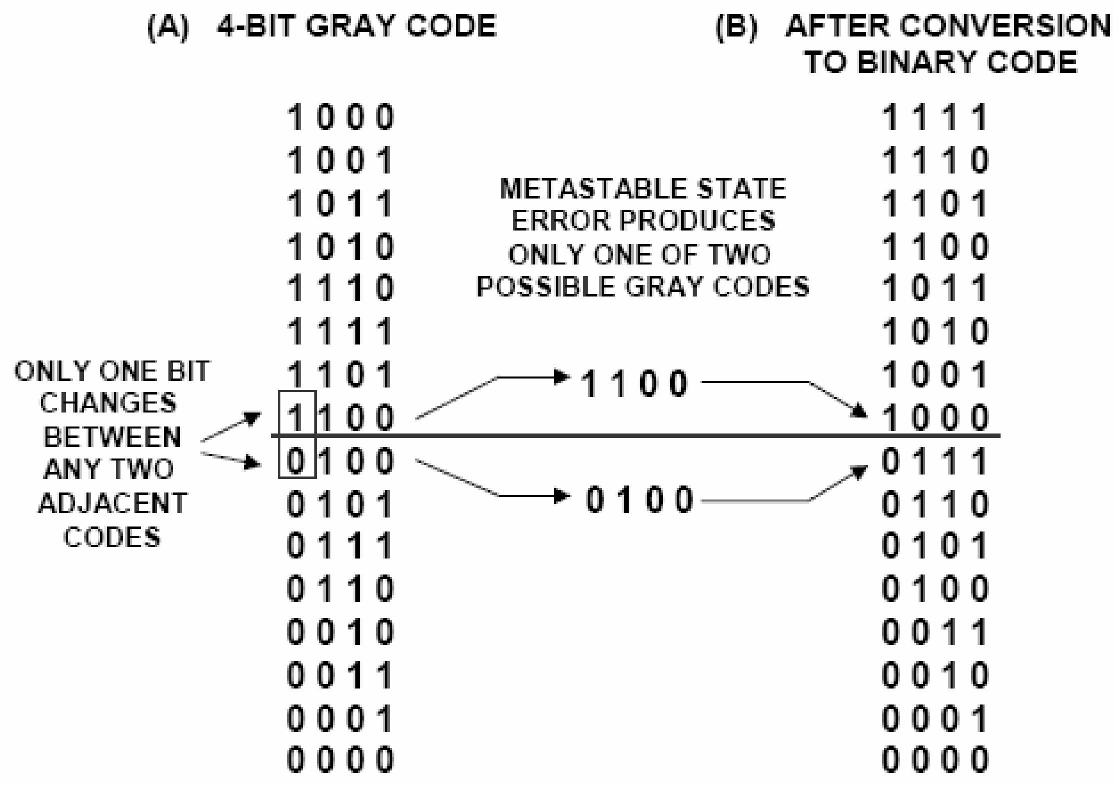


Figure 3.54: *Gray Code Decoding Reduces Amplitude of Metastable State Errors*

Notes

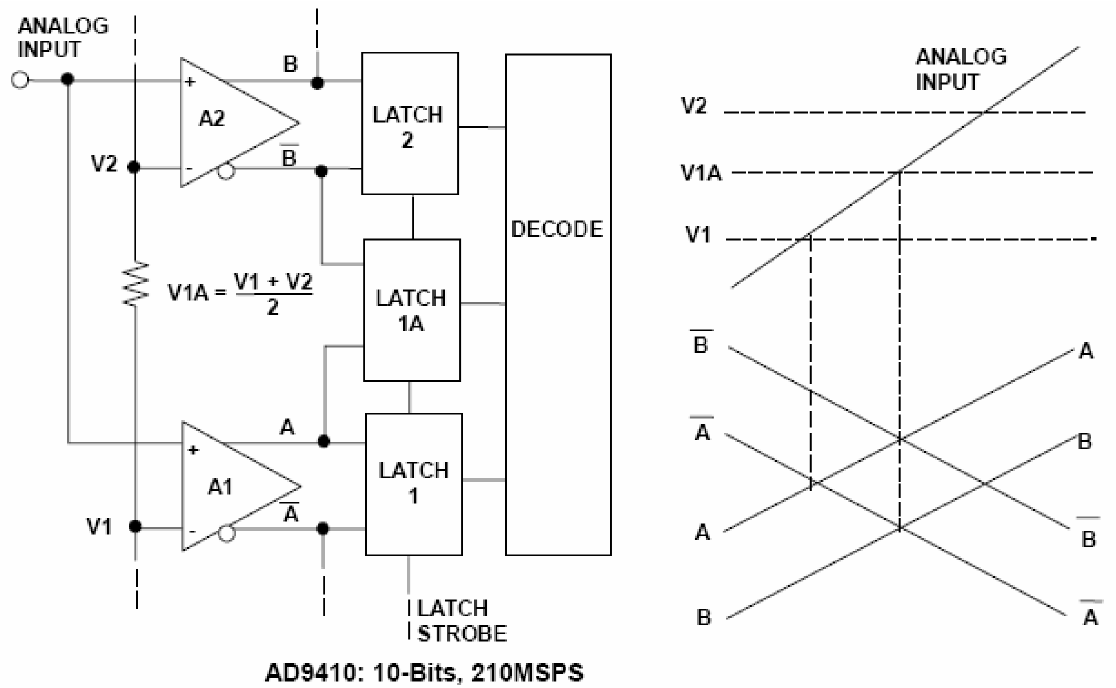


Figure 3.55: *"Interpolating" Flash Reduces the Number of Preamplifiers by Factor of Two*

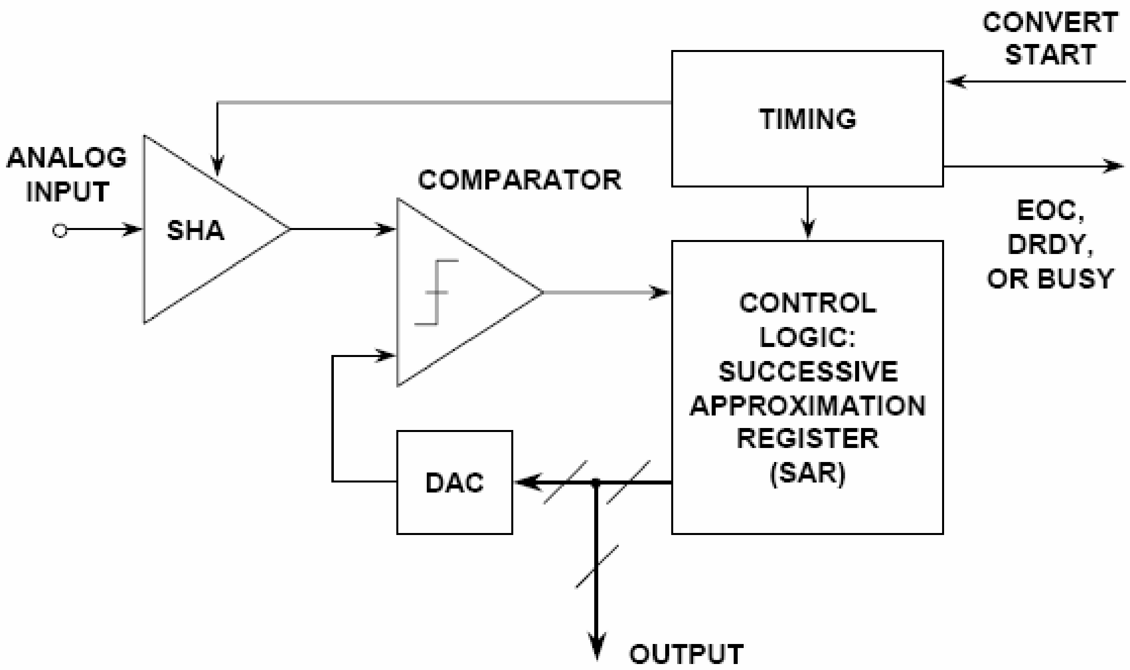


Figure 3.56: *Basic Successive Approximation ADC (Feedback Subtraction ADC)*

Notes

Notes

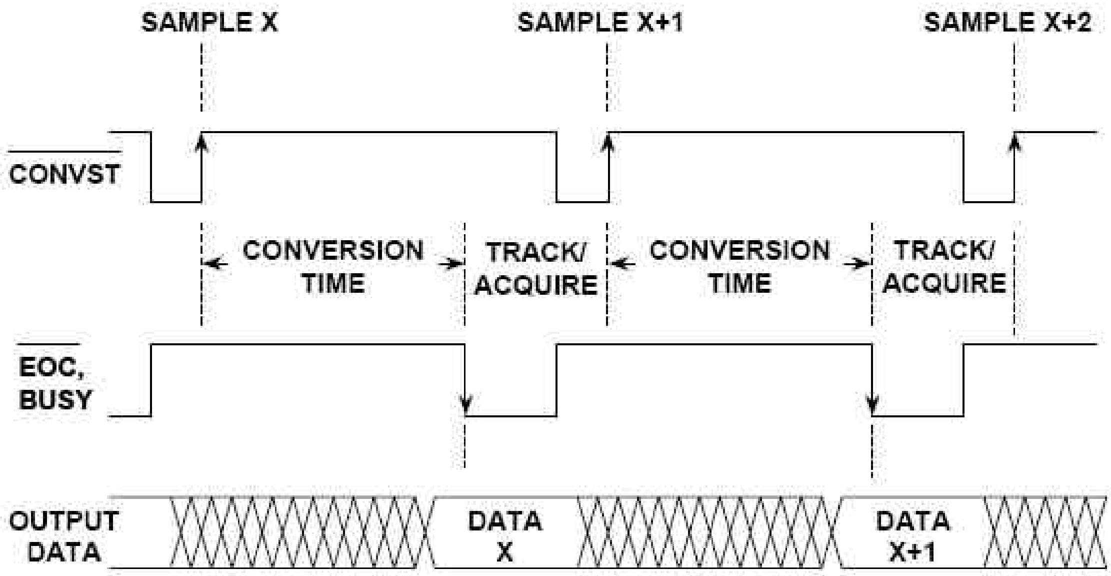


Figure 3.57: *Typical SAR ADC Timing*

Notes

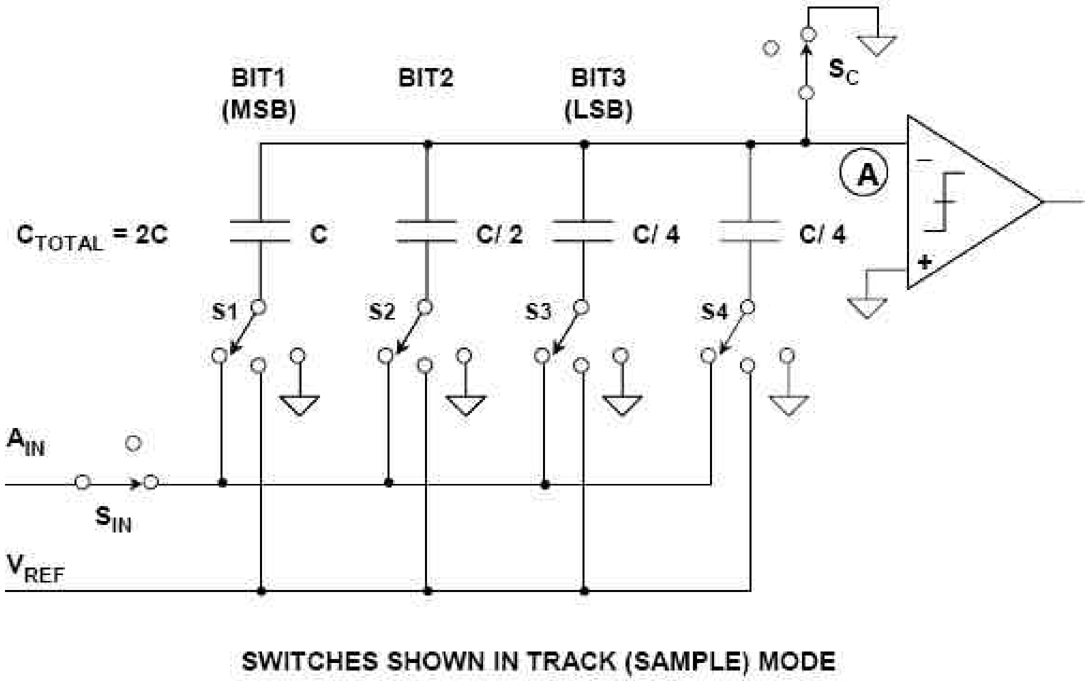


Figure 3.58: *3-Bit Switched Capacitor DAC*

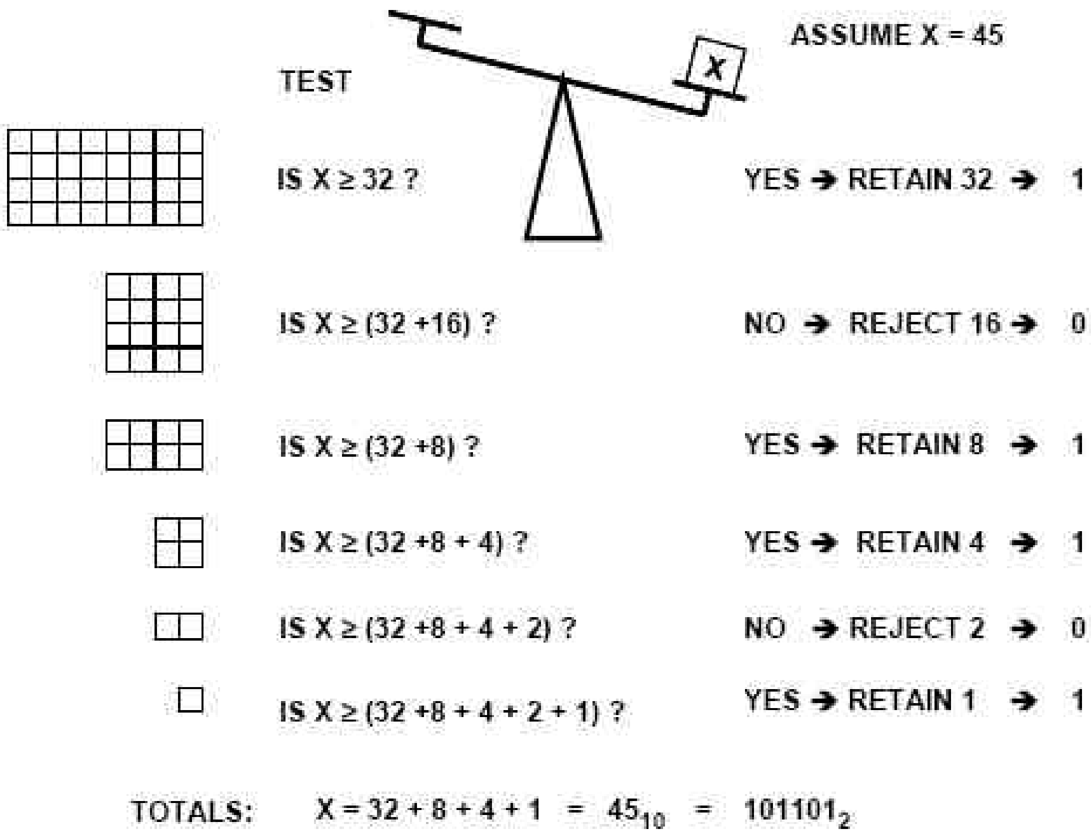
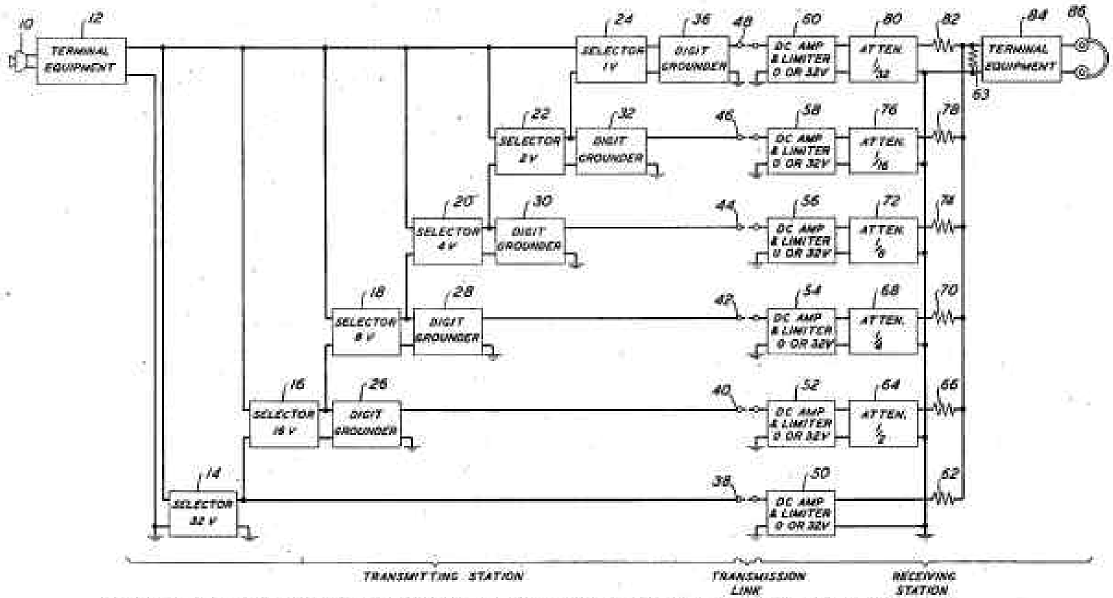


Figure 3.59: *Successive Approximation ADC Algorithm*

Notes

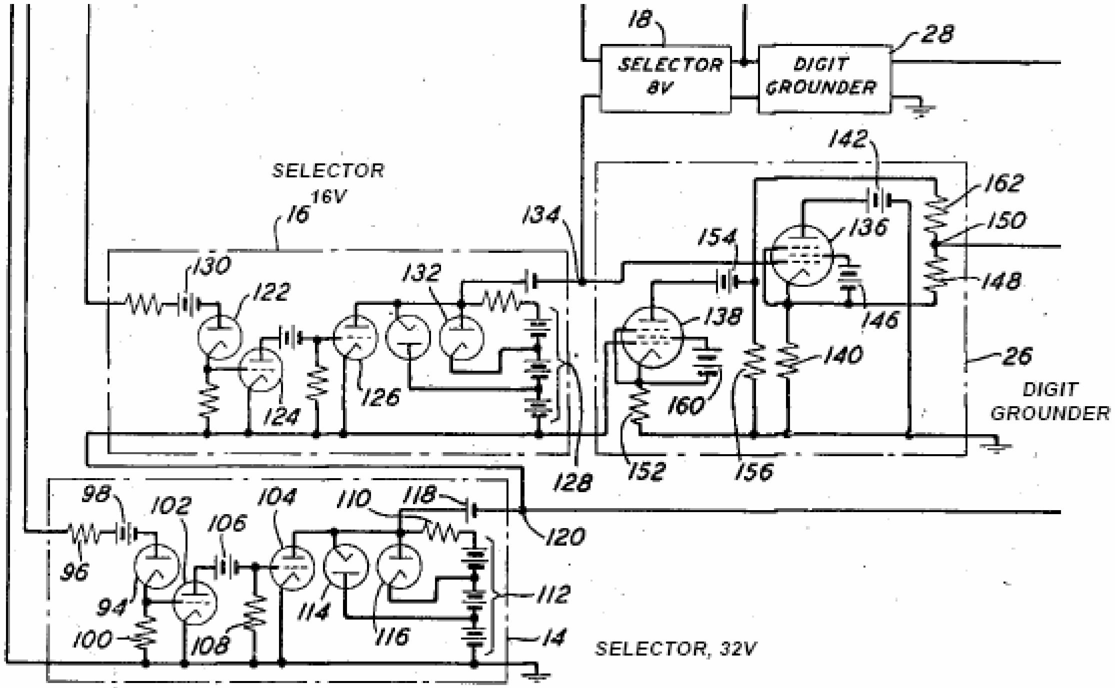


Extracted from: John C. Schelleng, "Code Modulation Communication System," *U.S. Patent 2,453,461*, Filed June 19, 1946, Issued November 9, 1948

Figure 3.60: *J. C. Schelleng's 1946 Successive Approximation ADC*

Notes

Notes



Extracted from: John C. Schelleng, "Code Modulation Communication System," *U.S. Patent 2,453,461*, Filed June 19, 1946, Issued November 9, 1948

Figure 3.61: *Details of the Selectors and Digit Grounders*

Notes

- 19" × 15" × 26"
- 150 lbs
- $8,500.00

Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

http://www.analogic.com

Figure 3.62: *1954 "DATRAC" 11-Bit, 50-kSPS SAR ADC Designed by Bernard M. Gordon at EPSCO*

	RESOLUTION	SAMPLING RATE	POWER	CHANNELS
AD7482	12-BITS	3.0MSPS	80mW	1
AD7484	14-BITS	3.0MSPS	80mW	1
AD7490	12-BITS	1.0MSPS	6mW	16
AD7928	12-BITS	1.0MSPS	5.4mW	8
AD974	16-BITS	0.2MSPS	120mW	4
AD7677*	16-BITS	1.0MSPS	130mW	1
AD7621*	16-BITS	3.0MSPS	100mW	1
AD7674*	18-BITS	0.8MSPS	120mW	1

* PulSAR® SERIES

Figure 3.63: *Resolution / Conversion Time Comparison for Representative Single-Supply SAR ADCs*

Notes

Notes

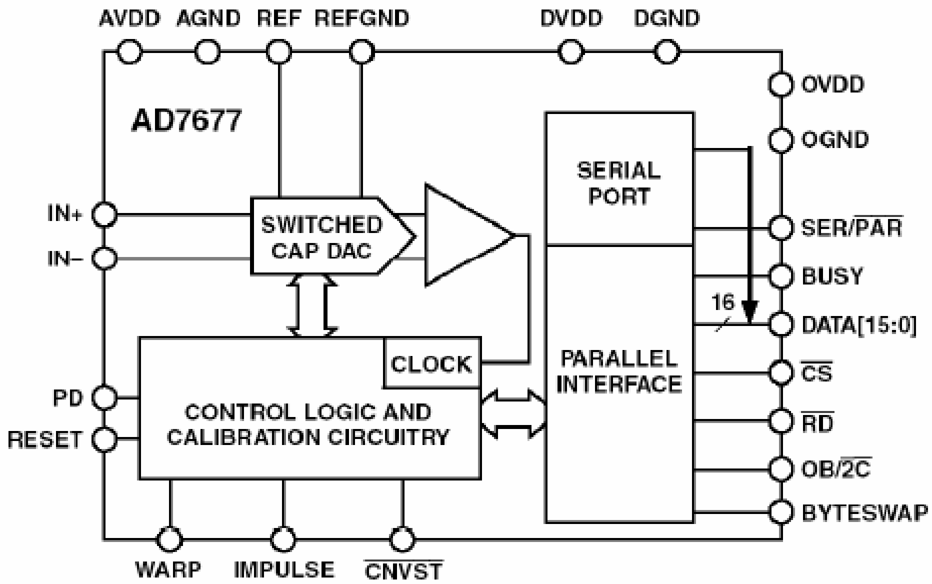
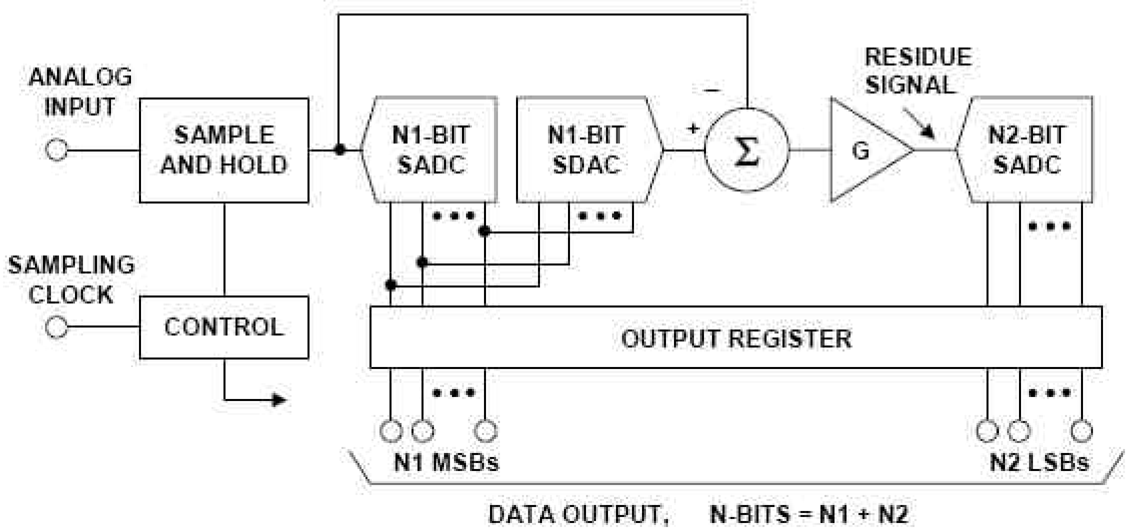


Figure 3.64: *AD7677 16-Bit 1-MSPS Switched Capacitor PulSAR® ADC*

Notes



See: R. Staffin and R. Lohman, "Signal Amplitude Quantizer," U.S. Patent 2,869,079, Filed December 19, 1956, Issued January 13, 1959

Figure 3.65: *N-bit Two-Stage Subranging ADC*

Notes

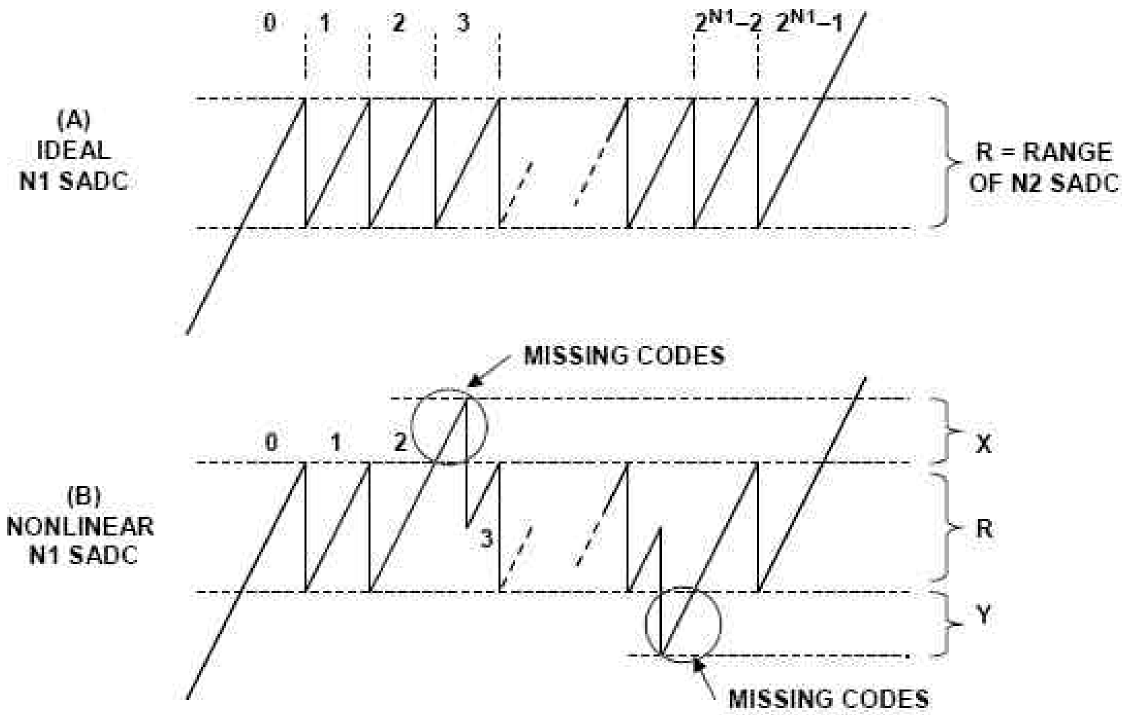


Figure 3.66: *Residue Waveforms at Input of N2 Sub-ADC*

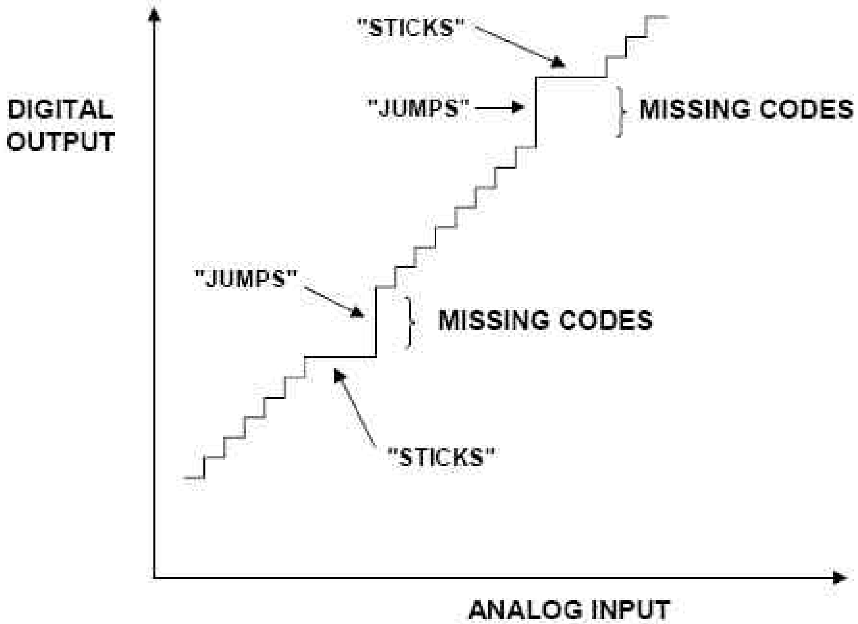


Figure 3.67: *Missing Codes Due to MSB SADC Nonlinearity or Interstage Misalignment*

Notes

Notes

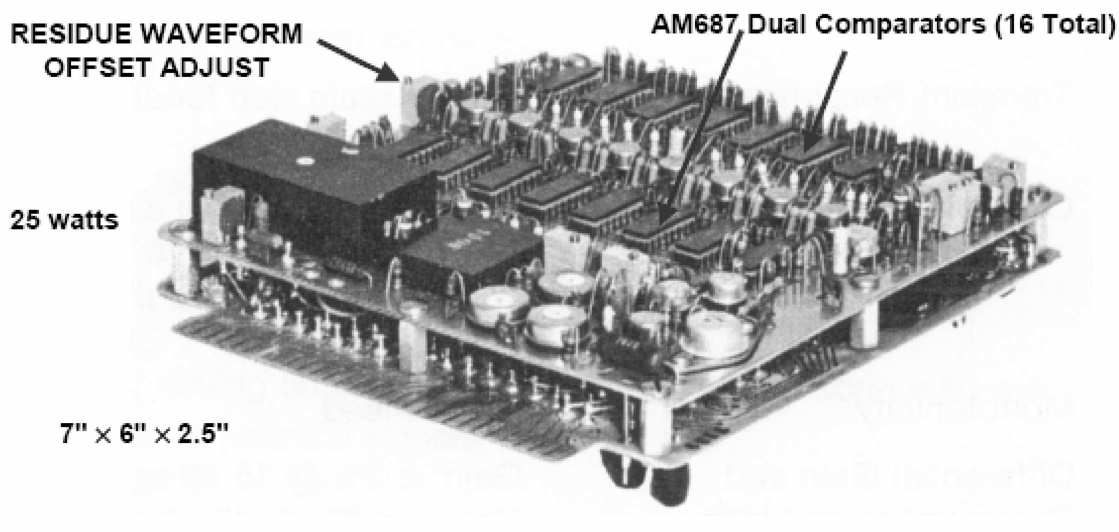


Figure 3.68: *MOD-815, 8-Bit, 15 MSPS 4×4 Subranging ADC, 1976, Computer Labs, Inc.*

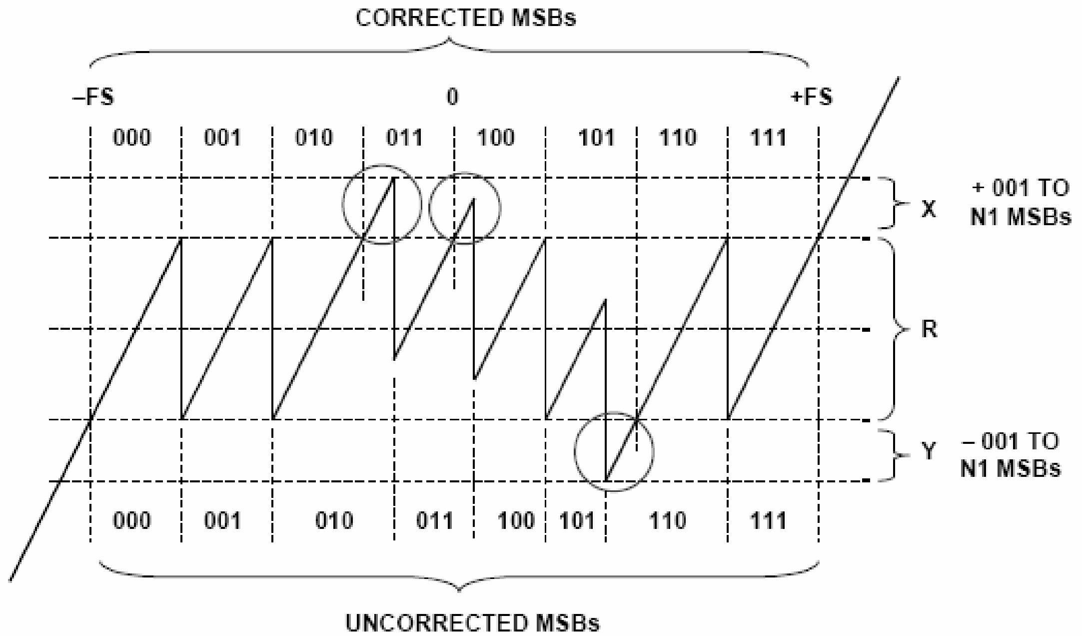
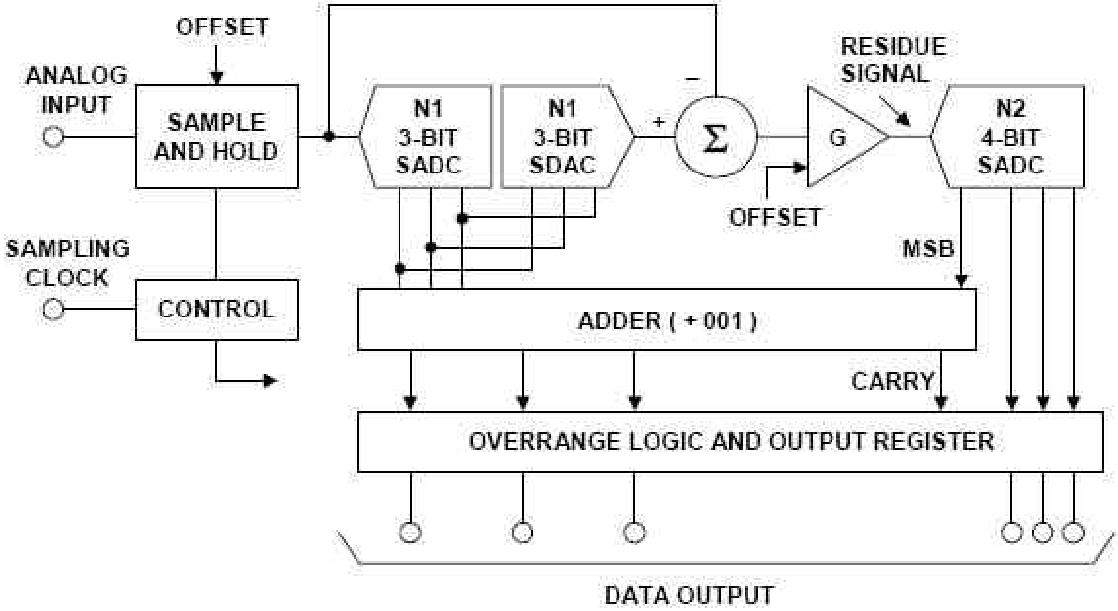


Figure 3.69: *Error Correction Using Added Quantization Levels for N1 = 3*

Notes

Notes



SEE: T. C. Verster, "A Method to Increase the Accuracy of Fast Serial-Parallel Analog-to-Digital Converters," *IEEE Transactions on Electronic Computers*, EC-13, 1964, pp. 471-473

Figure 3.70: *6-Bit Subranging Error Corrected ADC, N1 = 3, N2 = 4*

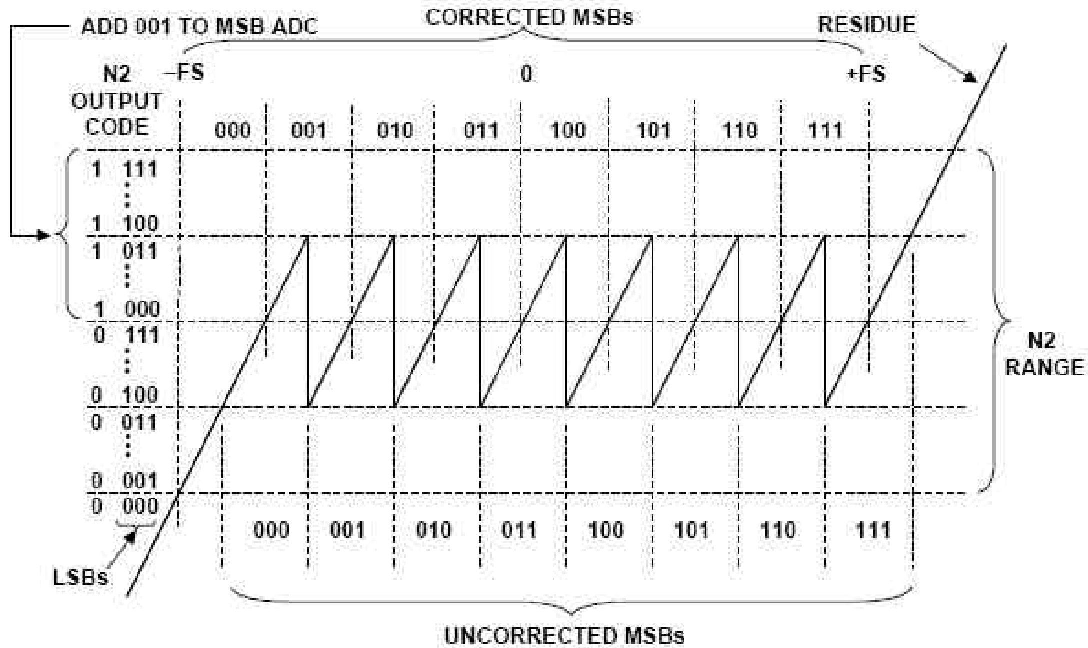


Figure 3.71: *6-Bit Error Corrected Subranging ADC N1 = 3, N2 = 4, Ideal MSB SADC*

Notes

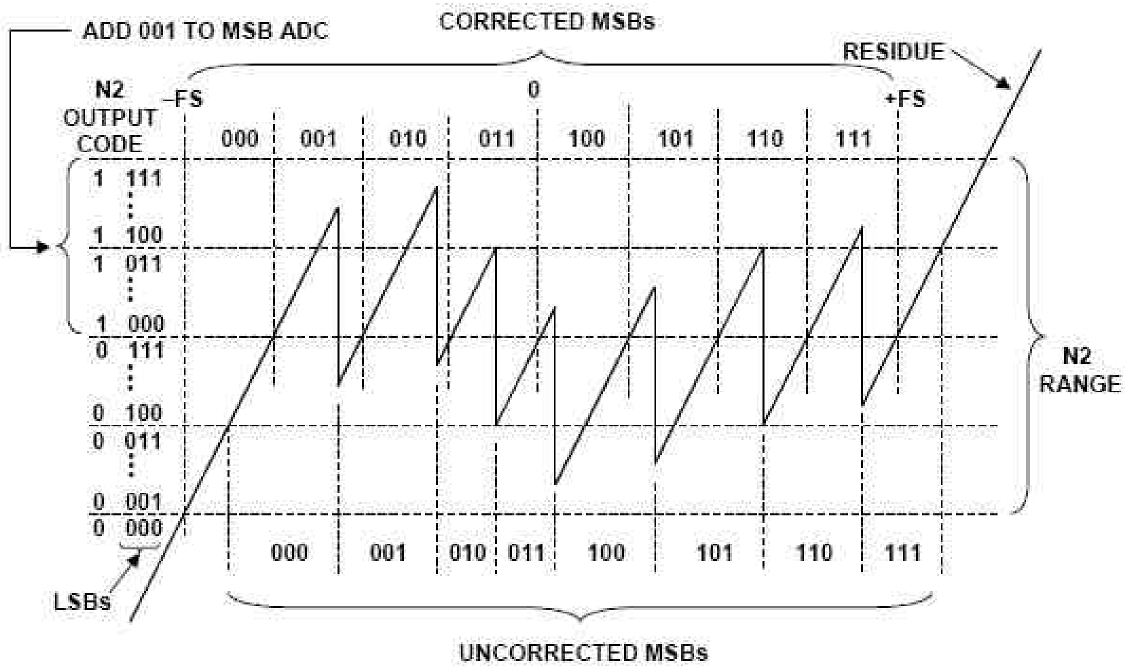


Figure 3.72: *6-Bit Error Corrected Subranging ADC 1 = 3, N2 = 4, Nonlinear MSB SADC*

Notes

Notes

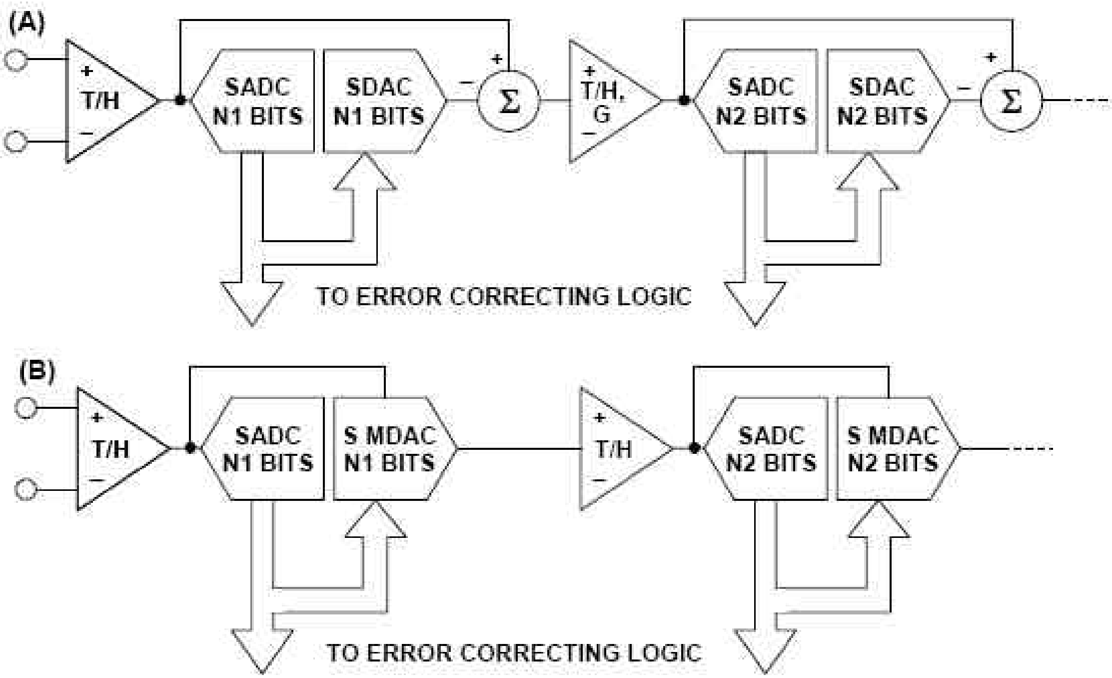


Figure 3.73: *Generalized Pipeline Stages in a Subranging ADC with Error Correction*

Notes

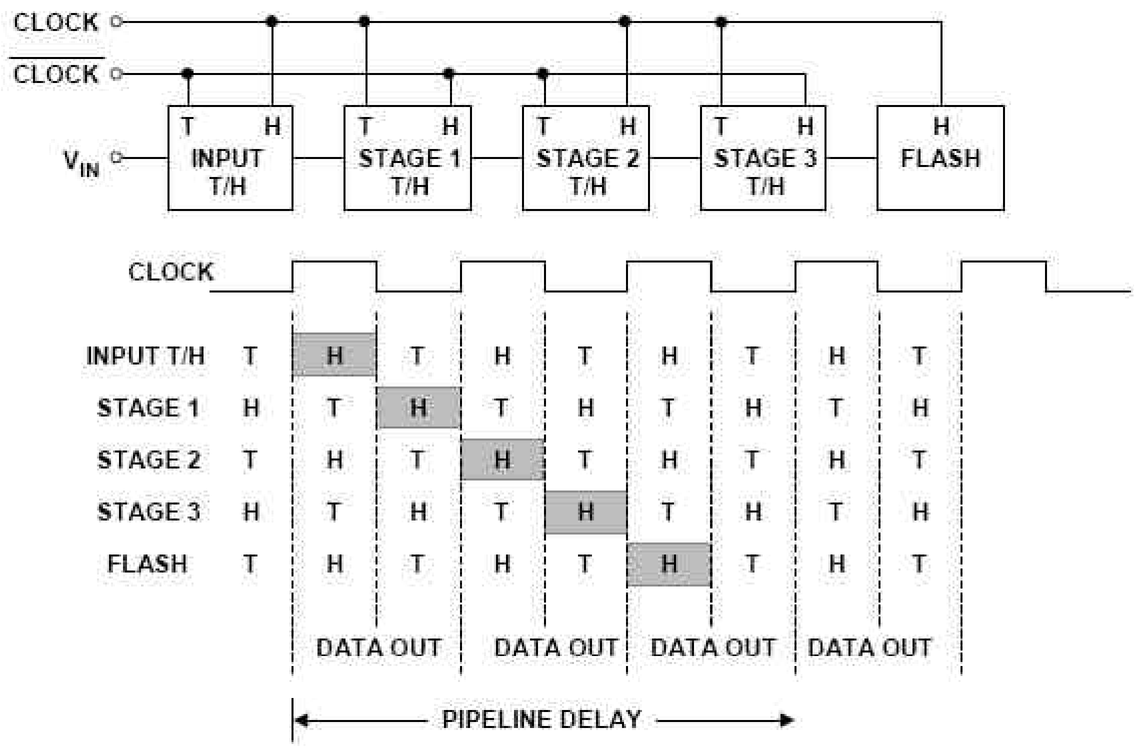


Figure 3.74: *Clock Issues in Pipelined ADCs*

Notes

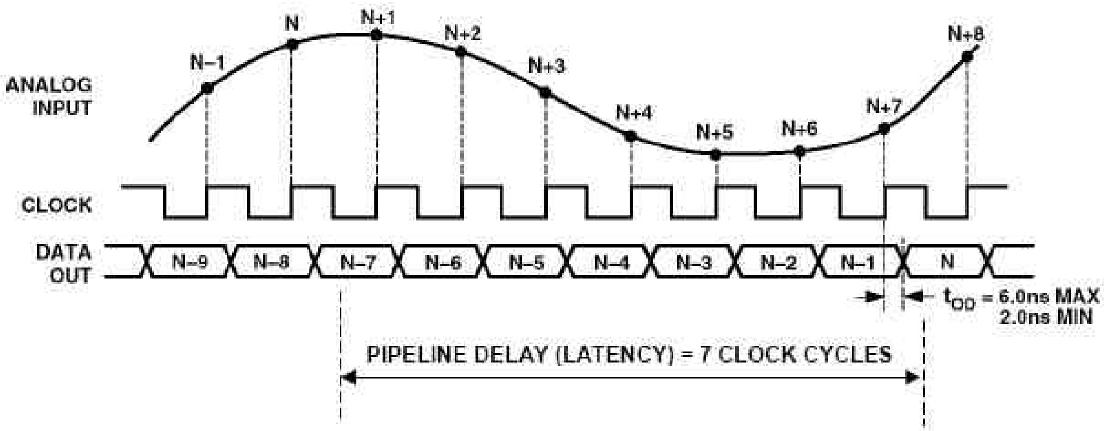


Figure 3.75: *Typical Pipelined ADC Timing for AD9235 12-Bit, 65-MSPS ADC*

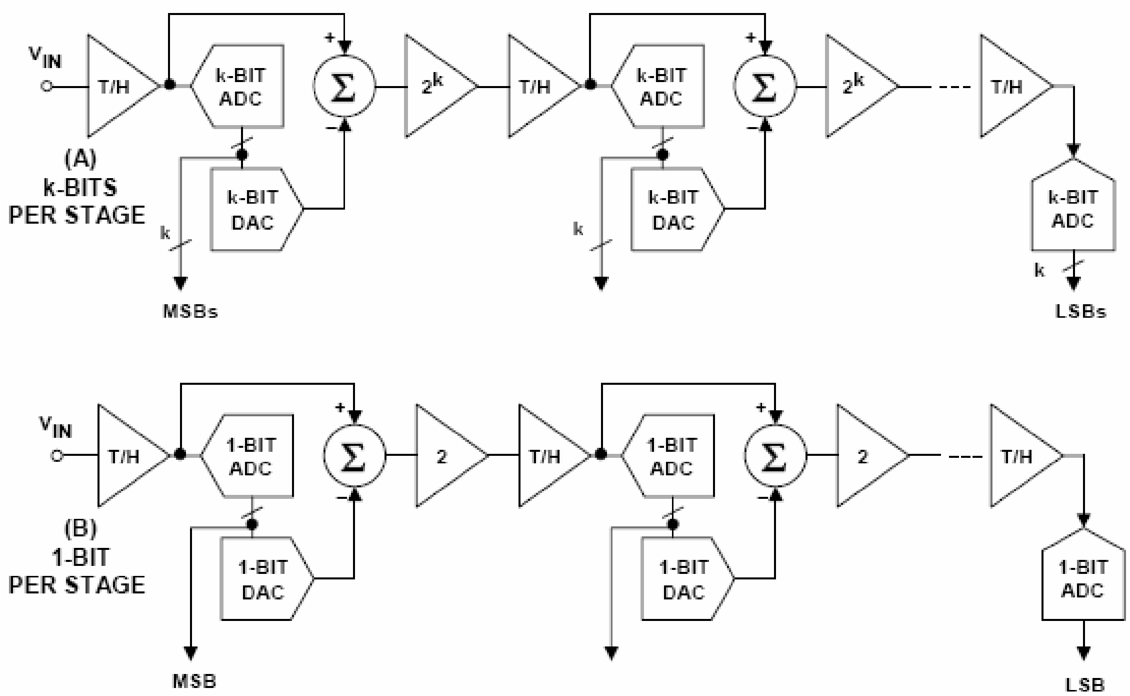


Figure 3.76: Basic Pipelined ADC with Identical Stages

Notes

Notes

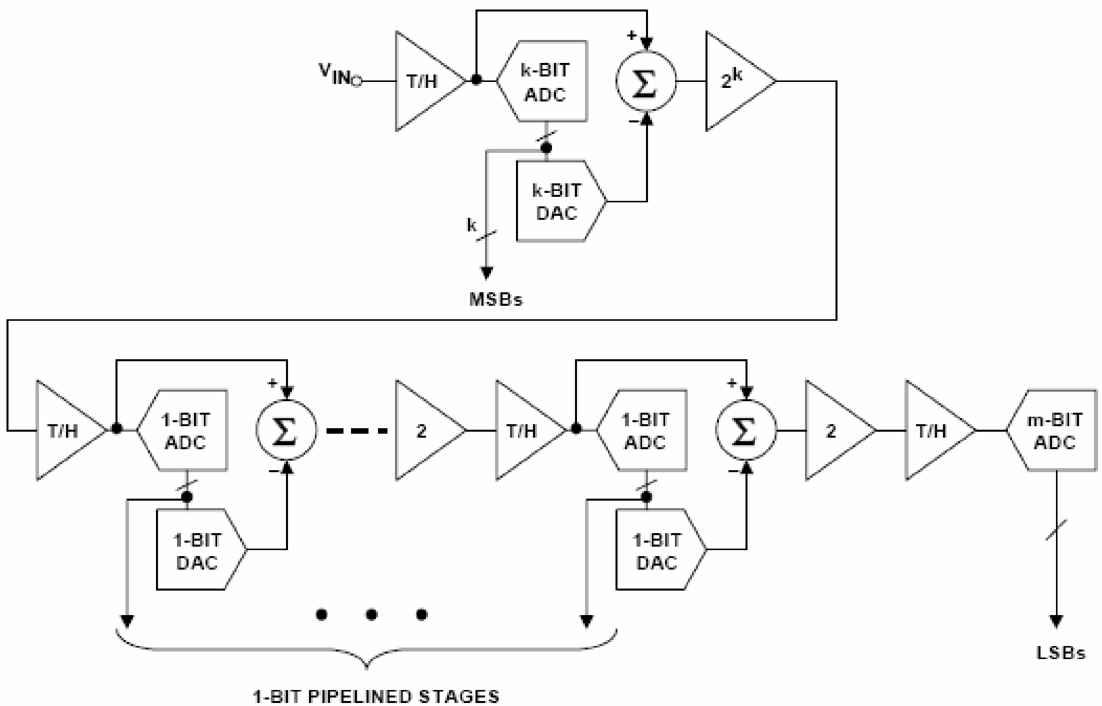


Figure 3.77: *Multibit and 1-Bit Pipelined Core Combined*

Notes

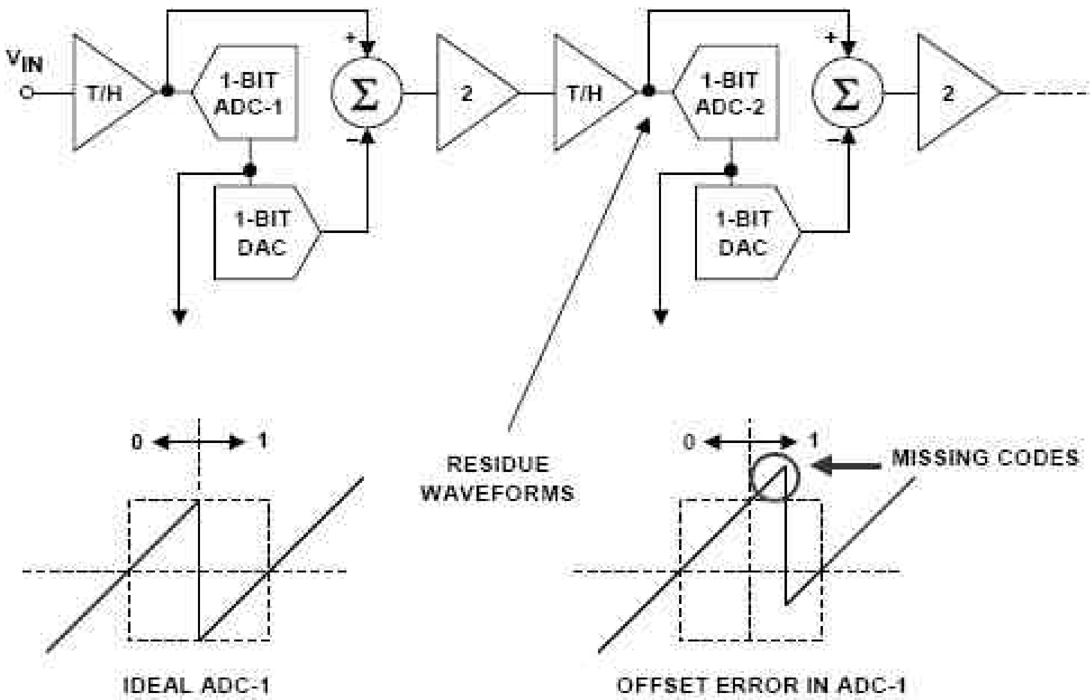


Figure 3.78: *1-Bit per Stage Pipelined ADC*

Notes

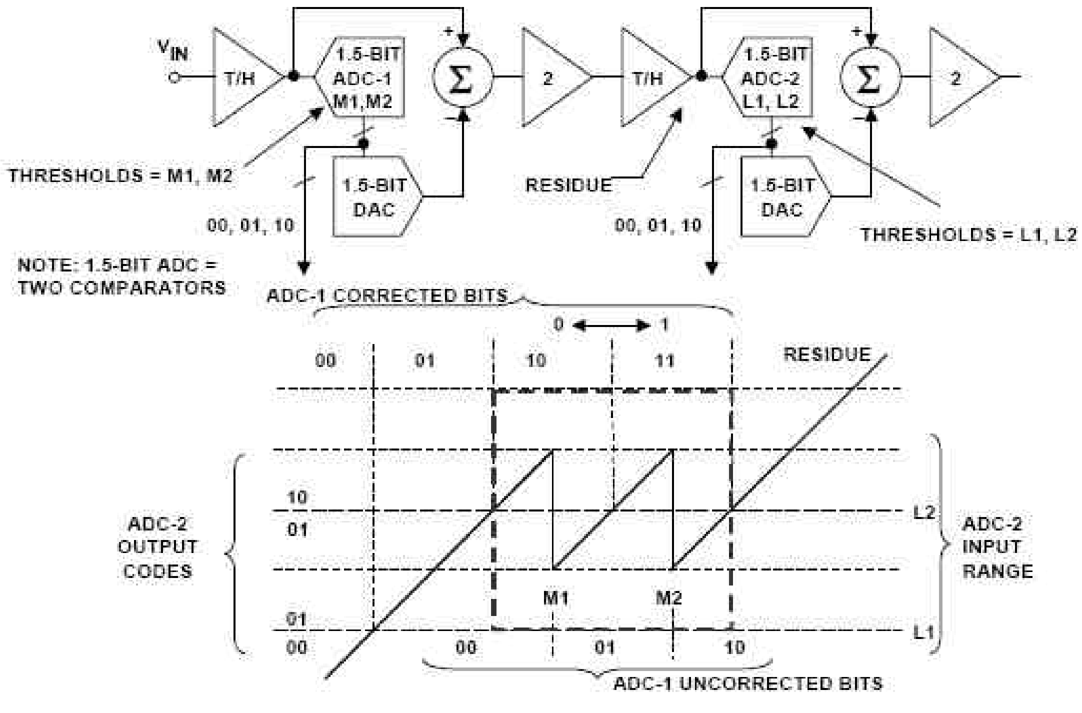


Figure 3.79: *1.5-Bit per Stage Pipeline Showing Error Corrected Range*

Notes

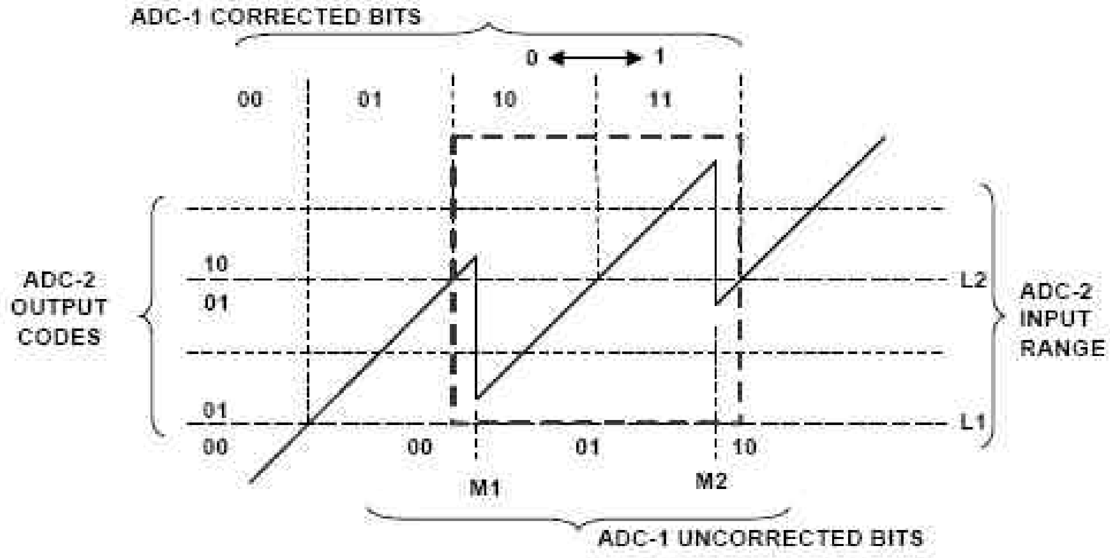


Figure 3.80: *Residue Waveform for 1.5-Bit ADC-2 Stage Input with Nonlinear ADC-1 Stage, Case 1*

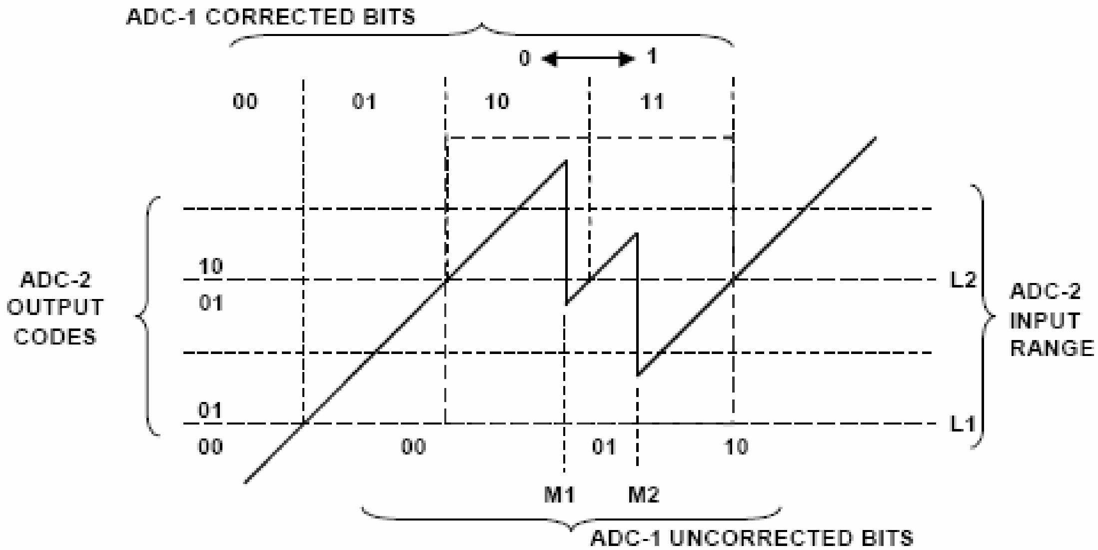
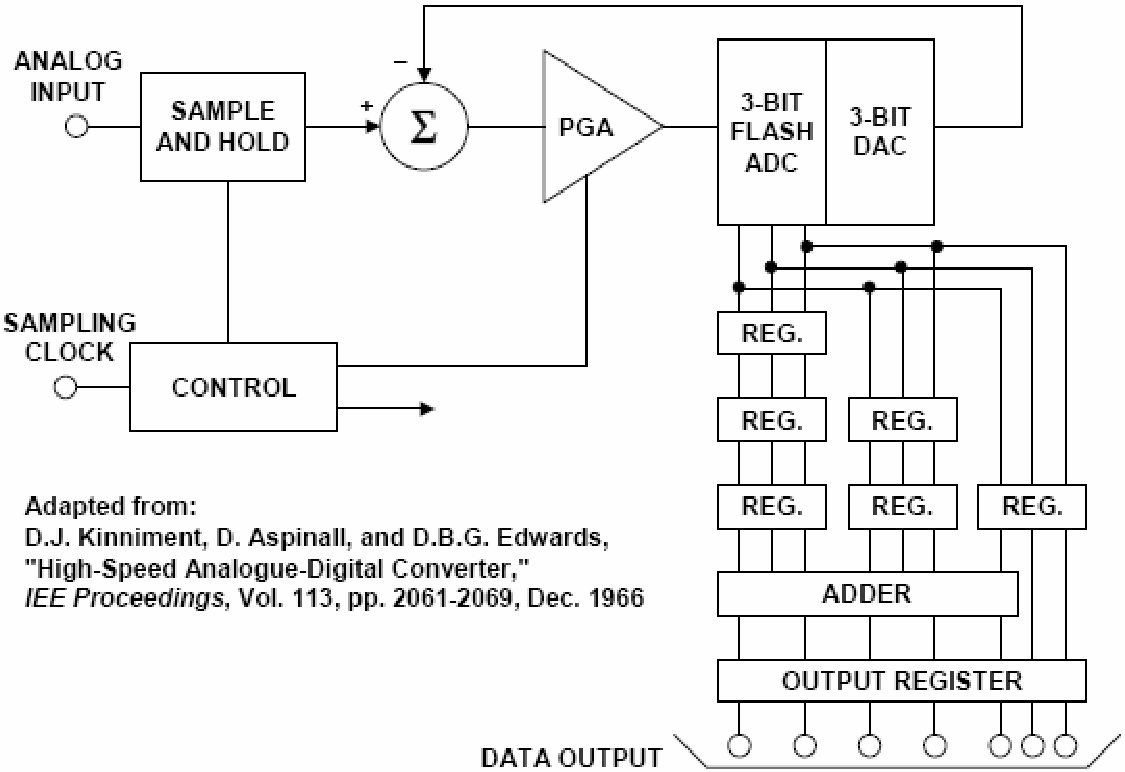


Figure 3.81: *Residue Waveform for 1.5-Bit ADC-2 Stage Input with Nonlinear ADC-1 Stage, Case 2*

Notes

Notes



Adapted from:
D.J. Kinniment, D. Aspinall, and D.B.G. Edwards, "High-Speed Analogue-Digital Converter," *IEE Proceedings*, Vol. 113, pp. 2061-2069, Dec. 1966

Figure 3.82: *Kinniment, et. al., 1966 Pipelined 7-bit, 9-MSPS Recirculating ADC Architecture*

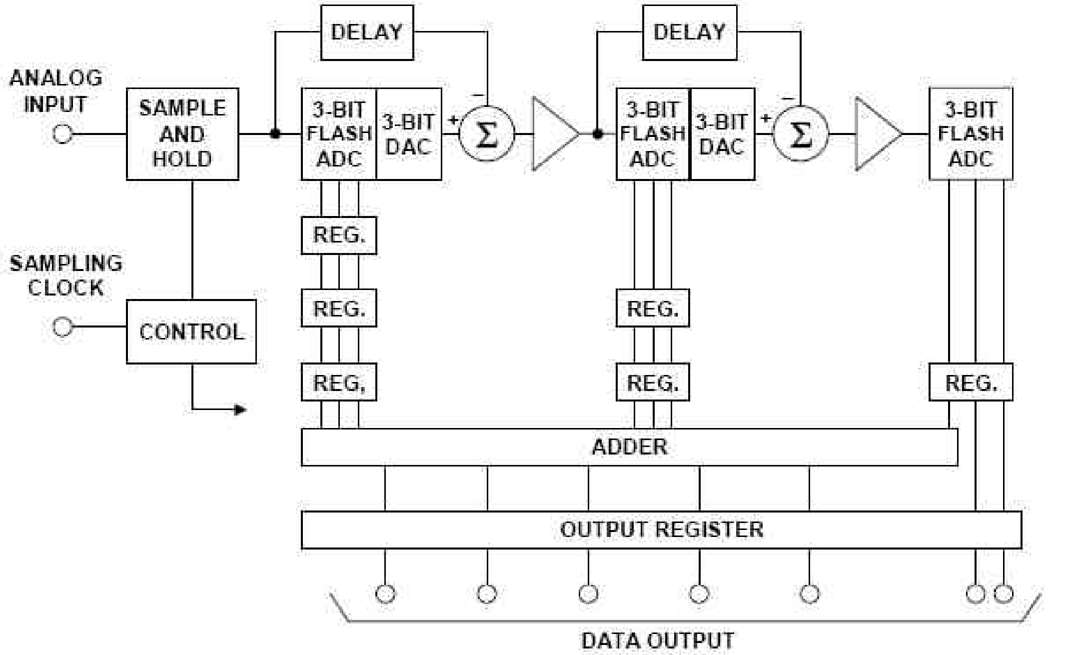


Figure 3.83: *Kinniment, et. al., 1966 Proposed Pipelined 7-bit ADC Architecture*

Notes

Notes

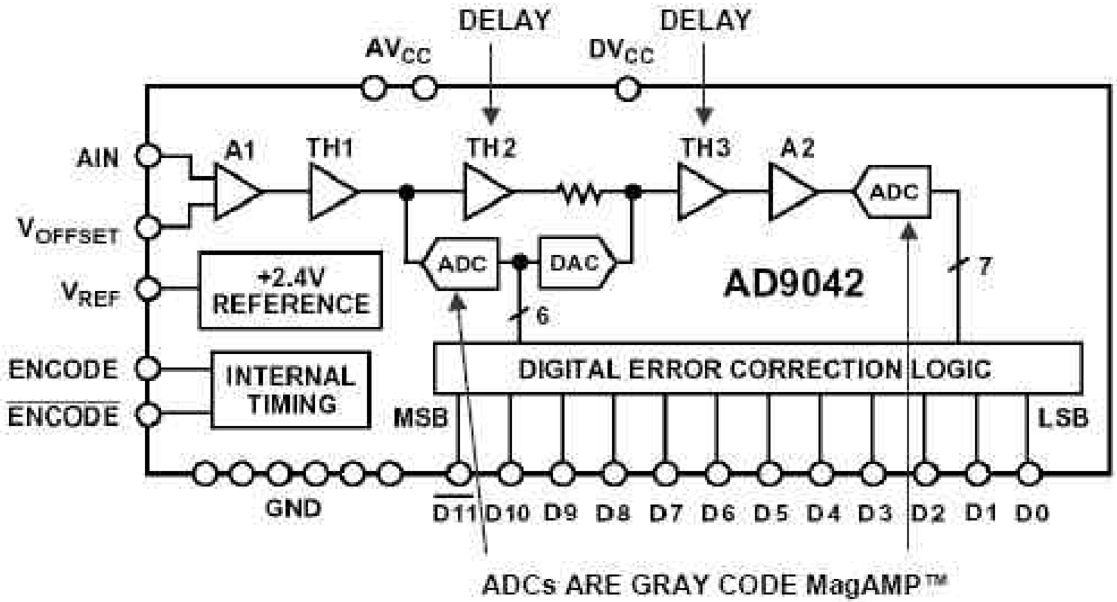


Figure 3.84: *AD9042 12-Bit 41-MSPS ADC, 1995*

Notes

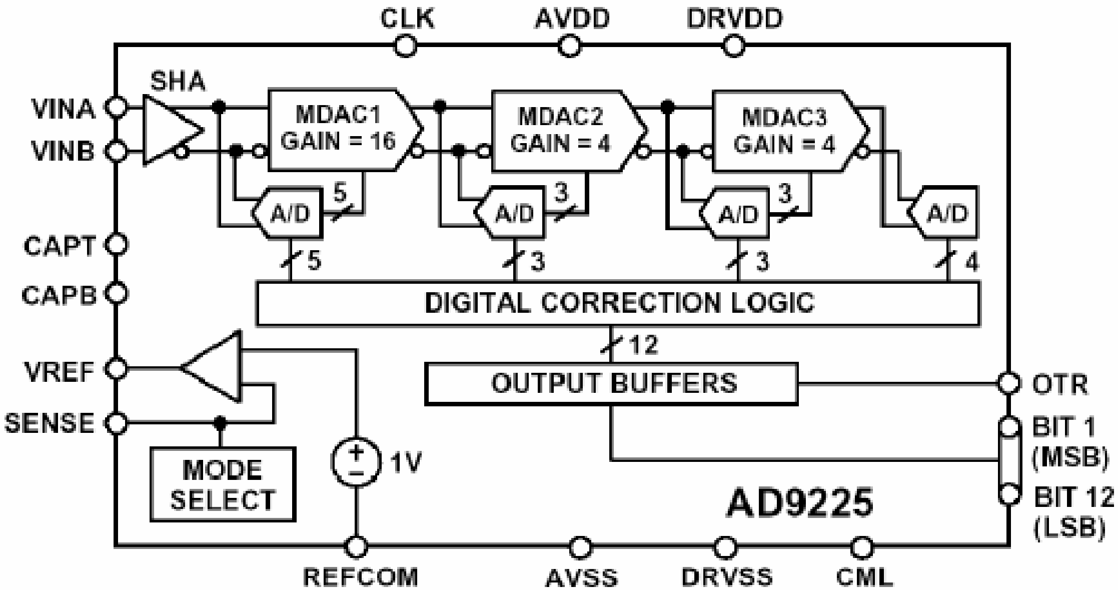


Figure 3.85: *AD9225 12-Bit 25-MSPS CMOS ADC, 1998*

Notes

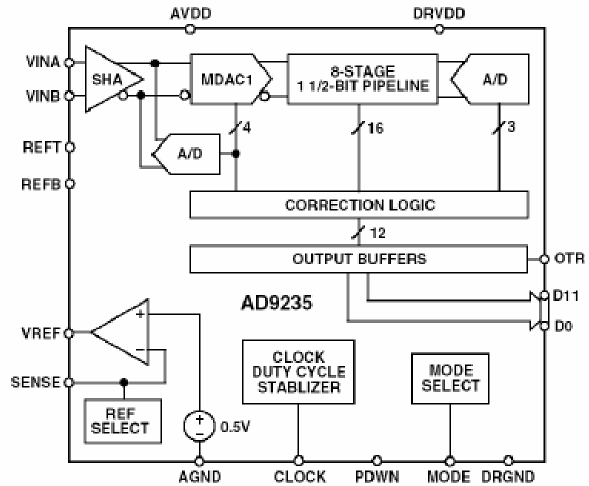


Figure 3.86: *AD9235 12-Bit, 65-MSPS CMOC ADC, 2001*

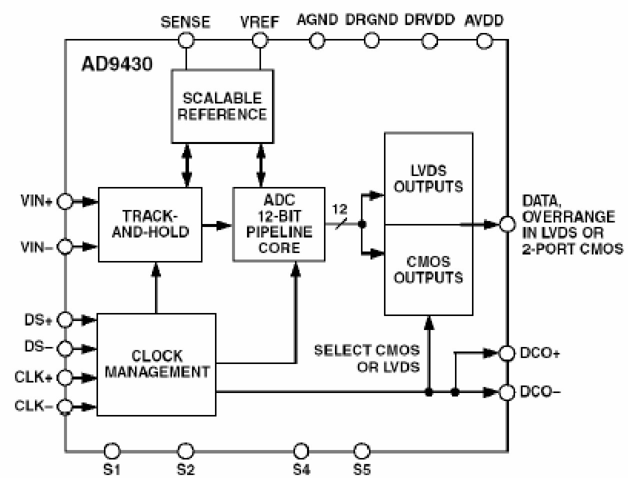


Figure 3.87: *AD9430 12-Bit, 170-/210-MSPS ADC, 2002*

Notes

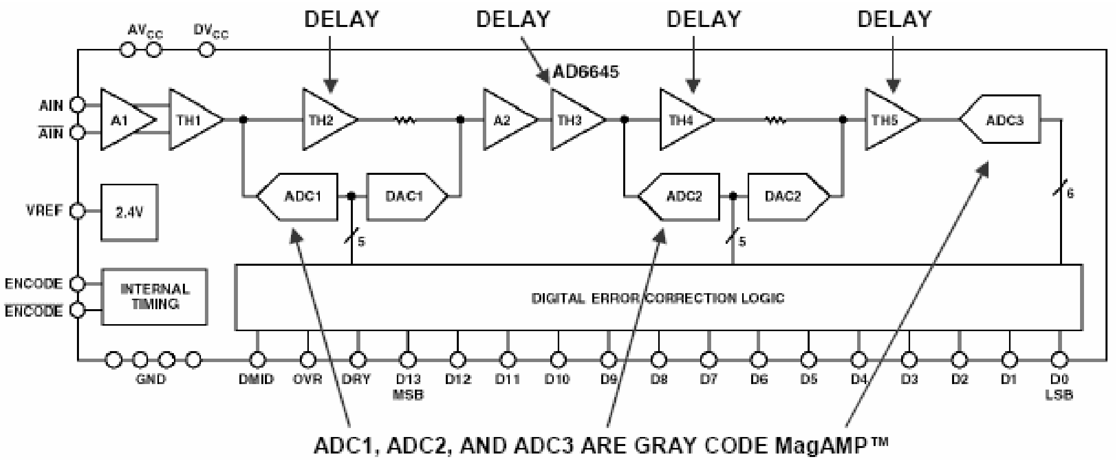
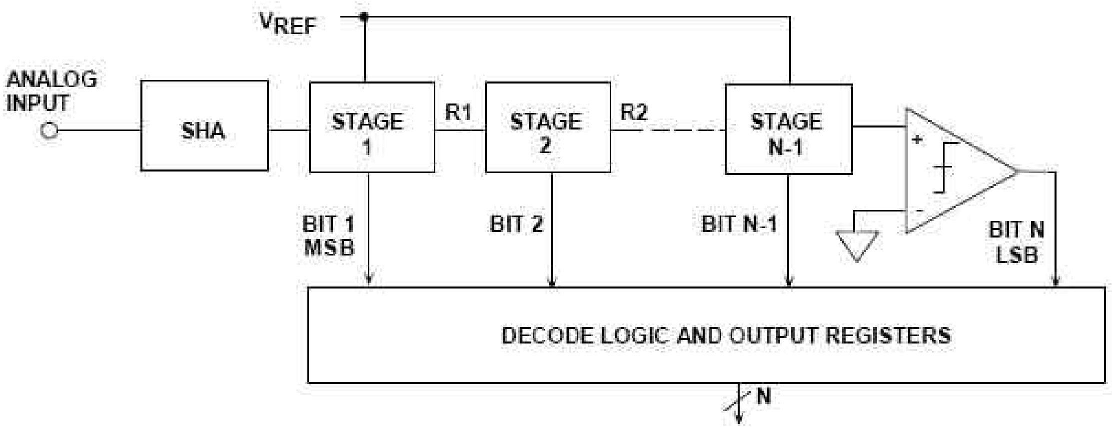


***Figure 3.88:** AD6645 14-Bit, 105-MSPS ADC, 2003 (80-MSPS Version Released in 2002)*

Notes



B. D. Smith, "An Unusual Electronic Analog-Digital Conversion Method," *IRE Transactions on Instrumentation*, June 1956, pp. 155-160.

Figure 3.89: *Generalized Bit-Per-Stage ADC Architecture*

Notes

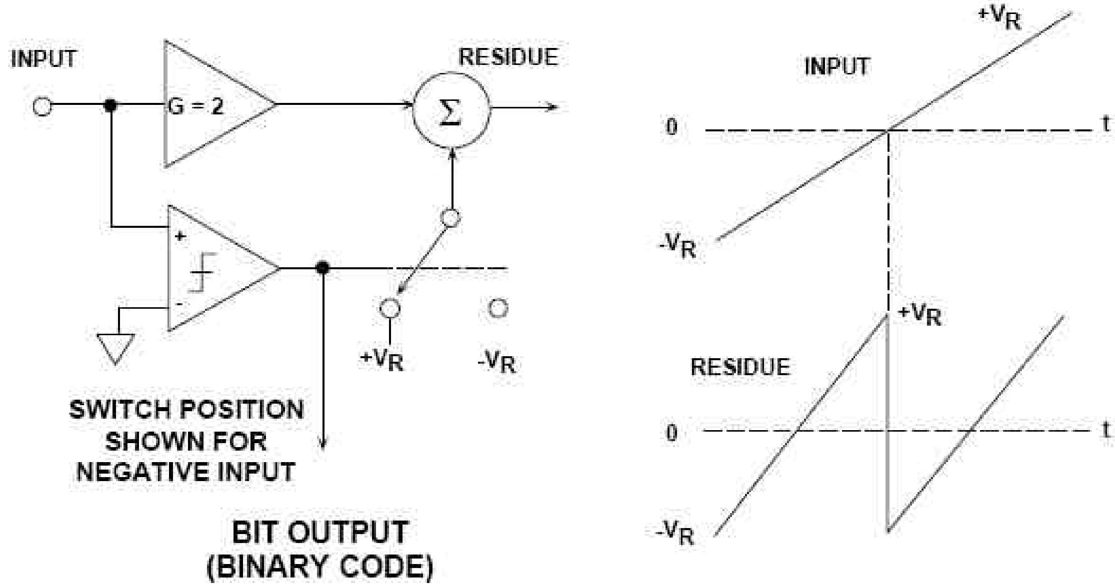


Figure 3.90: *Single-Stage Transfer Function for Binary ADC*

Notes

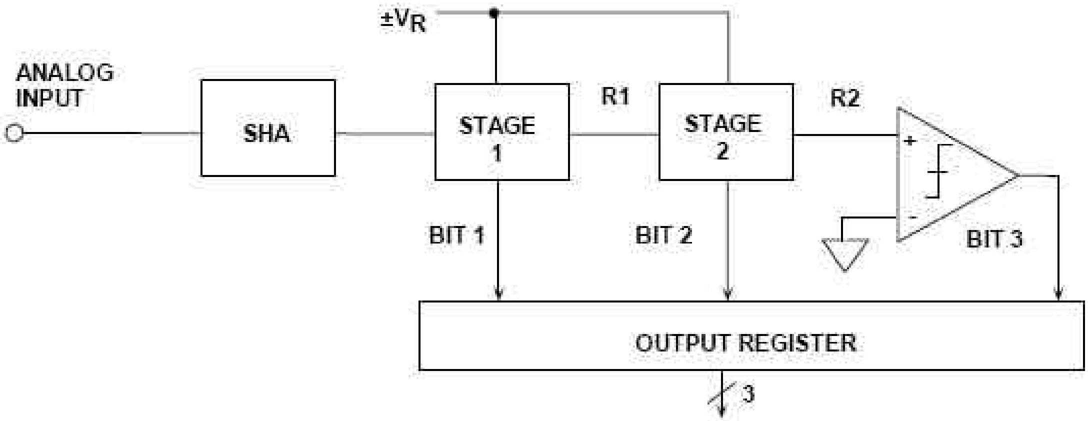


Figure 3.91: *3-bit Serial ADC with Binary Output*

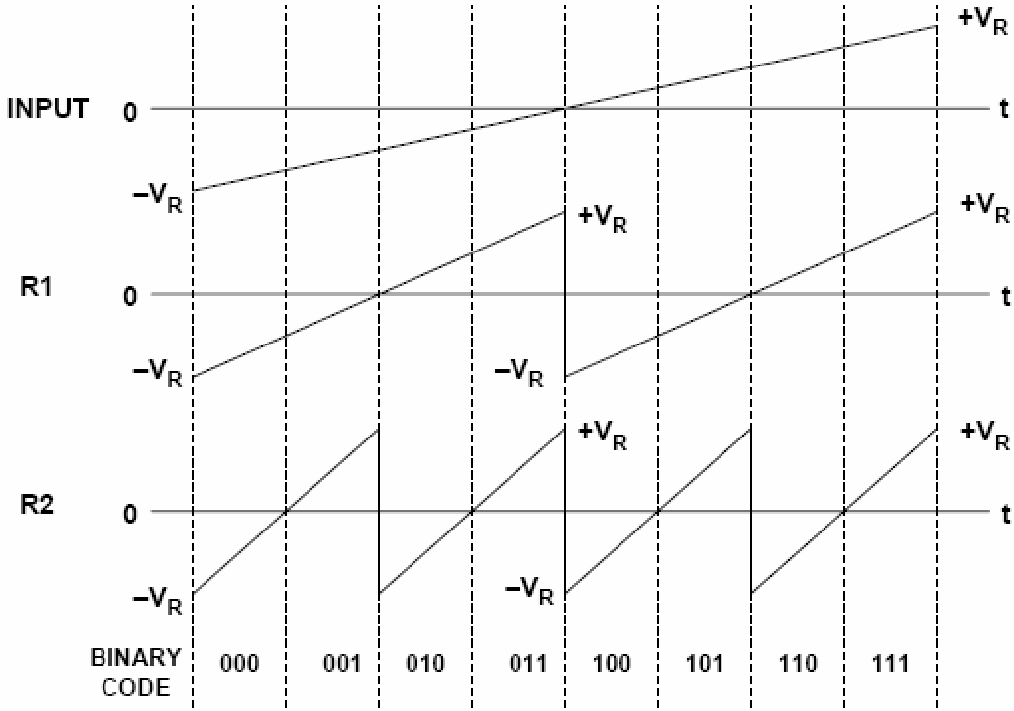


Figure 3.92: *Input and Residue Waveforms of 3-Bit Binary Ripple ADC*

Notes

Notes

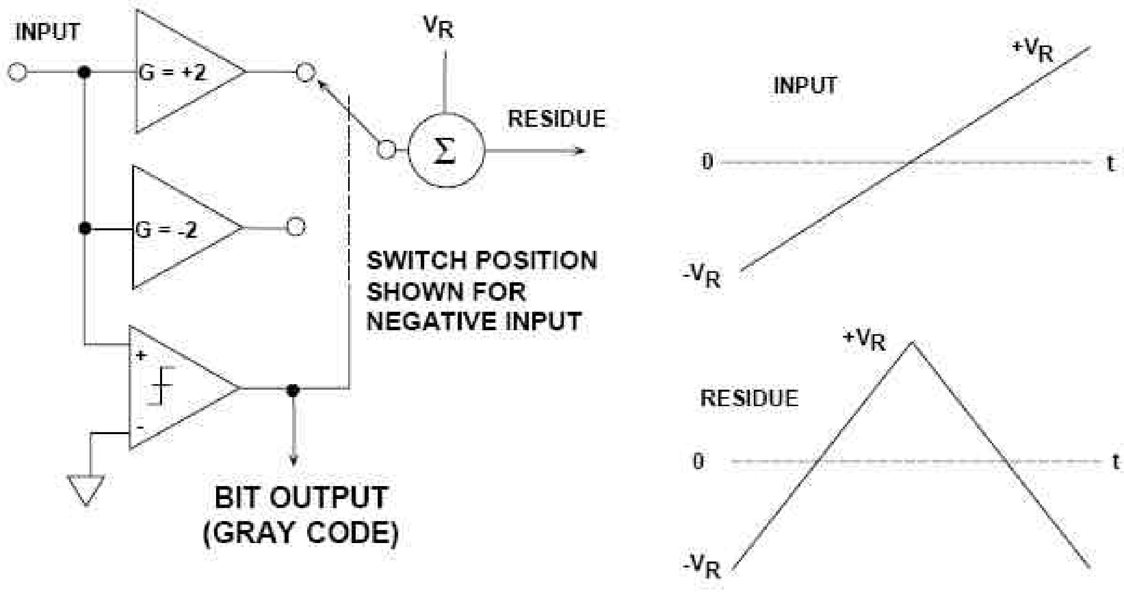


Figure 3.93: *Folding Stage Functional Equivalent Circuit*

Notes

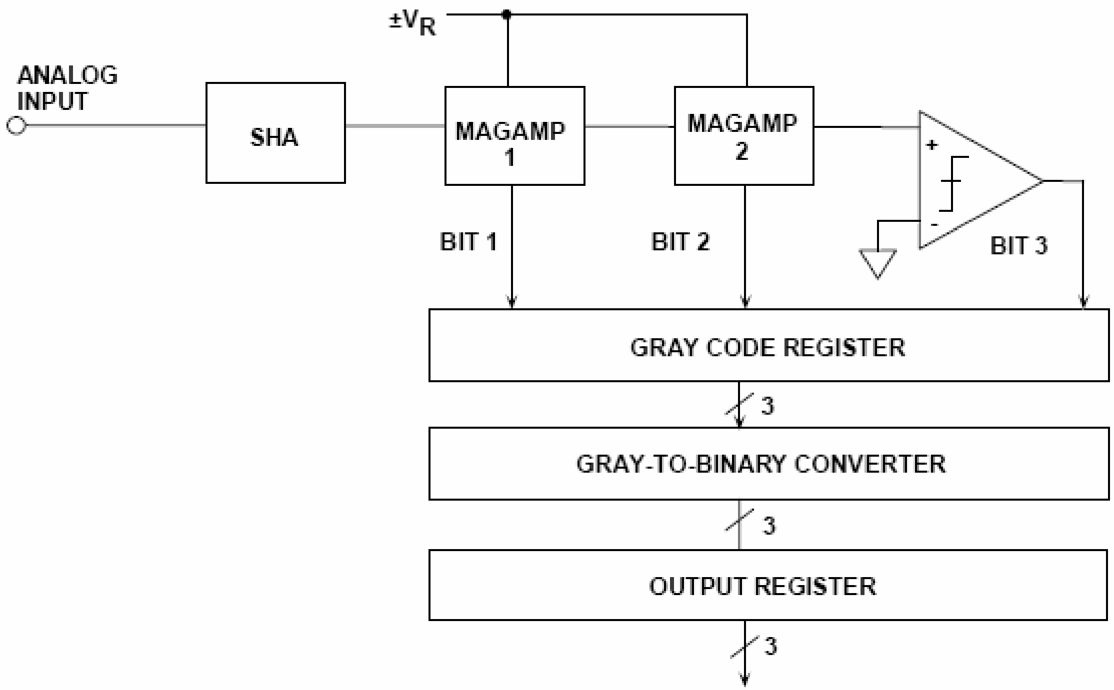


Figure 3.94: *3-bit Folding ADC Block Diagram*

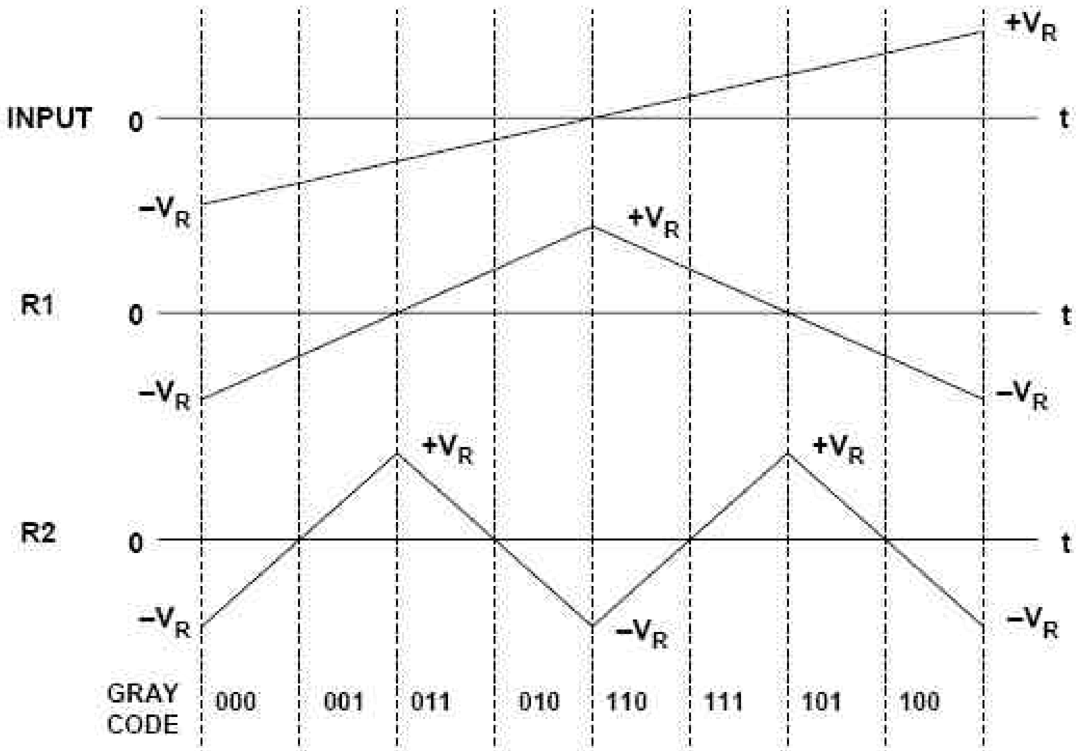
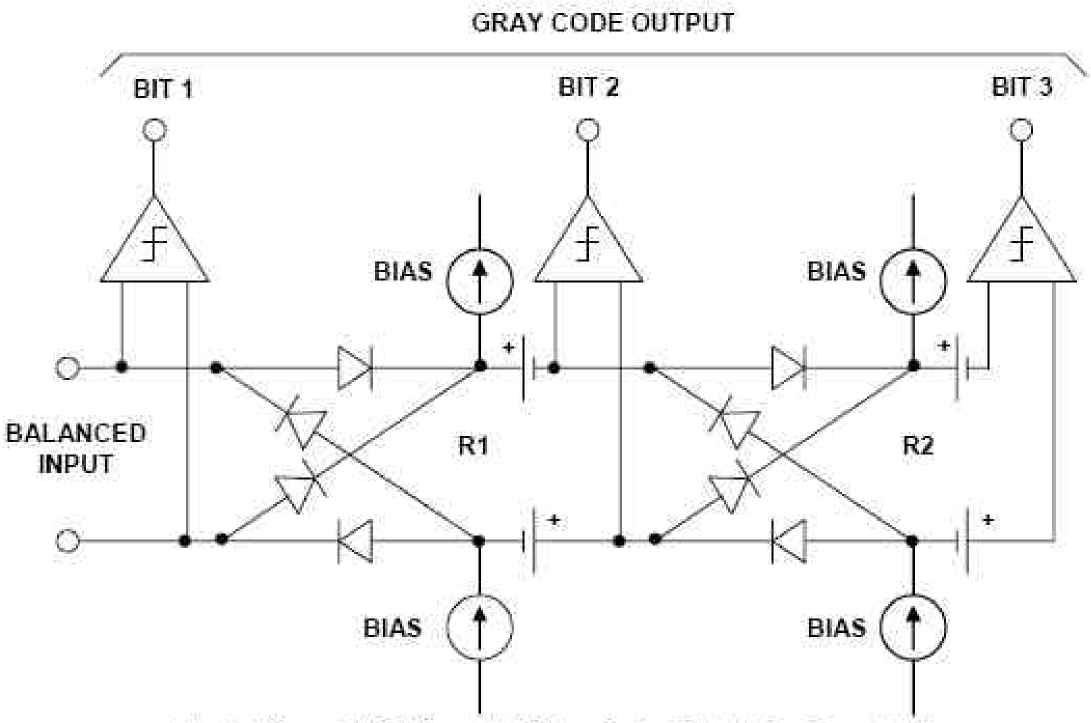


Figure 3.95: *Input and Residue Waveforms for 3-Bit Folding ADC*

Notes

Notes



Adapted from: N. E. Chasek, "Pulse Code Modulation Encoder,"
U.S. Patent 3,035,258, Filed November 14, 1960, Issued May 15, 1962

Figure 3.96: *3-Bit Folding ADC Based on N. E. Chasek's Design*

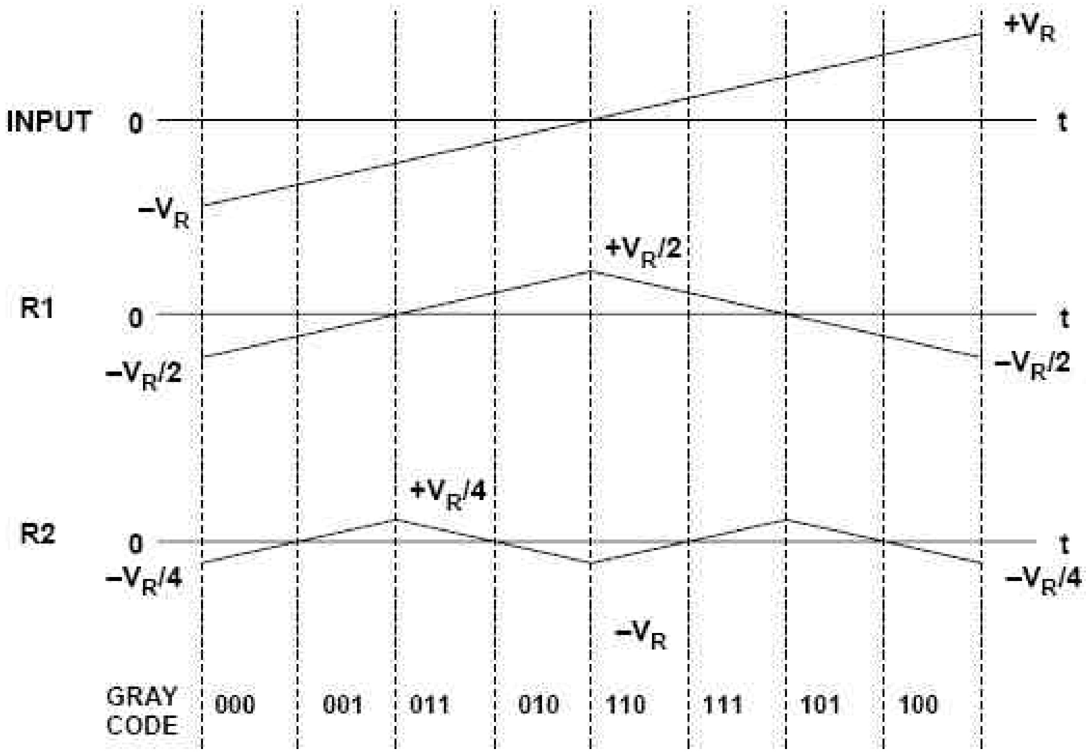
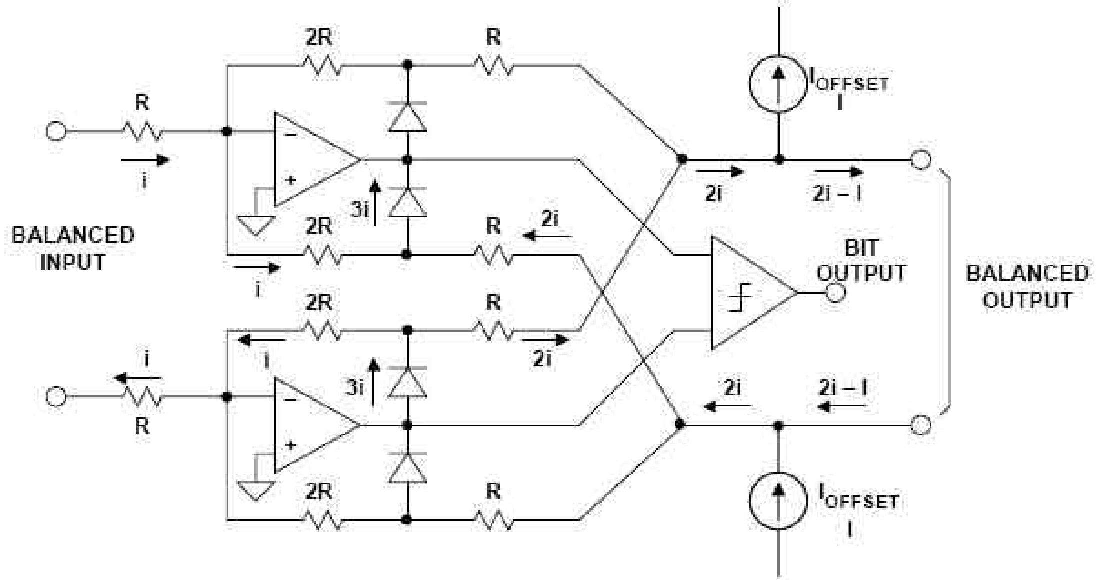


Figure 3.97: *Single-Ended Waveforms in Chasek's Folding ADC*

Notes

Notes



Extracted from: F. D. Waldhauer, "Analog-to-digital Converter," *U.S. Patent 3,187,325*, Filed July 2, 1962, Issued June 1, 1965

Figure 3.98: *F. D. Waldhaur's Classic Folding Stage using Rectifier Amplifiers*

Notes

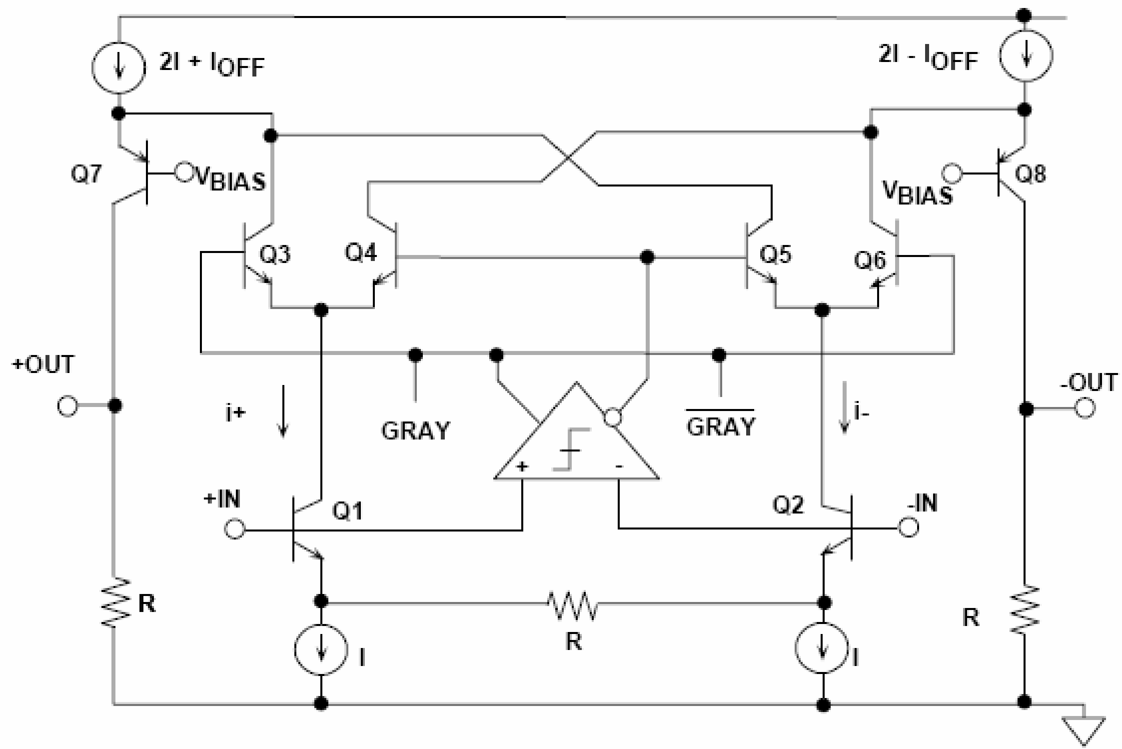


Figure 3.99: A Modern Current-Steering MagAMP™ Stage

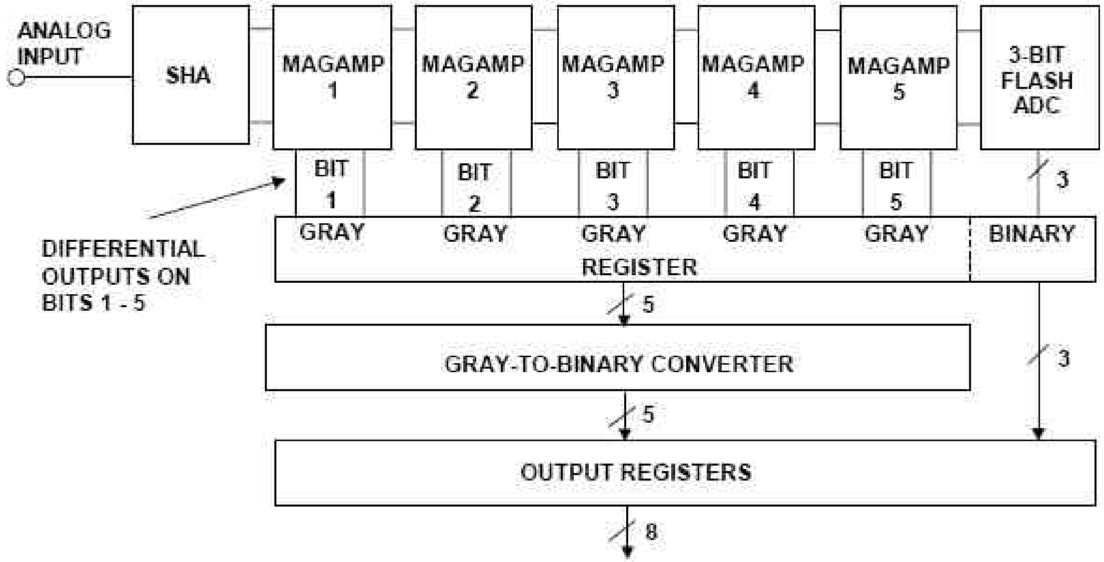


Figure 3.100: *AD9054A 8-bit, 200-MSPS ADC Functional Diagram*

Notes

Notes

◆ Reeve's counting ADC	1939
◆ Successive approximation	1946
◆ Flash (electron tube coders)	1948
◆ Bit-per-stage (binary and folding-Gray)	1956
◆ Subranging	1956
◆ Subranging with error correction	1964
◆ Pipeline with error correction	1966

Note: Dates are first publications or patent filings

Figure 3.101: *High Speed ADC Architecture Timeline*

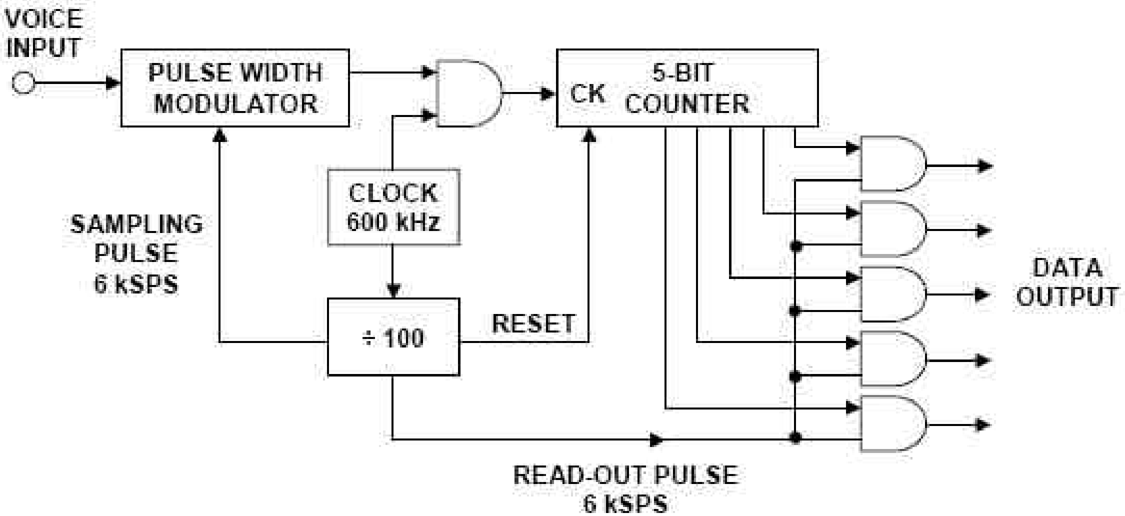
Notes

◆ Reeve's counting ADC	1939
◆ Charge run-down:	1946
◆ Ramp run-up	1951
◆ Tracking	1950
◆ Voltage-to-frequency converter (VFC)	1952
◆ Dual Slope	1957
◆ Triple Slope	1967
◆ Quad Slope	1973

Note: Dates are first publications or patent filings

Figure 3.102: *Counting and Integrating ADC Architecture Timeline*

Notes



Adapted from: Alec Harley Reeves, "Electric Signaling System,"
***U.S. Patent 2,272,070*, Filed November 22, 1939, Issued February 3, 1942**

Figure 3.103: *A. H. Reeves' 5-bit Counting ADC*

Notes

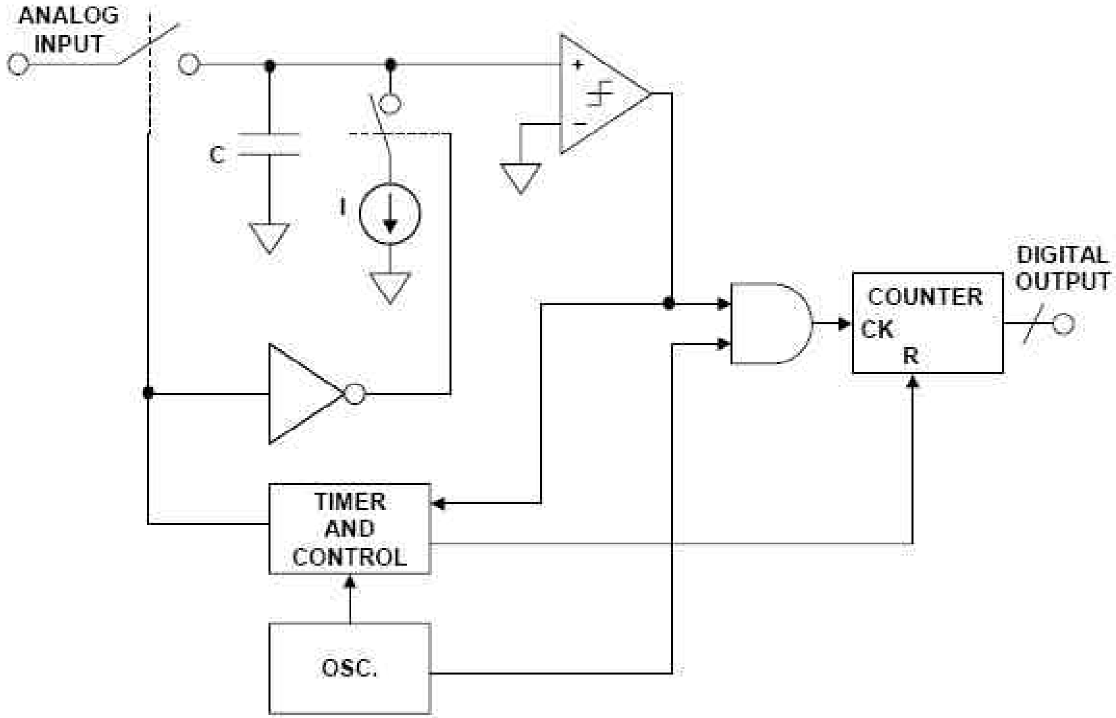


Figure 3.104: *Charge Run-Down ADC*

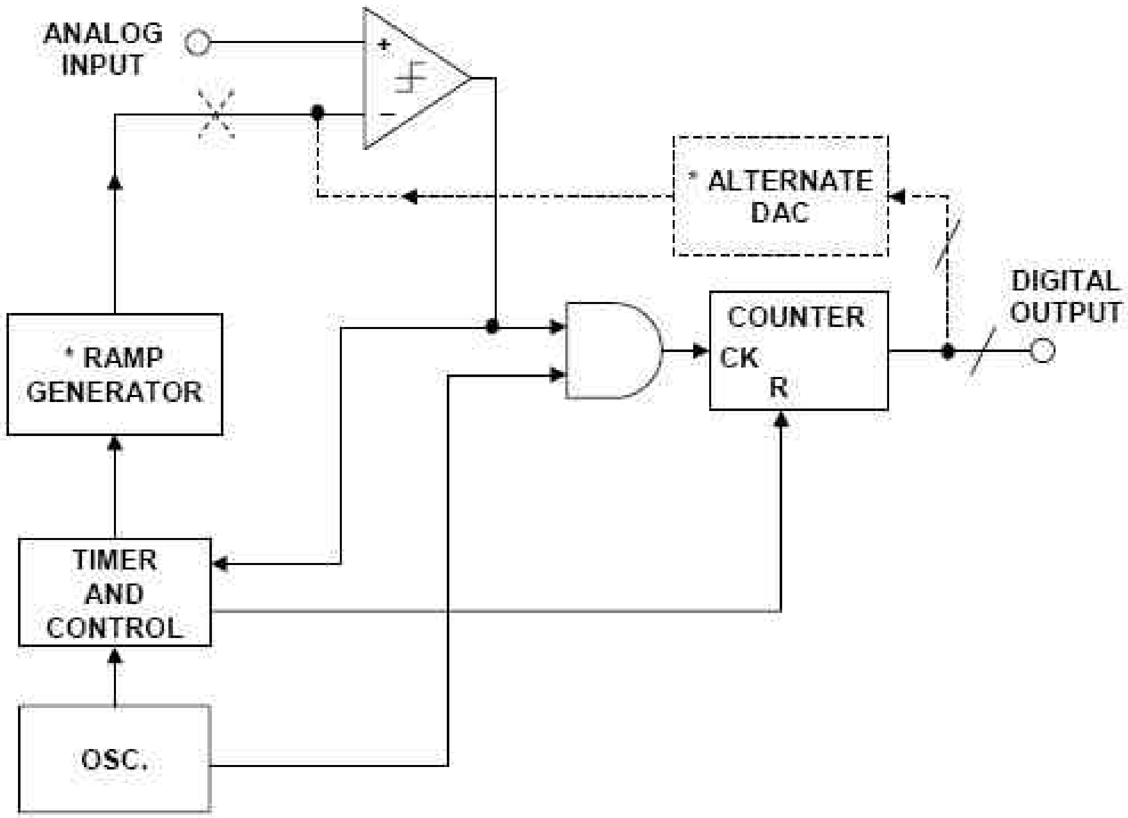


Figure 3.105: *Ramp Run-Up ADC*

Notes

Notes

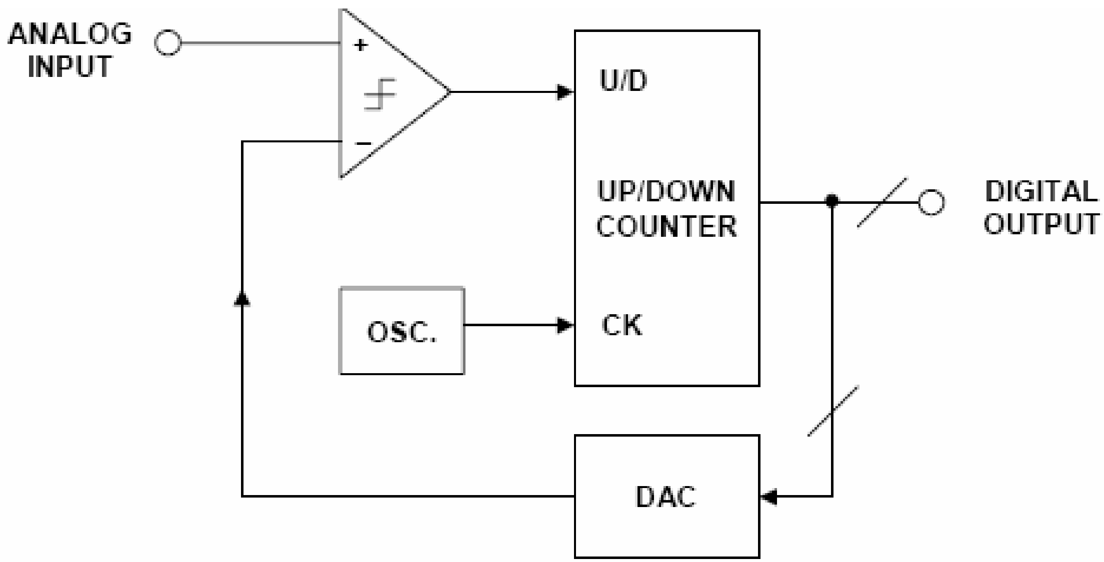
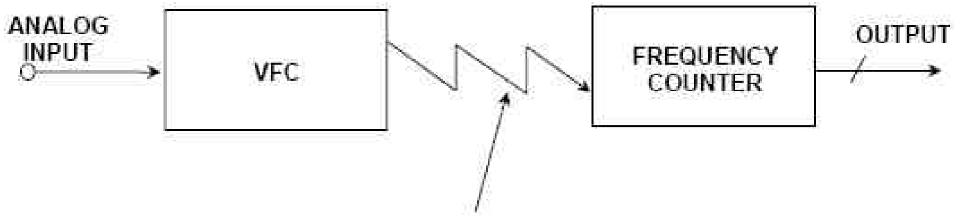


Figure 3.106: *Tracking ADC*



- CONNECTION NEED NOT BE DIRECT
- CIRCUIT IS IDEAL FOR TELEMETRY

Figure 3.107: *Voltage-to-Frequency Converter (VFC) and Frequency Counter Make a Low-Cost, Versatile, High-Resolution ADC*

Notes

Notes

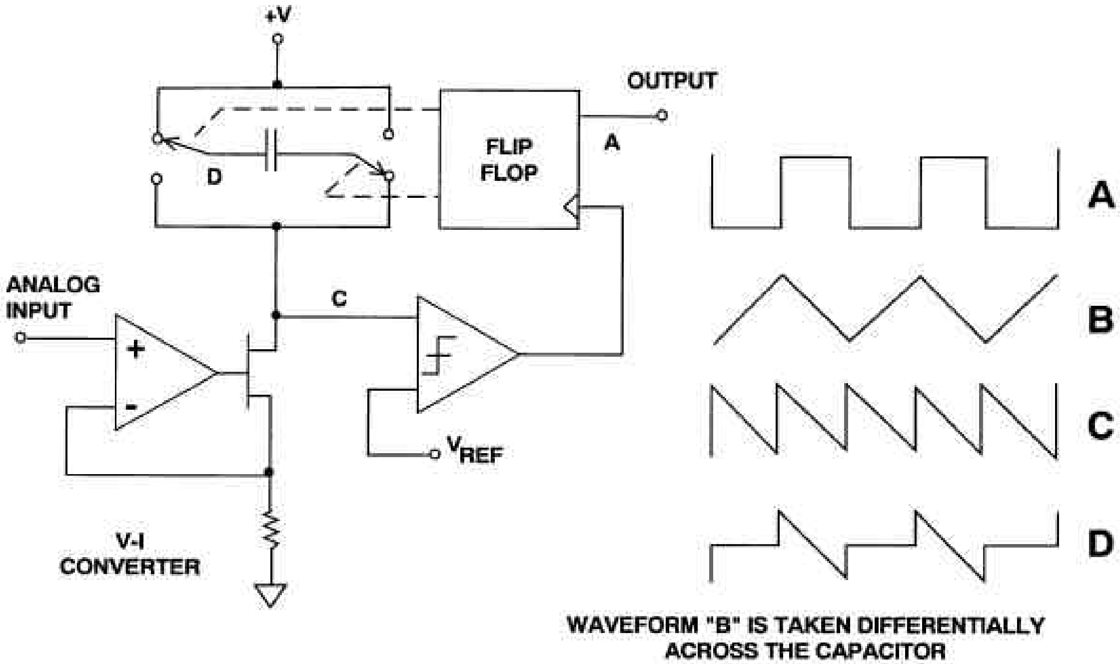


Figure 3.108: *A Current-Steering VFC*

Notes

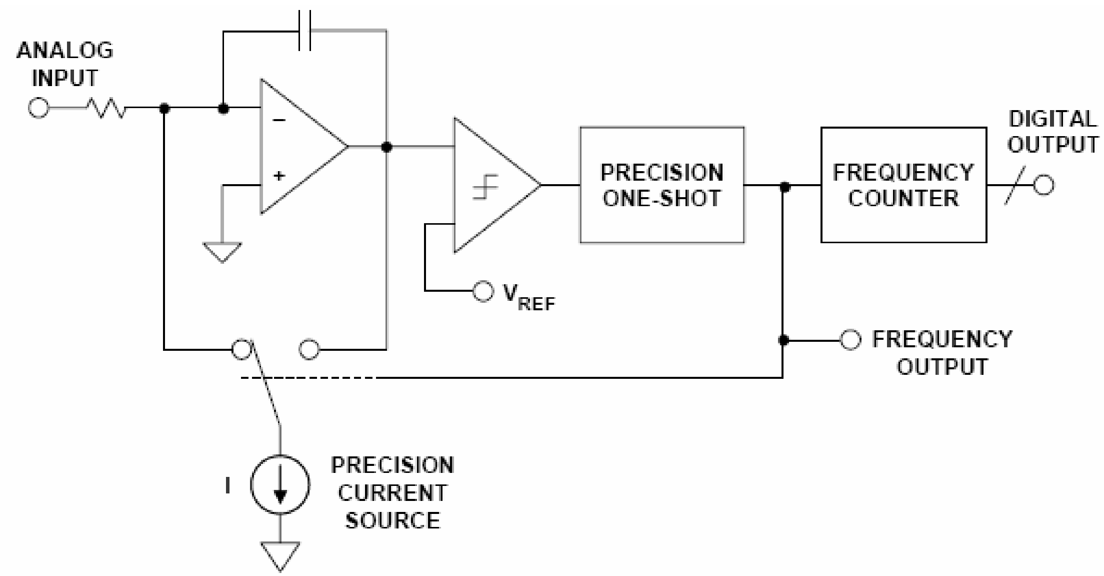


Figure 3.109: *Charge Balance Voltage-to-Frequency Converter (VFC)*

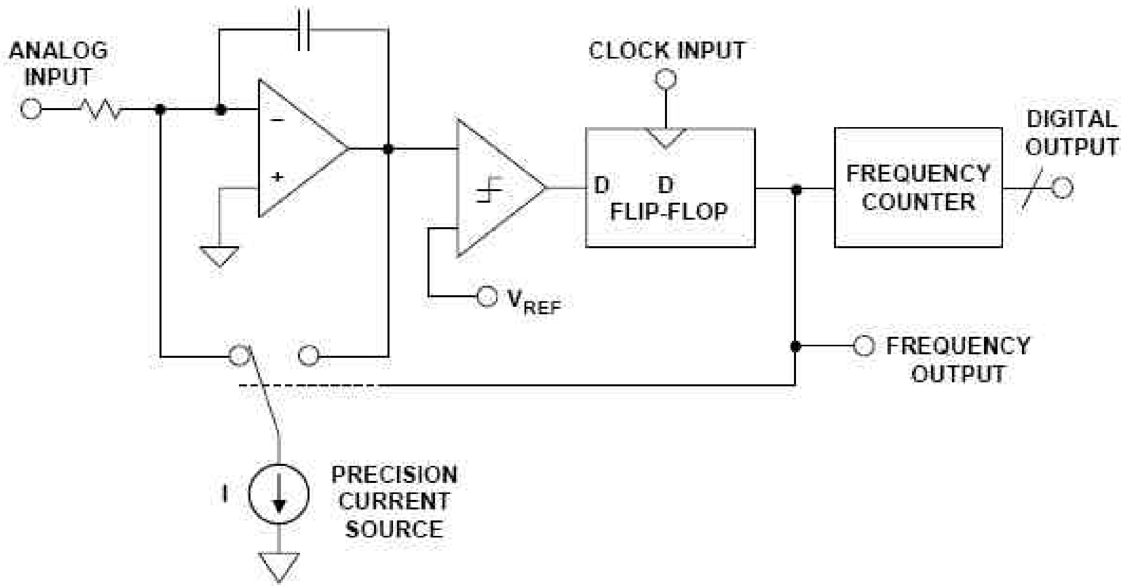


Figure 3.110: *Synchronous VFC (SVFC)*

Notes

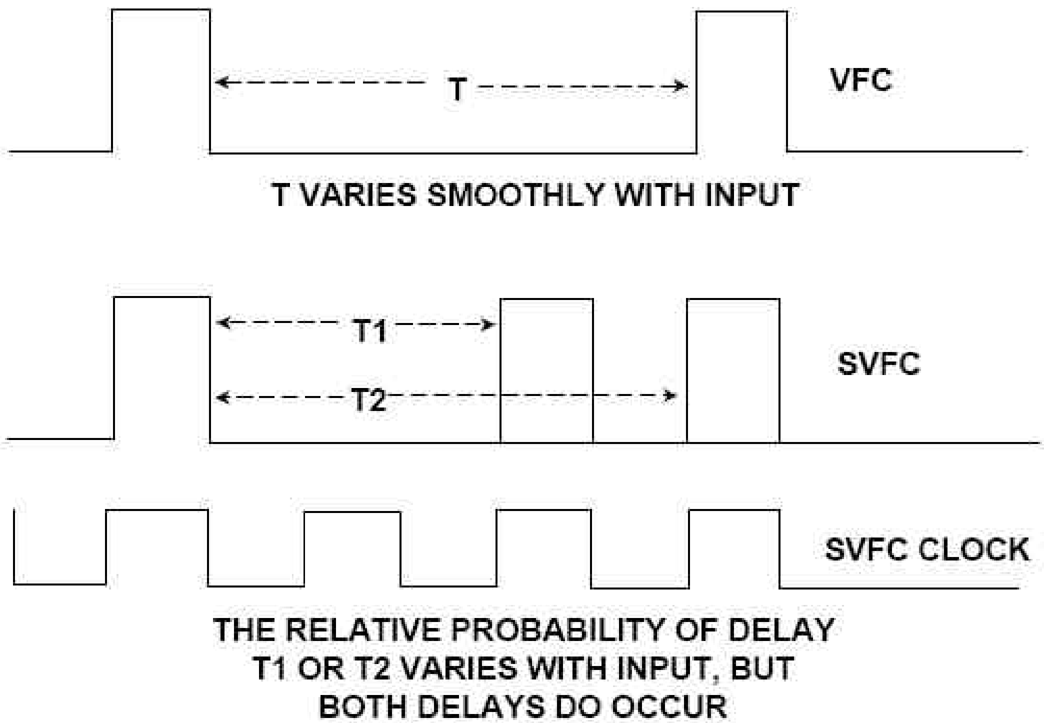
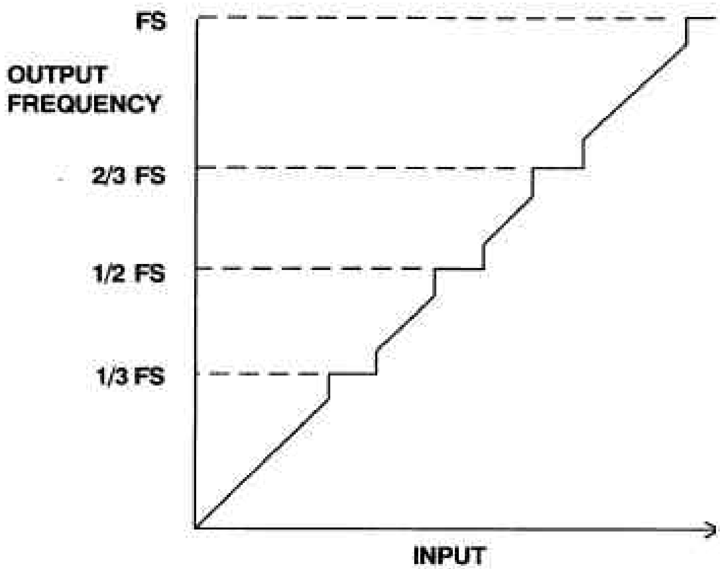


Figure 3.111: *VFC and SVFC Waveforms*

Notes

Notes



- Nonlinearities caused by injection locking due to clock feedthrough
- Should only be 6-8 LSBs at 18-bits with proper layout and decoupling
- Nonlinearities occur at subharmonics of the clock, where FS = $F_{clock}/2$

Figure 3.112: *SVFC Nonlinearity*

Notes

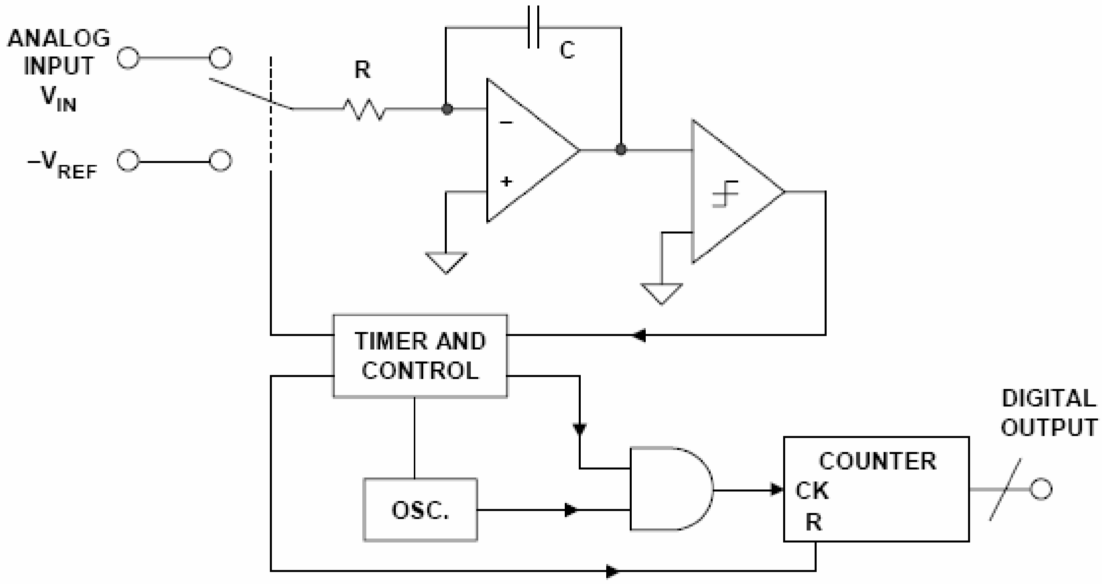
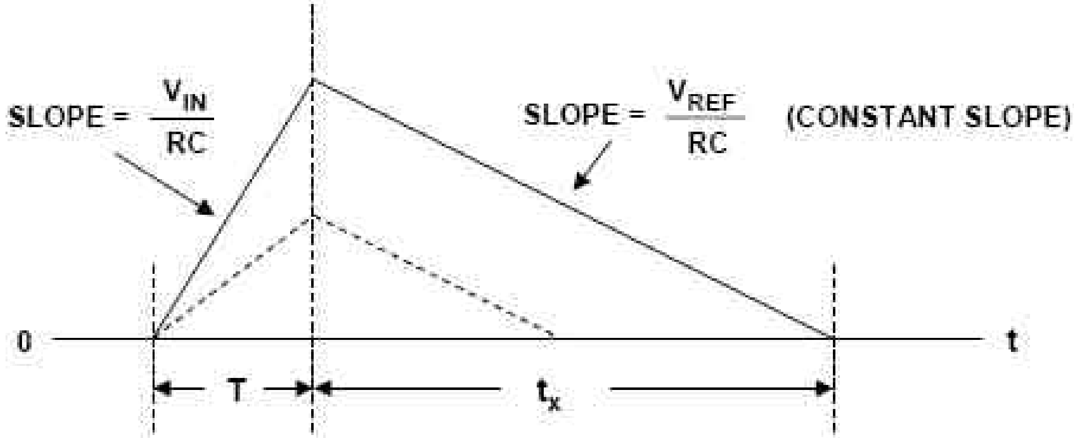


Figure 3.113: *Dual slope ADC*



$$\frac{V_{IN}}{RC} T = \frac{V_{REF}}{RC} t_x$$

$$t_x = \frac{V_{IN}}{V_{REF}} T$$

HIGH NORMAL MODE REJECTION AT MULTIPLES OF $\frac{1}{T}$

Figure 3.114: *Dual Slope ADC Integrator Output Waveforms*

Notes

Notes

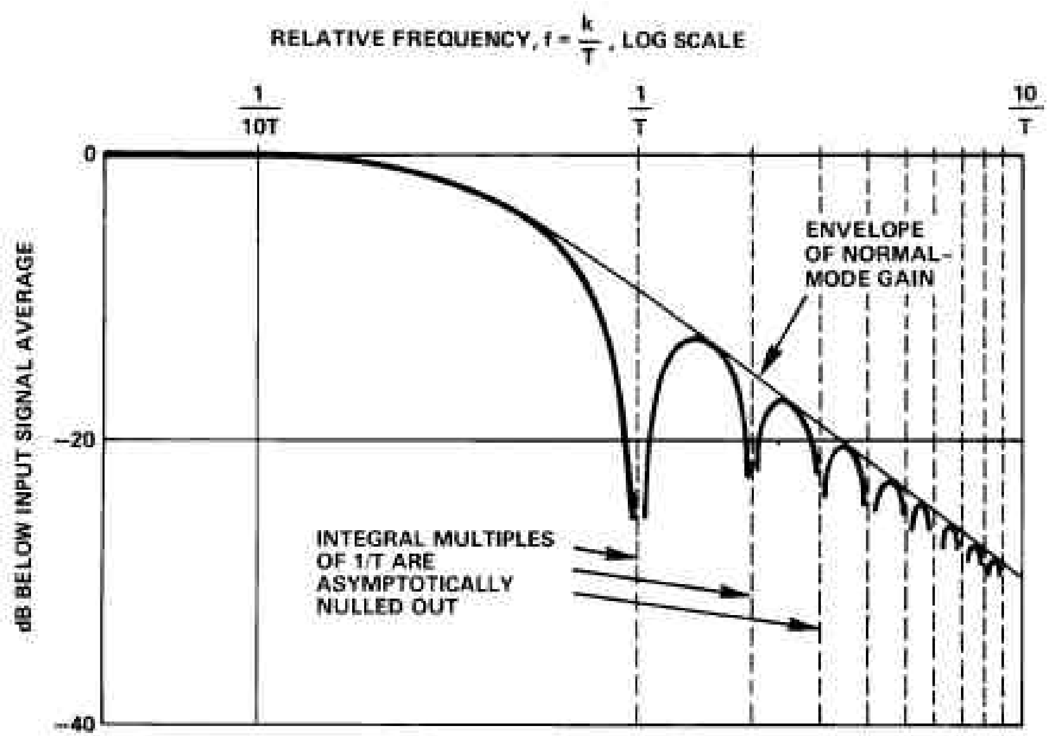


Figure 3.115: *Frequency Response of Integrating ADC*

Notes

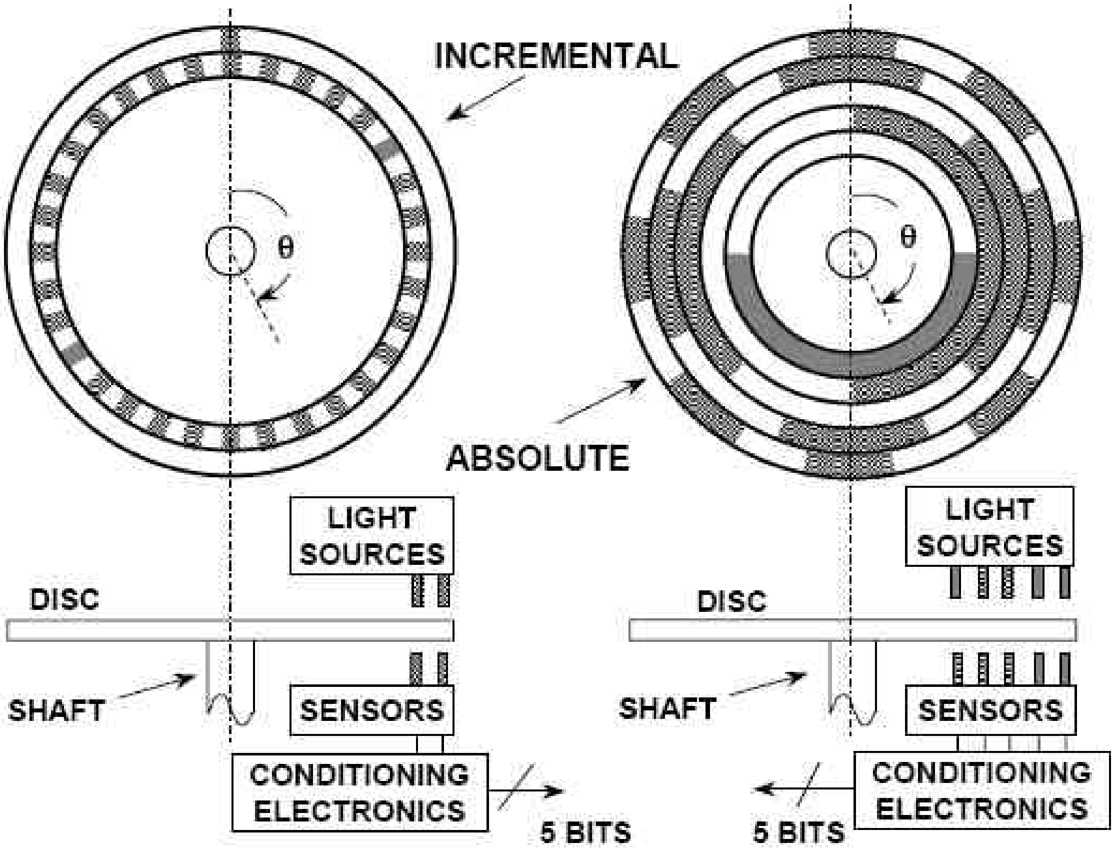


Figure 3.116: *Incremental and Absolute Optical Encoders*

Notes

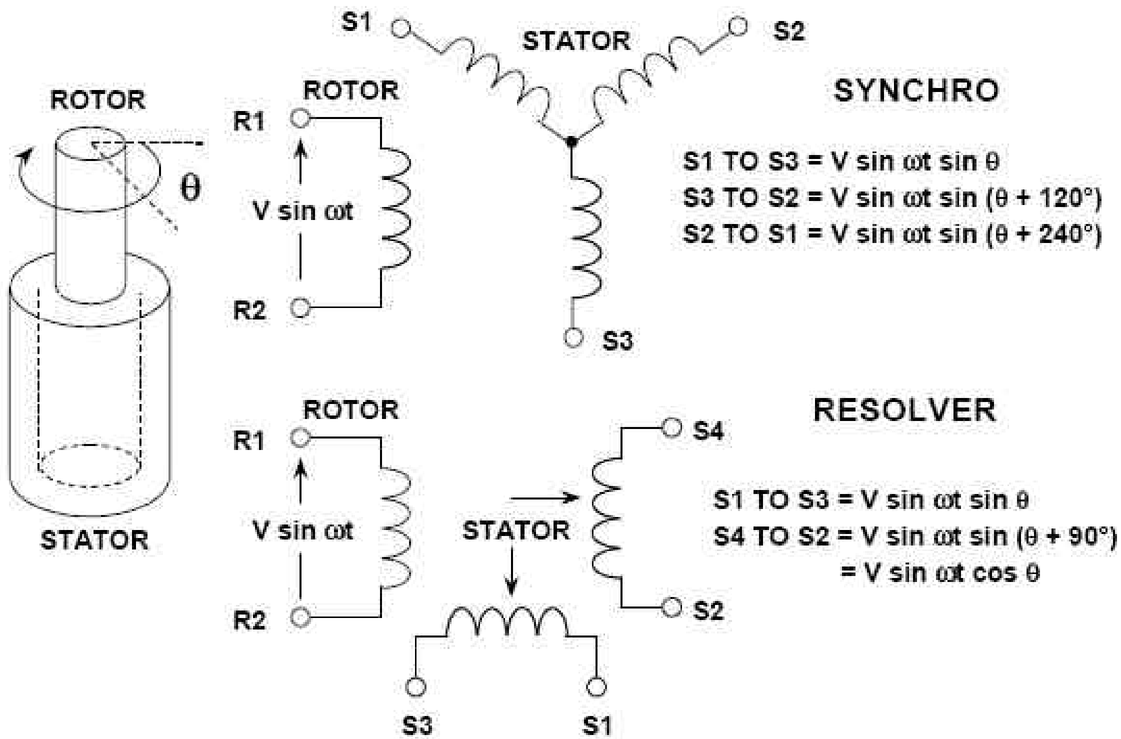


Figure 3.117: *Synchros and Resolvers*

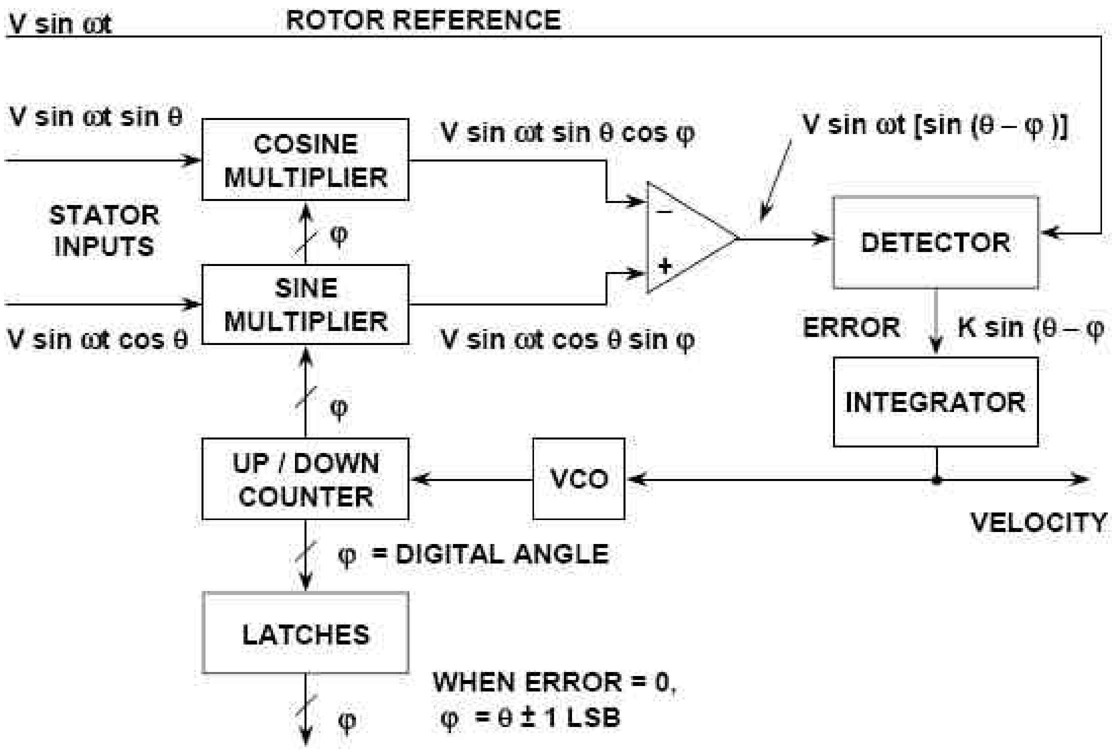


Figure 3.118: *Resolver-to-Digital Converter (RDC)*

Notes

Notes

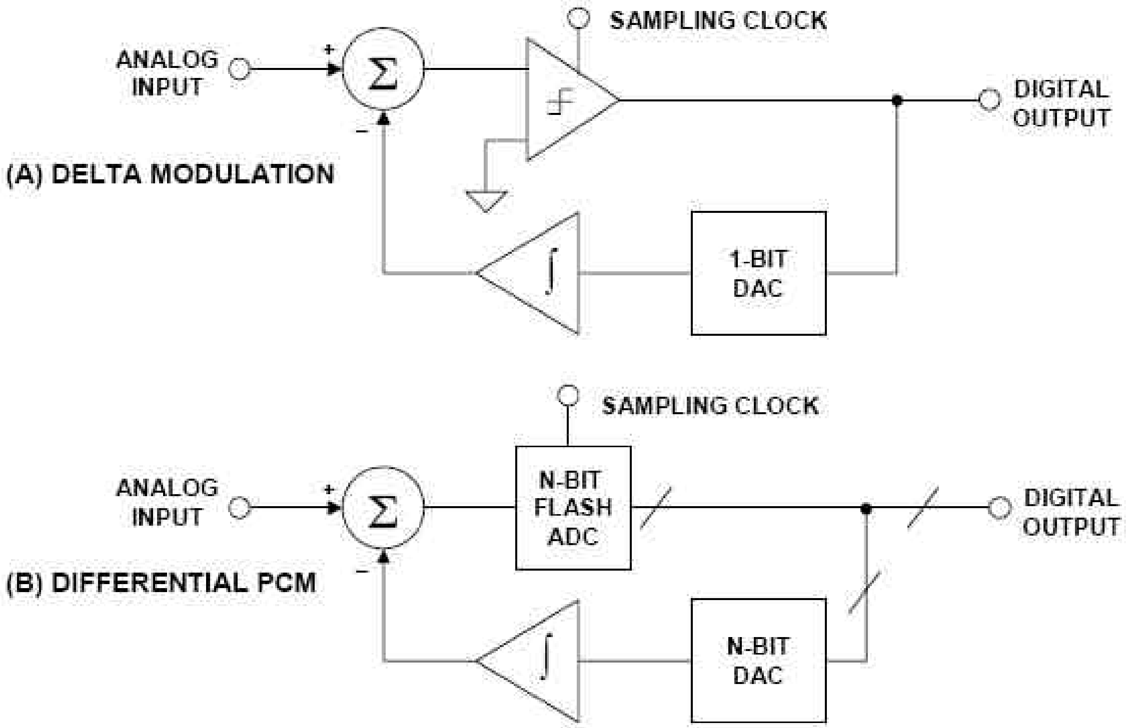


Figure 3.119: *Delta Modulation and Differential PCM*

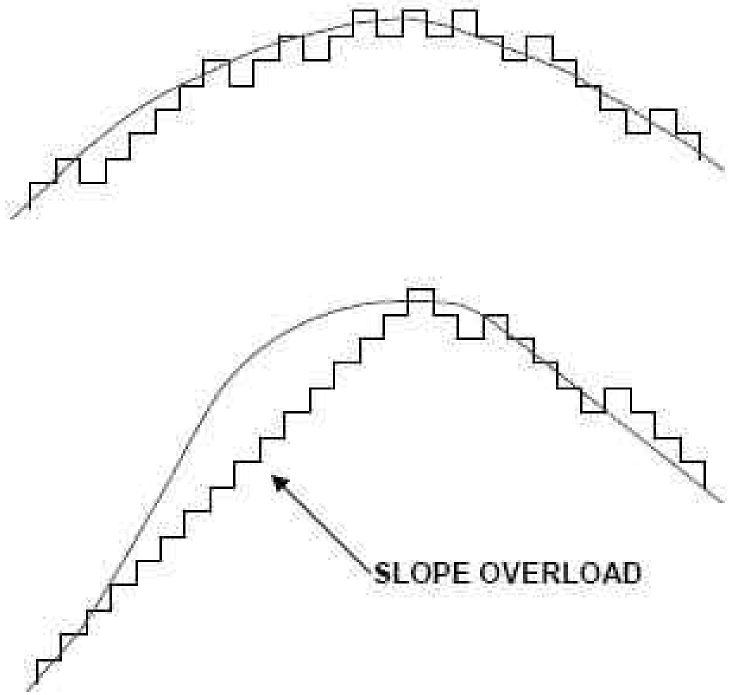


Figure 3.120: *Quantization Using Delta Modulation*

Notes

Notes

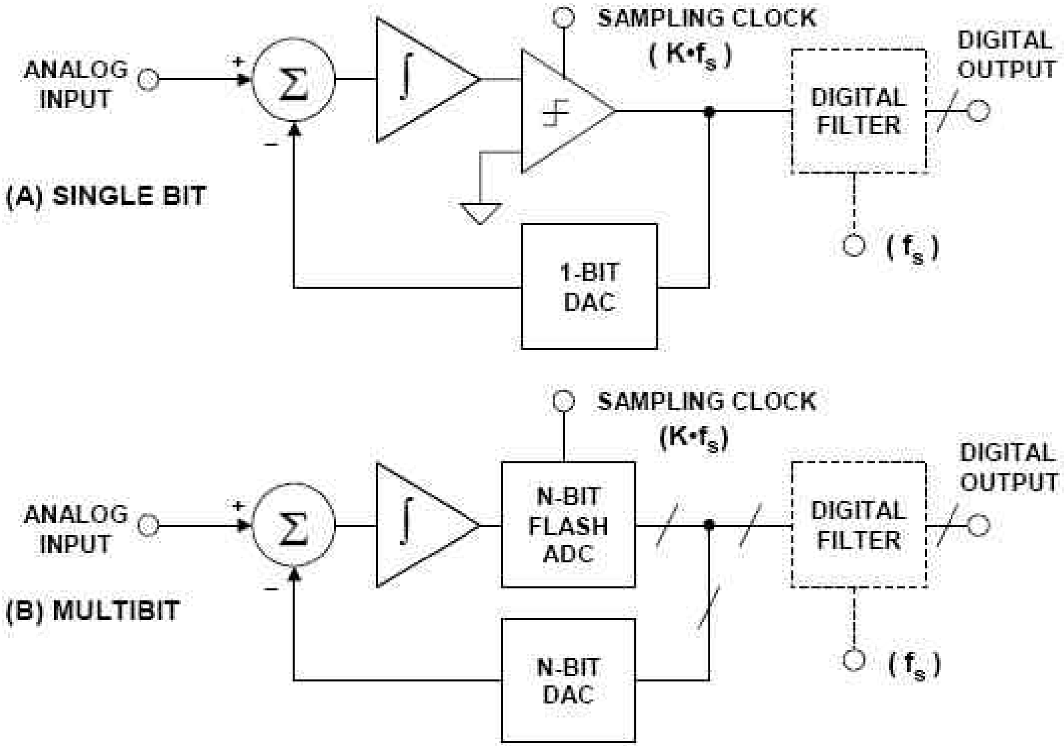


Figure 3.121: *Single and Multibit Sigma-Delta ADCs*

Notes

◆ Delta Modulation	1950
◆ Differential PCM	1950
◆ Single and multibit oversampling with noise shaping	1954
◆ First called Δ-Σ, "delta-sigma"	1962
◆ Addition of digital filtering and decimation for Nyquist ADC	1969
◆ Bandpass Sigma-Delta	1988

Note: Dates are first publications or patent filings

Figure 3.122: *Sigma-Delta ADC Architecture Timeline*

Notes

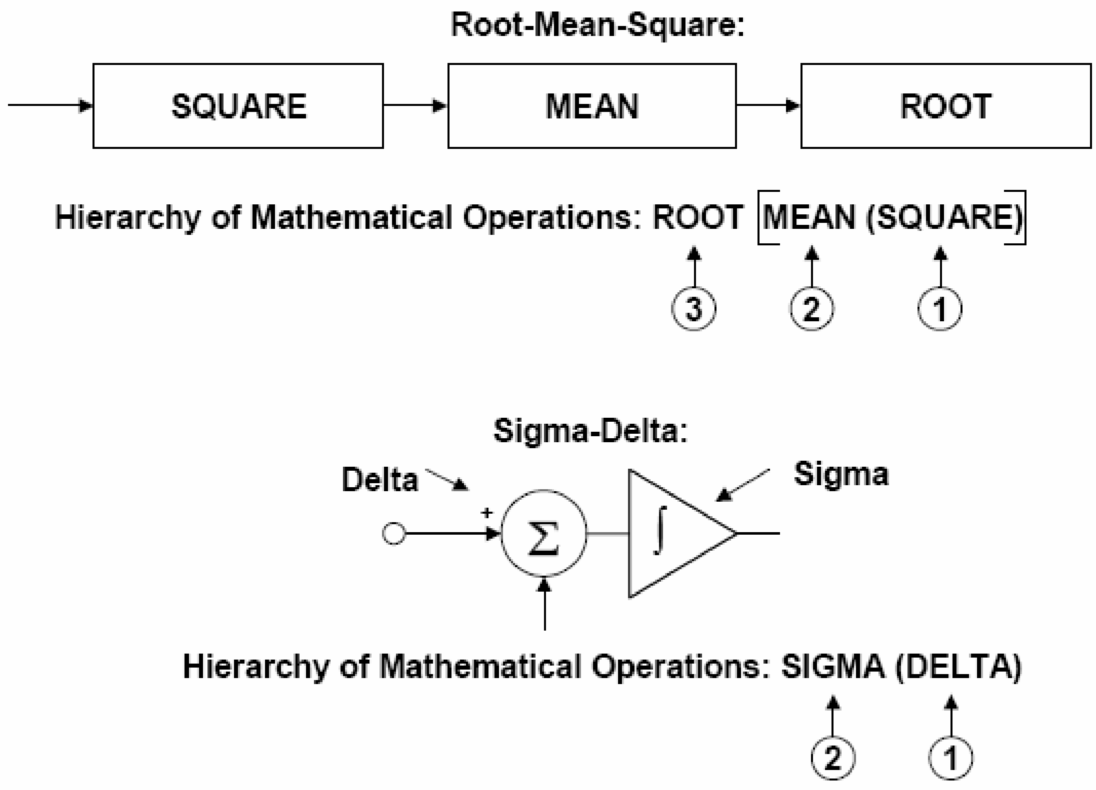


Figure 3.123: *Sigma-Delta (Σ-Δ) or Delta-Sigma (Δ-Σ)?*

- Low Cost, High Resolution (to 24-bits)
- Excellent DNL
- Low Power, but Limited Bandwidth (Voiceband, Audio)
- Key Concepts are Simple, but Math is Complex
  - Oversampling
  - Quantization Noise Shaping
  - Digital Filtering
  - Decimation
- Ideal for Sensor Signal Conditioning
  - High Resolution
  - Self, System, and Auto Calibration Modes
- Wide Applications in Voiceband and Audio Signal Processing

Figure 3.124: *Sigma-Delta ADCs*

Notes

Notes

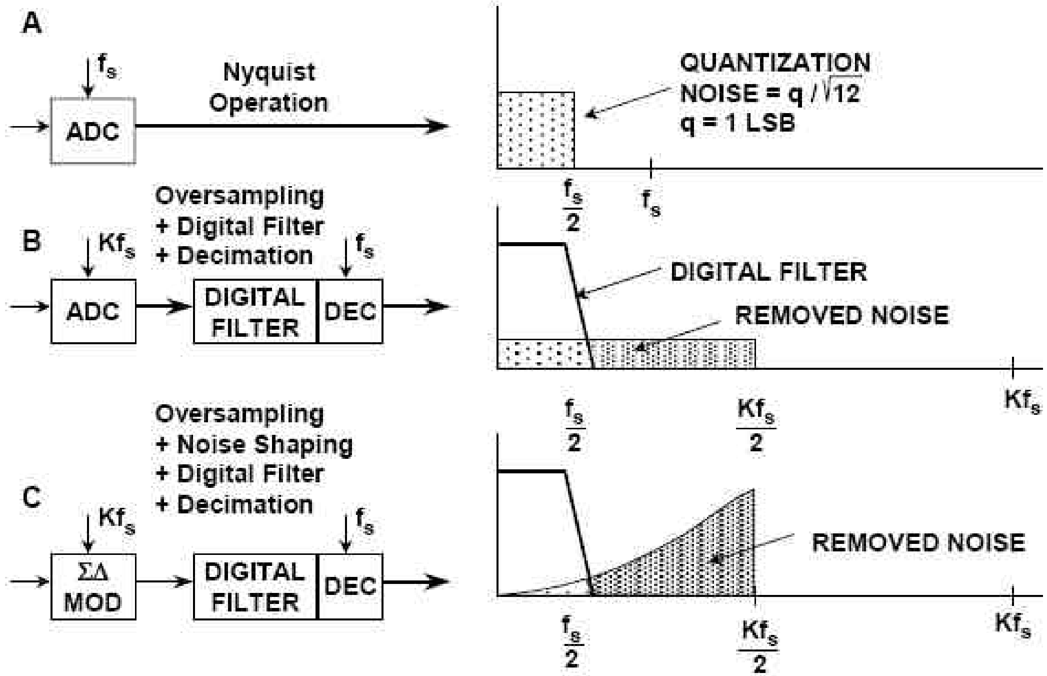


Figure 3.125: *Oversampling, Digital Filtering, Noise Shaping, and Decimation*

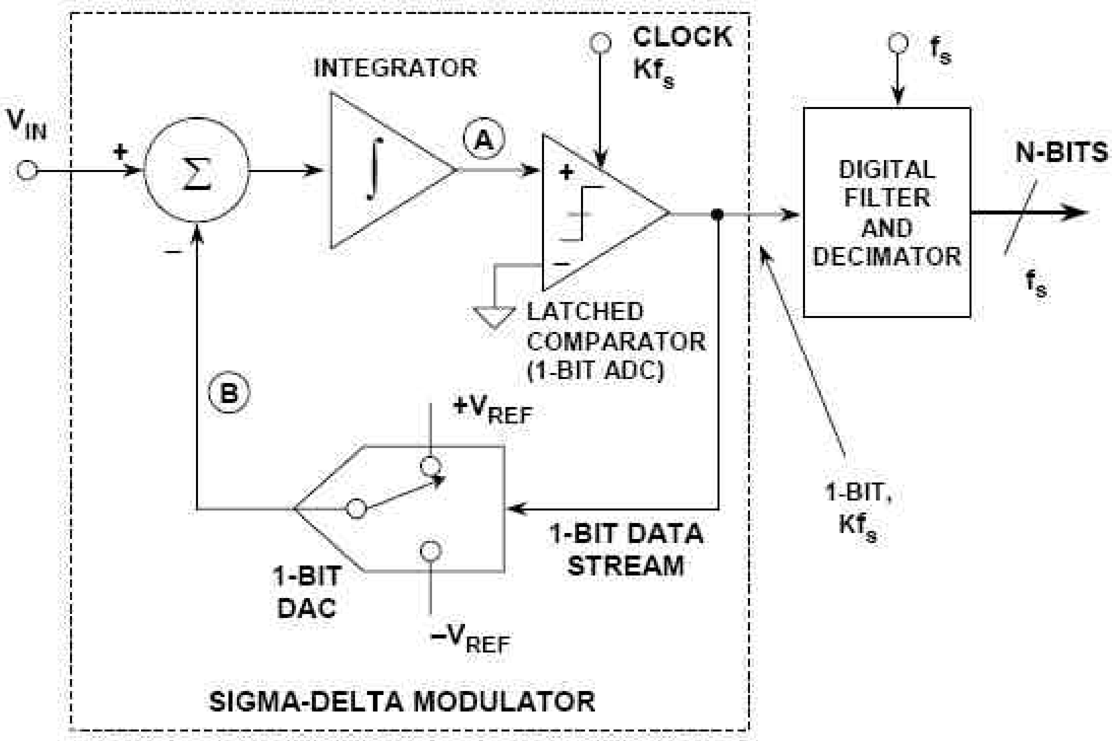


Figure 3.126: *First-Order Sigma-Delta ADC*

Notes

Notes

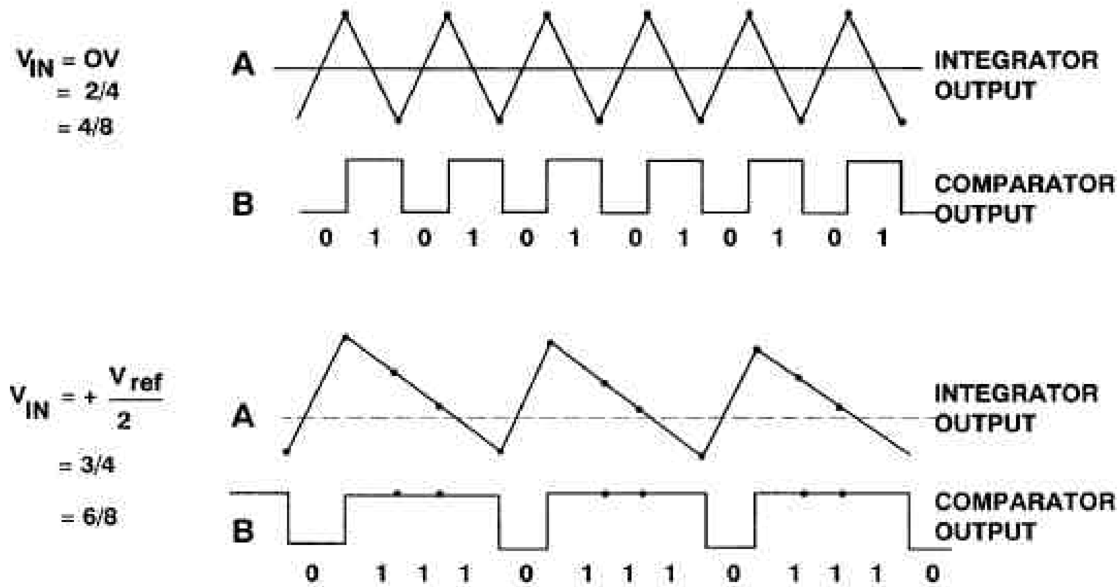
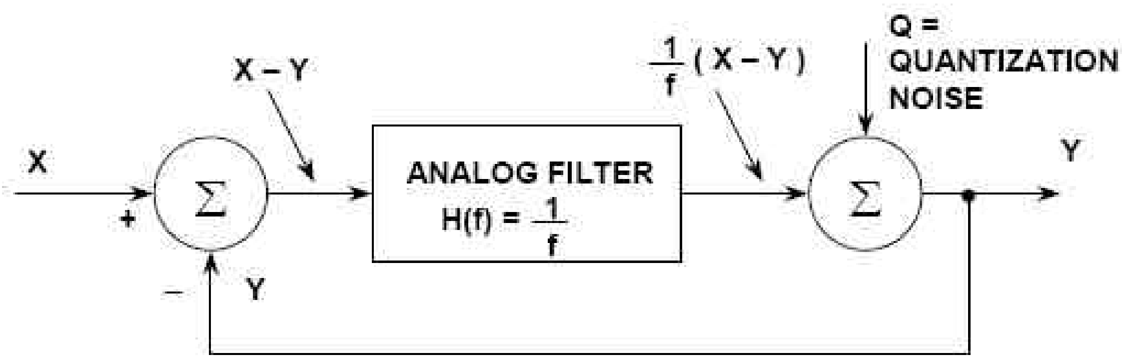


Figure 3.127: *Sigma-Delta Modulator Waveforms*

Notes



$$Y = \frac{1}{f}(X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \underbrace{\frac{X}{f+1}}_{\text{SIGNAL TERM}} + \underbrace{\frac{Q\,f}{f+1}}_{\text{NOISE TERM}}$$

Figure 3.128: *Simplified Frequency Domain Linearized Model of a Sigma-Delta Modulator*

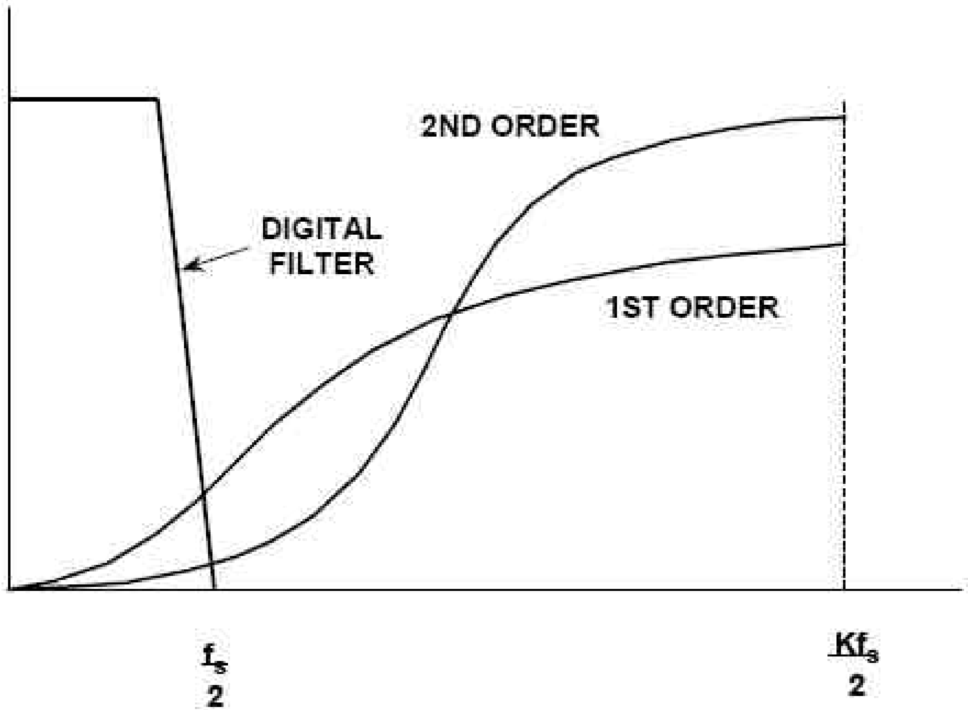


Figure 3.129: *Sigma-Delta Modulators Shape Quantization Noise*

Notes

Notes

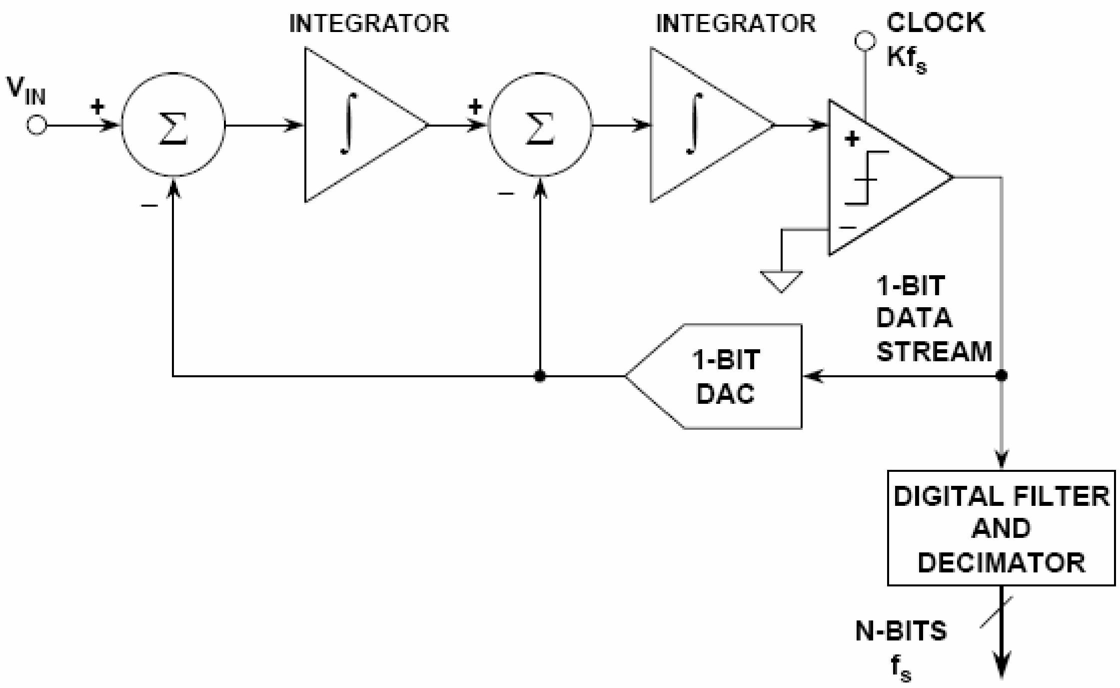


Figure 3.130: *Second-Order Sigma-Delta ADC*

Notes

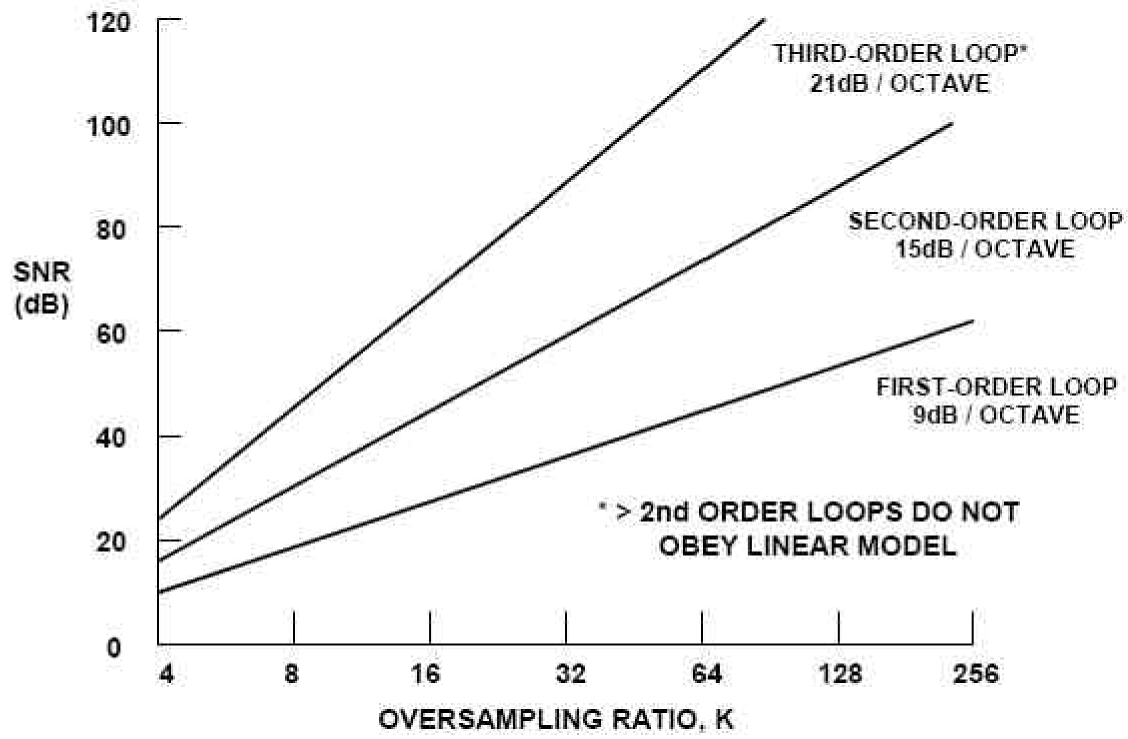


Figure 3.131: *SNR Versus Oversampling Ratio for First, Second, and Third-Order Loops*

Notes

16 SAMPLES OF SIGMA-DELTA MODULATOR DATA OUTPUT STREAM		BINARY EQUIVALENT
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 . . . 8/16	=	1000
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 . . . 9/16	=	1001

REPEATS EVERY 16 SAMPLES

Figure 3.132: *Repetitive Bit Pattern in Sigma-Delta Modulator Output*

Notes

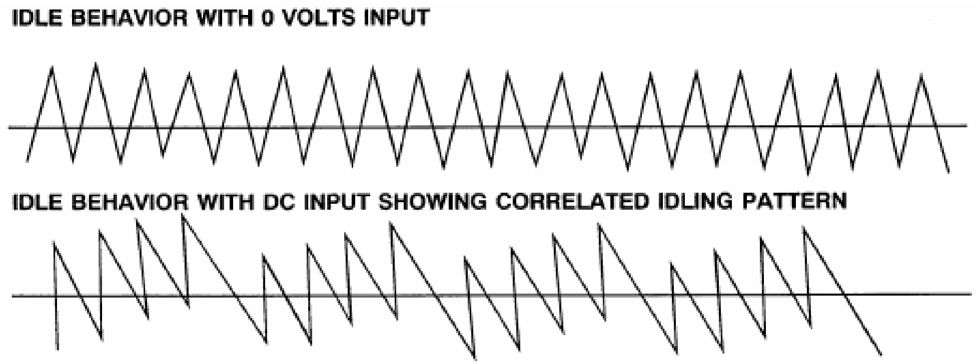


Figure 3.133: *Idling Patterns for First-Order Sigma-Delta Modulator (Integrator Output)*

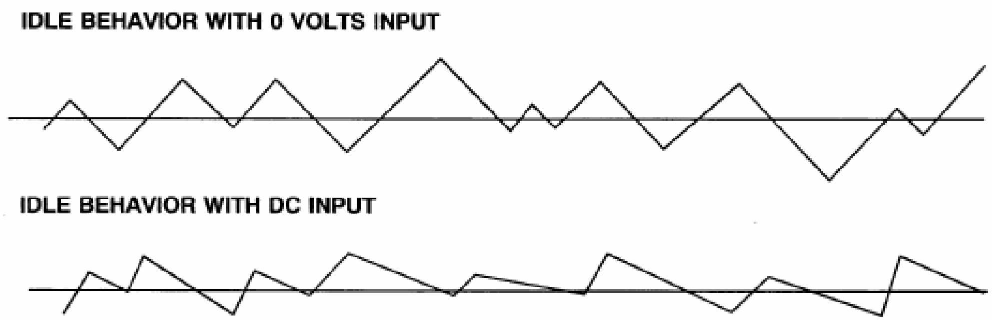


Figure 3.134: *Idling Patterns for Second-Order Sigma-Delta Modulator (Integrator Output)*

Notes

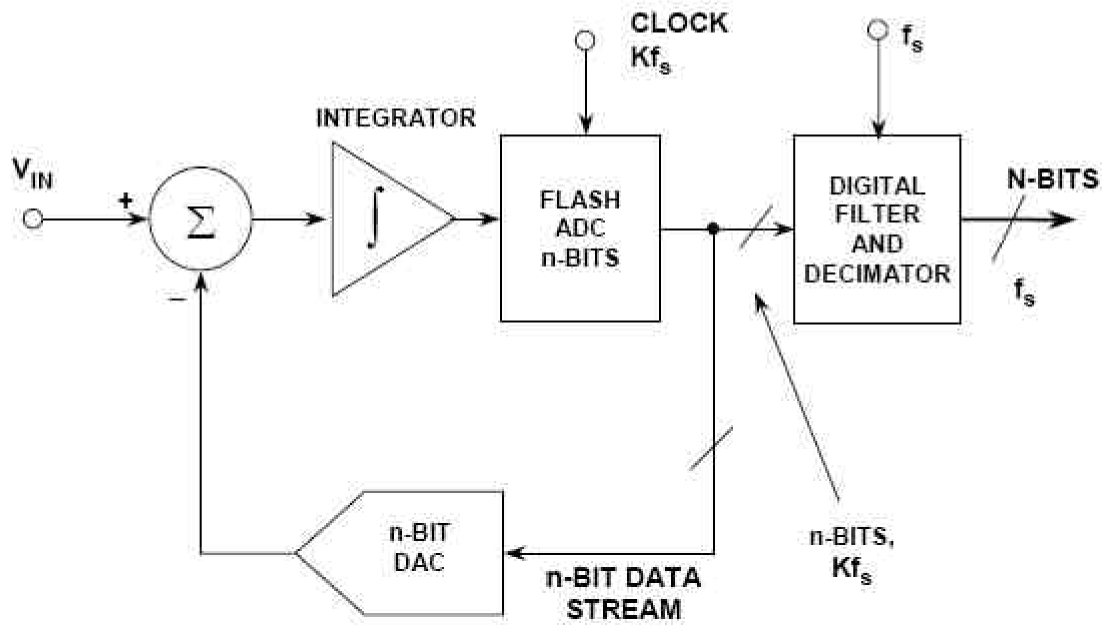


Figure 3.135: *Multi-Bit Sigma-Delta ADC*

Notes

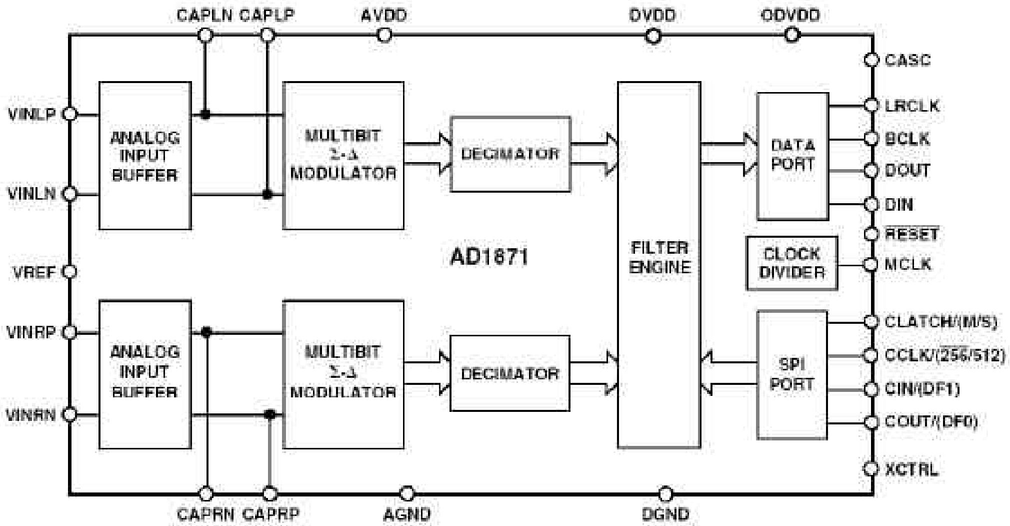


Figure 3.136: *AD1871 24-Bit 96-kSPS Stereo Audio Multi-Bit Sigma-Delta ADC*

Notes

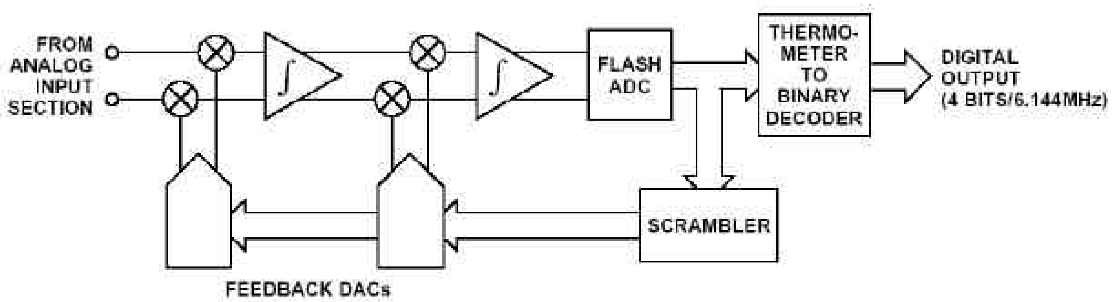


***Figure 3.137:** Details of the AD1871 Second-Order Modulator and Data Scrambler*

Notes

- Single +5 V Power Supply
- Differential Dual-Channel Analog Inputs
- 16-/20-/24-Bit Word Lengths Supported
- 105 dB (typ) A-Weighted Dynamic Range
- 103 dB (typ) THD+N (–20 dBFS input)
- 0.01 dB Decimator Filter Passband Ripple
- Second-Order, 128-/64-Times Oversampling Multibit Modulator with Data Scrambling
- Less than 350 mW (typ)
- Power-Down Mode
- On-Chip Voltage Reference
- Flexible Serial Output Interface
- 28-Lead SSOP Package

Figure 3.138: *AD1871 24-Bit, 96-kSPS Stereo Sigma-Delta ADC Key Specifications*

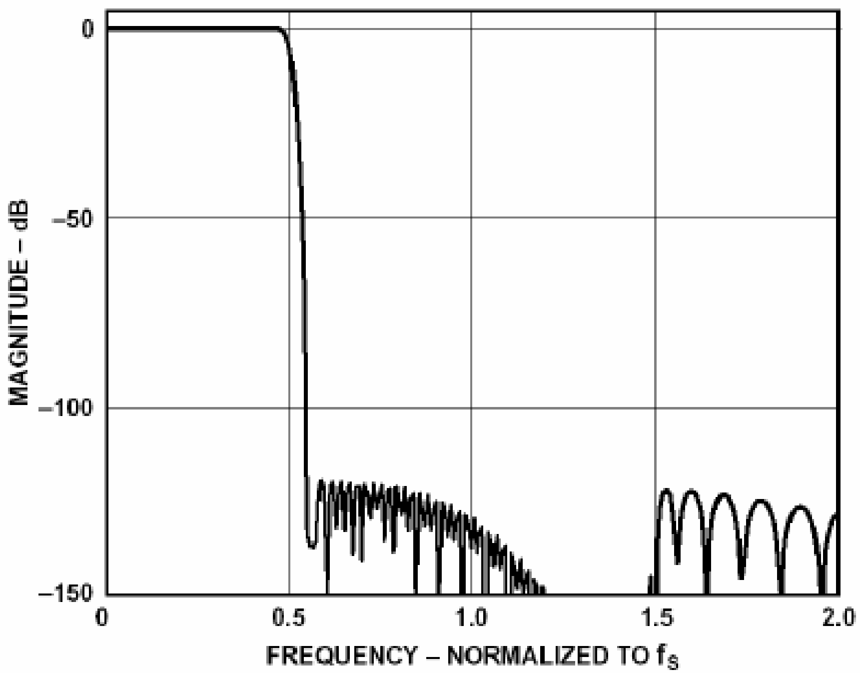


Figure 1.139: *AD1871 24-Bit, 96-kSPS Stereo Sigma-Delta ADC Digital Filter Characteristics*

Notes

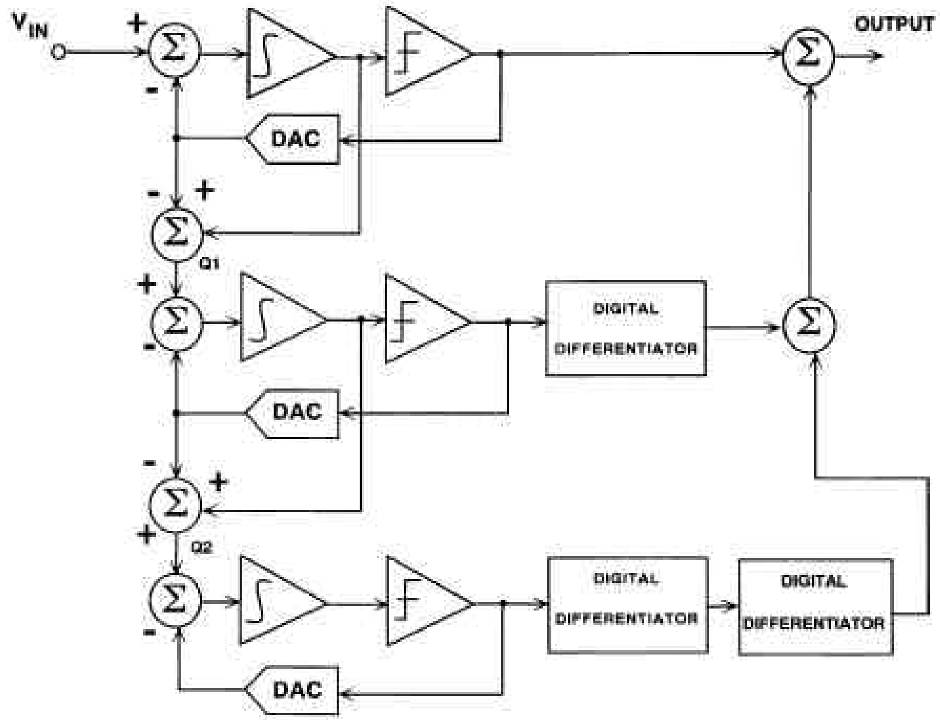


Figure 3.140: *Multi-Stage Noise Shaping Sigma-Delta ADC (MASH)*

Notes

Notes

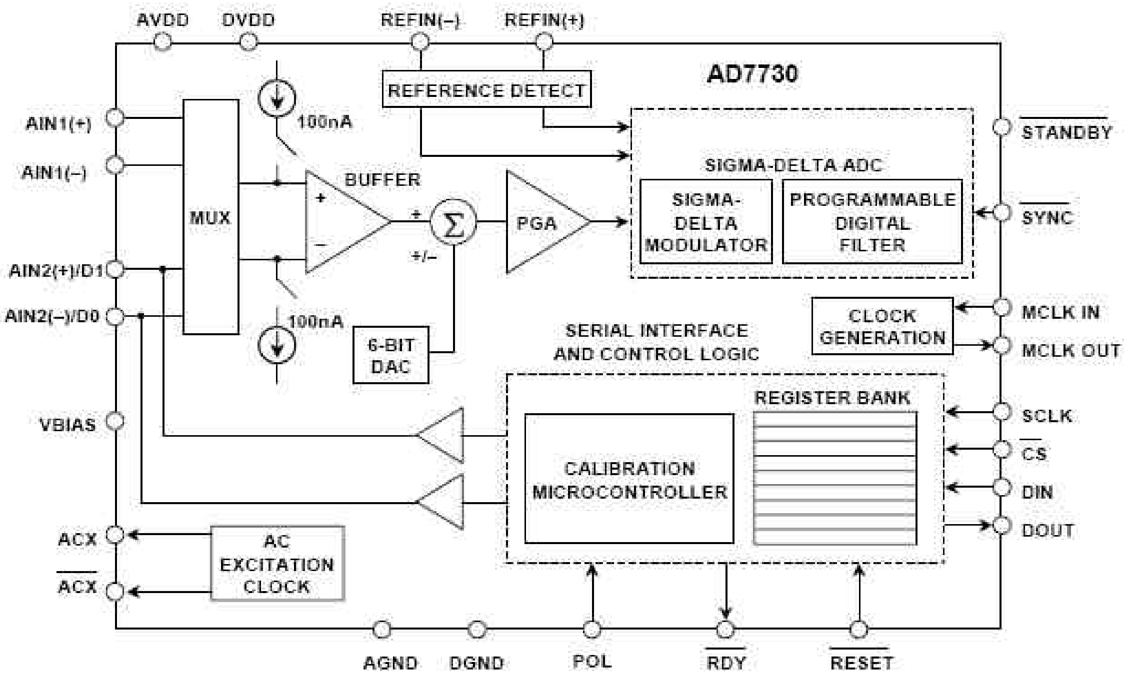


Figure 3.141: *AD7730 Sigma-Delta Single-Supply Bridge ADC*

Notes

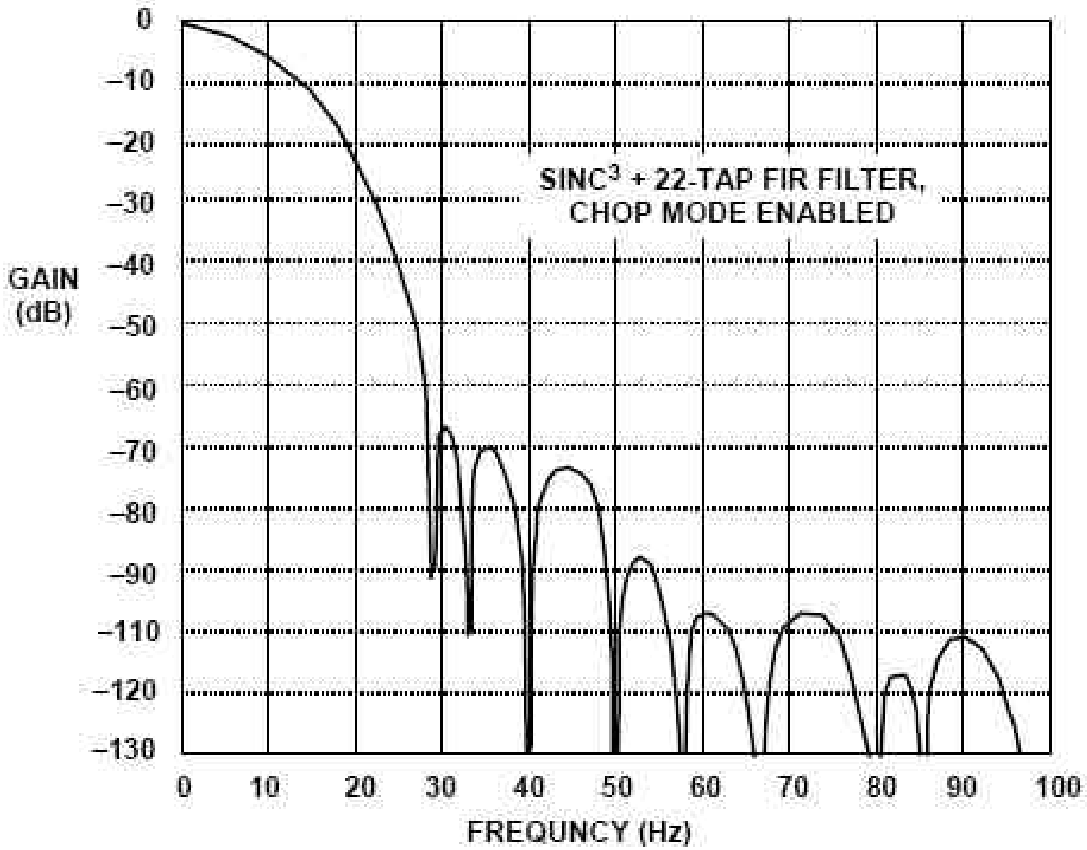


Figure 3.142: *AD7730 Digital Filter Response*

Notes

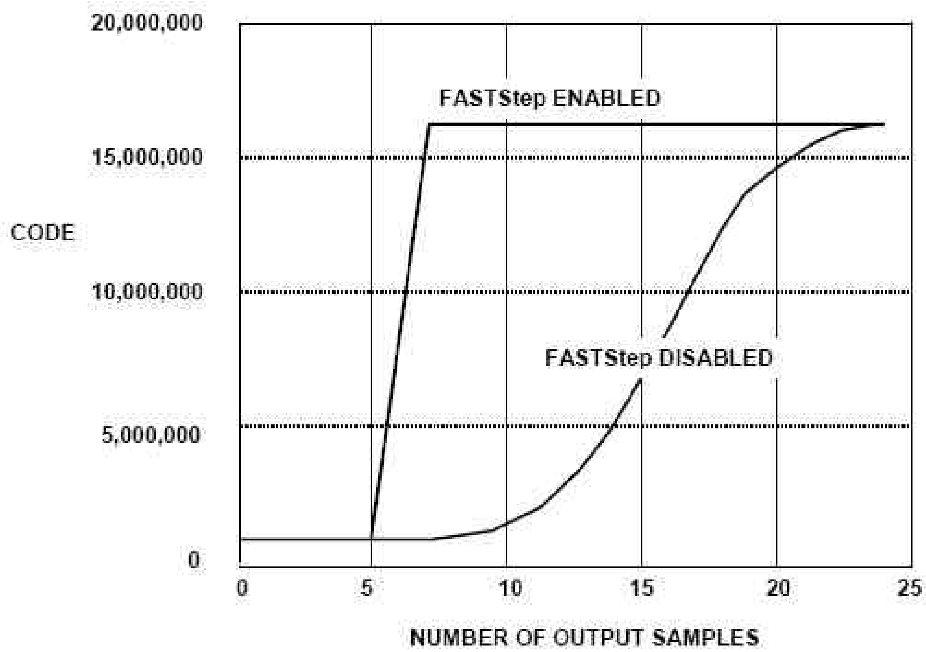


Figure 3.143: *AD7730 Digital Filter Settling Time Showing FASTStep™ Mode*

Notes

- Internal Zero-ScaleCalibration
  - 22 Output Cycles (CHP = 0)
  - 24 Output Cycles (CHP = 1)
- Internal Full-Scale Calibration
  - 44 Output Cycles (CHP = 0)
  - 48 Output Cycles (CHP = 1)
- Calibration Programmed via the Mode Register
- Calibration Coefficients Stored in Calibration Registers
- External Microprocessor Can Read or Write to Calibration Coefficient Registers

Figure 3.144: *AD7730 Calibration Options*

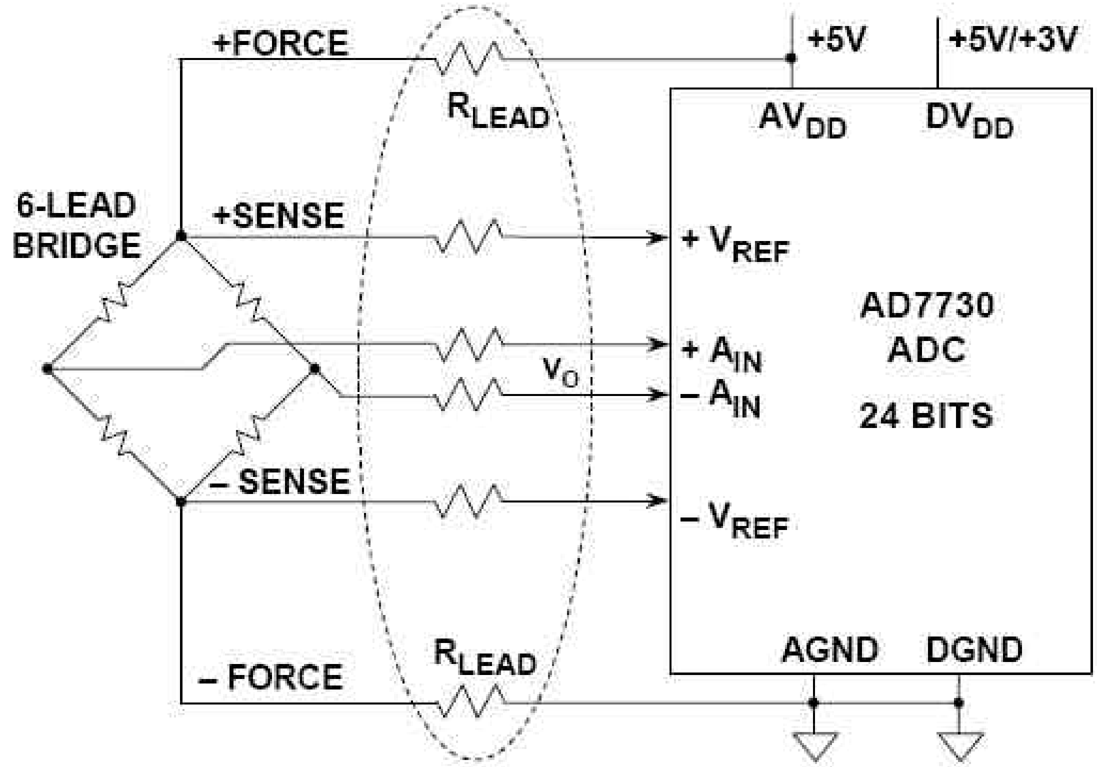


Figure 3.145: *AD7730 Bridge Application (Simplified Schematic)*

Notes

Notes

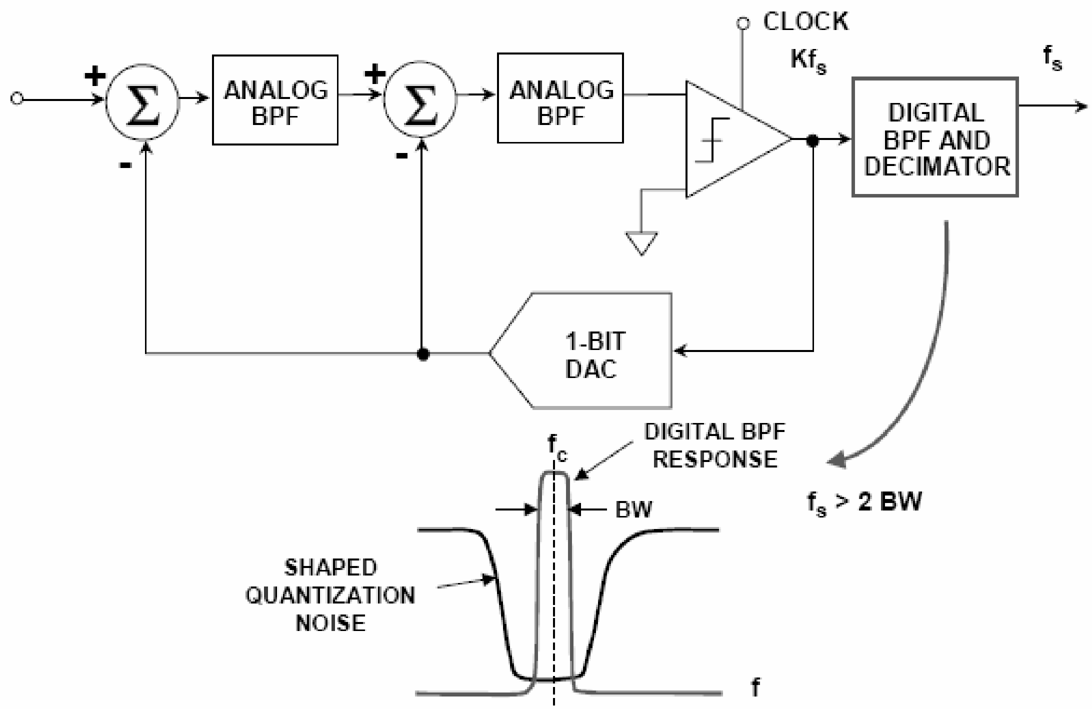


Figure 3.146: *Replacing Integrators with Resonators Gives a Bandpass Sigma-Delta ADC*

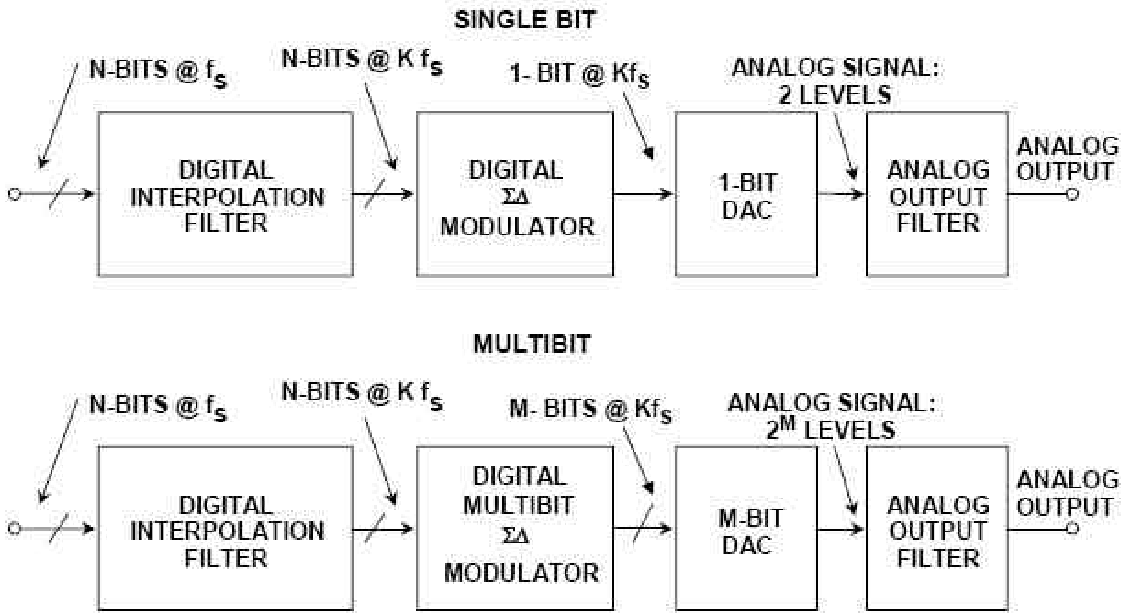


Figure 3.147: *Sigma-Delta DACs*

Notes

Notes

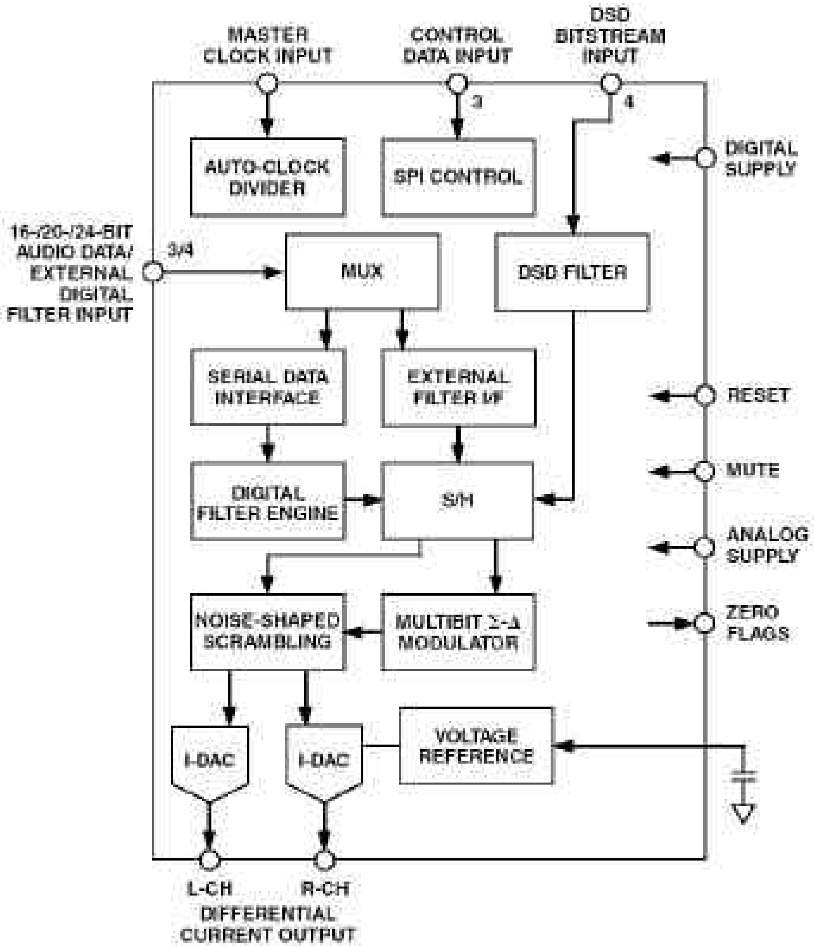


Figure 3.148: *AD1955 Multibit Sigma-Delta Audio DAC*

Notes

- Inherently Excellent Linearity
- High Resolution Possible (24-Bits)
- Oversampling Relaxes Analog Antialiasing Filter Requirements
- Ideal for CMOS Processes, no Trimming
- No SHA Required
- Added Functionality: On-Chip PGAs, Analog Filters, Autocalibration
- On-Chip Programmable Digital Filters (AD7725: Lowpass, Highpass, Bandpass, Bandstop)
- Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio, except for Bandpass Sigma-Delta ADCs
- Analog Multiplexer Switching Speed Limited by Internal Filter Settling Time.

Figure 3.149: *Sigma-Delta Summary*