Notes

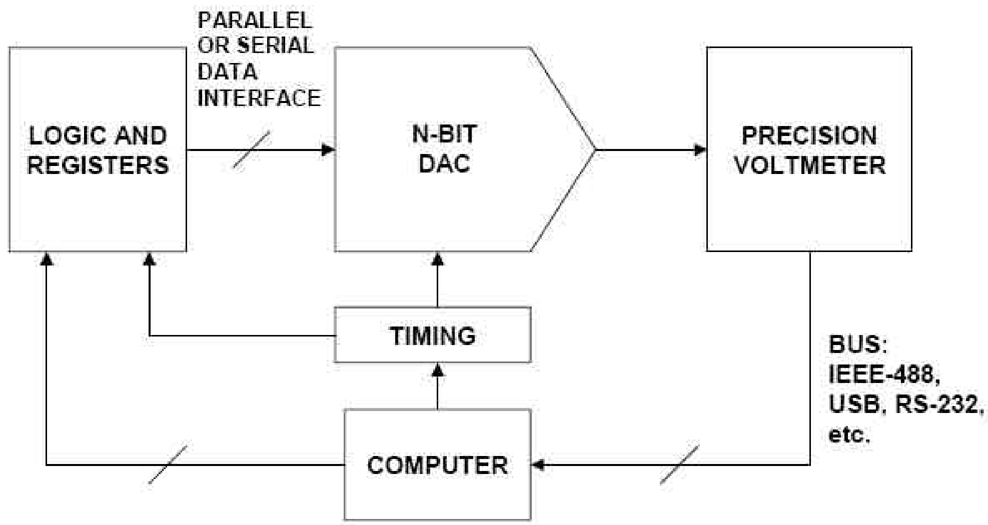


Figure 5.1: *Basic Test Setup for Measuring DAC Static Transfer Characteristics*

Notes

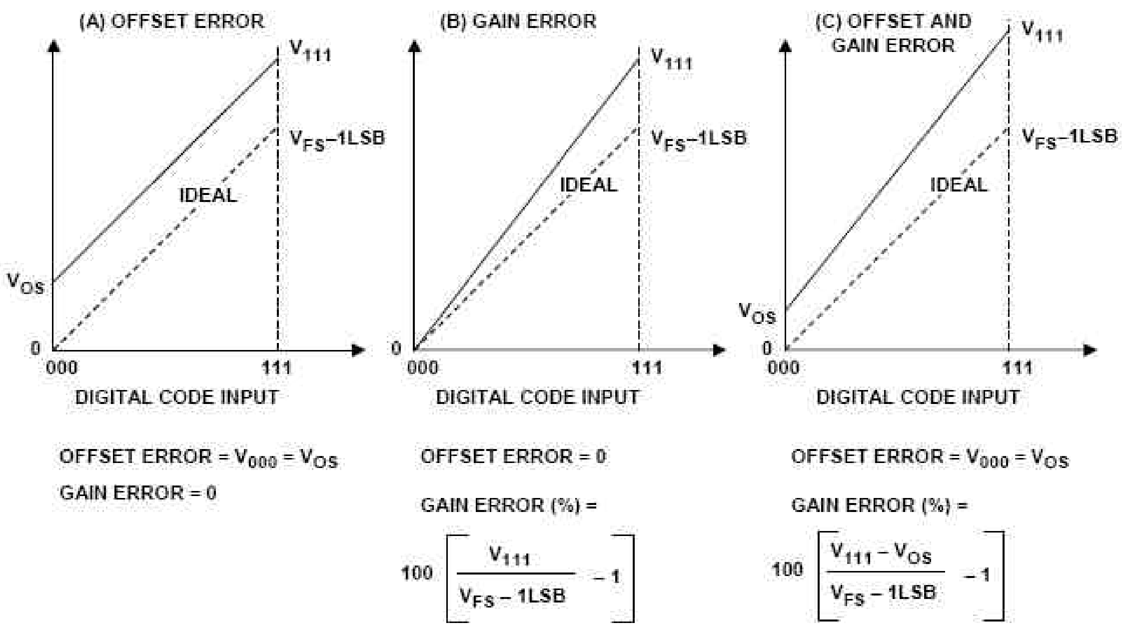


Figure 5.2: *Measuring Offset and Gain Error in a Unipolar DAC*

Notes

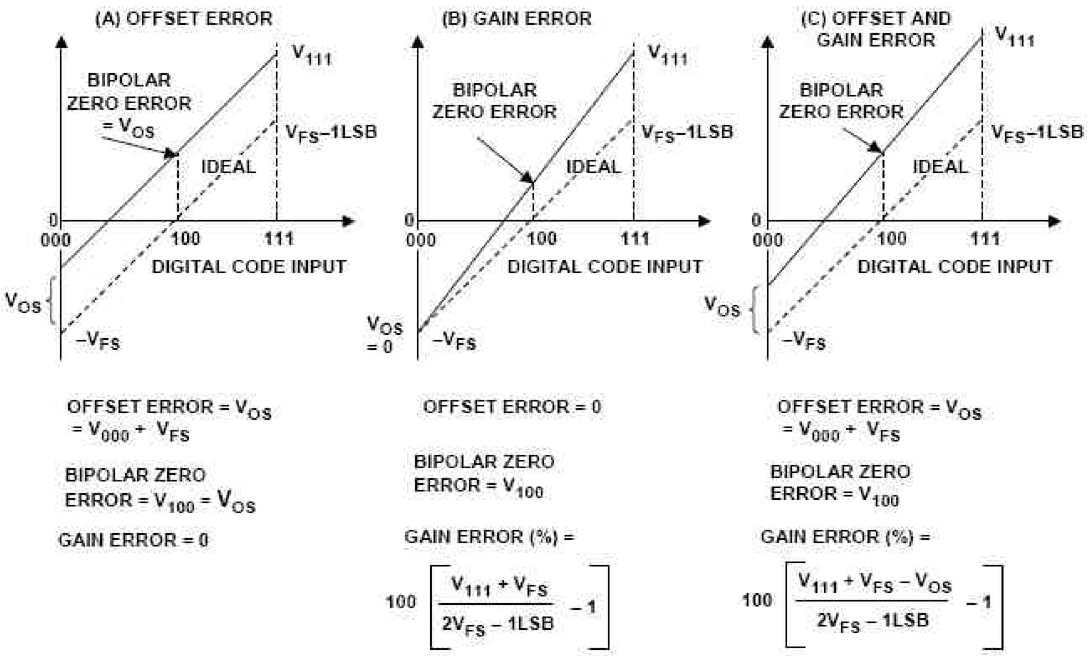


***Figure 5.3:** Measuring Offset, Bipolar Zero, and Gain Error in a Bipolar DAC*

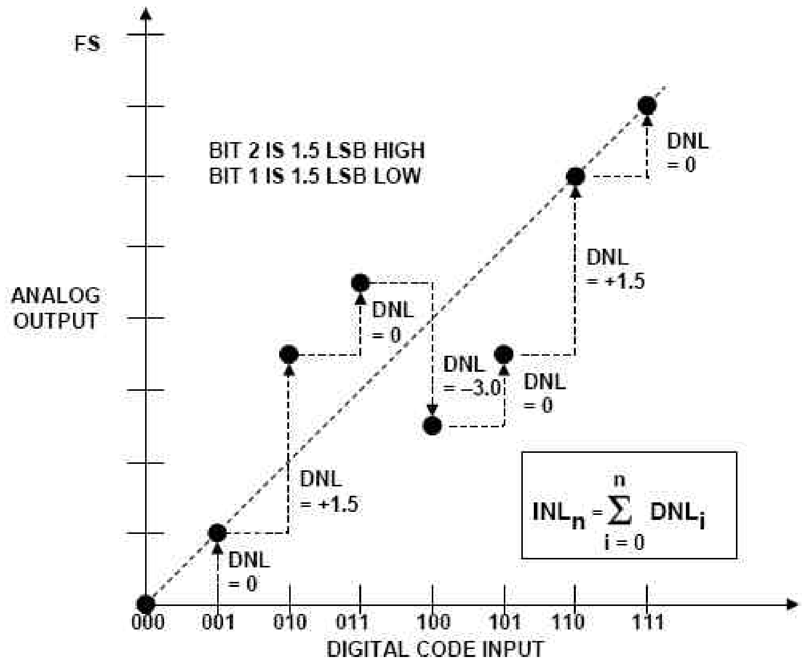


Figure 5.4: *Non-Ideal 3-Bit DAC Transfer Function Where Superposition Holds*

Notes

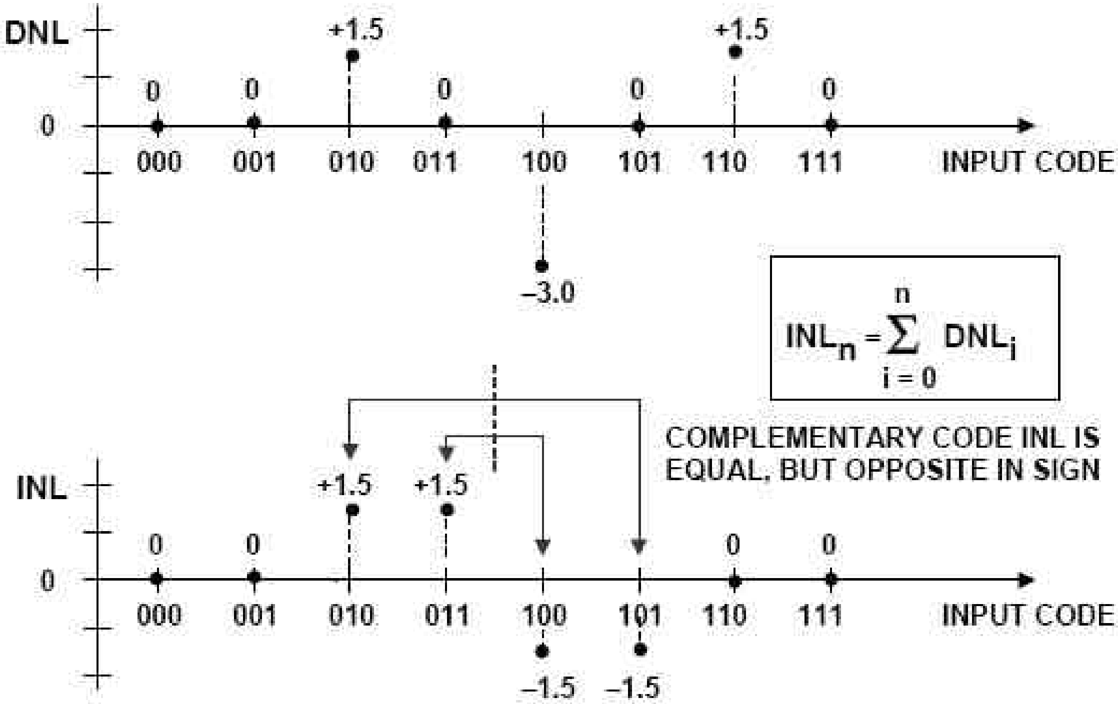


***Figure 5.5:** Differential and Integral Linearity for Non-Ideal 3-Bit Binary-Decoded DAC Where Superposition Holds*

Notes

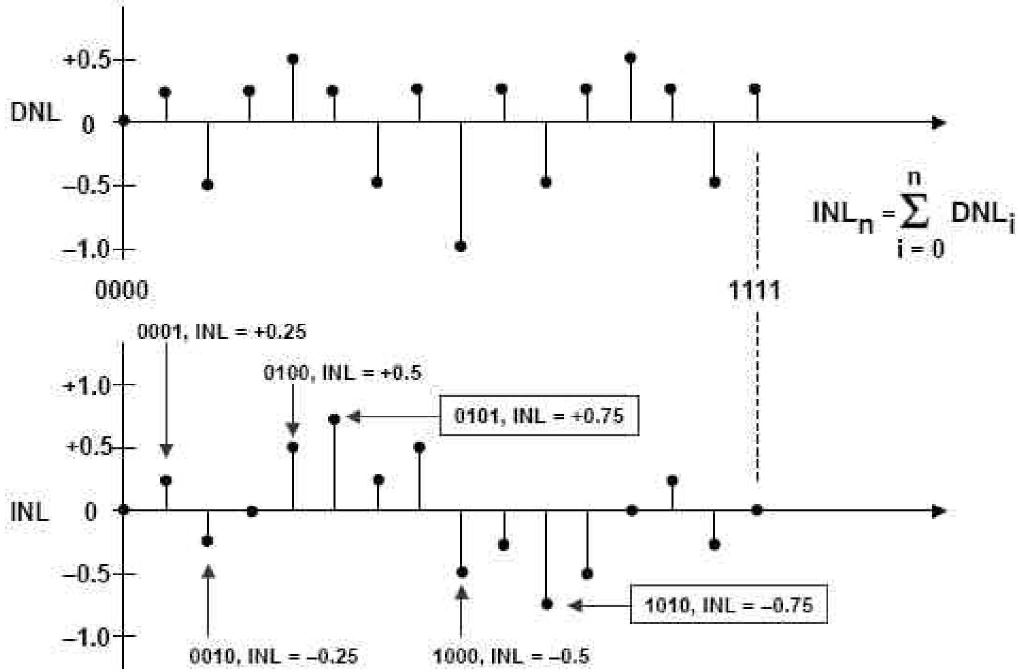


Figure 5.6: *DNL and INL for 4-Bit DAC Where Superposition Holds*

Notes

Figures from Chapter 5: Testing Data Converters in *Analog-Digital Conversion* by Walt Kester, Analog Devices Inc.

Notes

CHECK BIT SUM: $V_{1111} \overset{?}{=} V_{0000} + V_{0001} + V_{0010} + V_{0100} + V_{1000}$

$$1\ \text{LSB} = \frac{V_{1111} - V_{0000}}{15}$$

$1111 = V_{1111}$

BIT ERRORS:

$1000 = V_{1000}$, $0111 = V_{0111}$: $DNL4 = V_{1000} - V_{0111} - 1\ \text{LSB}$

$0100 = V_{0100}$, $0011 = V_{0011}$: $DNL3 = V_{0100} - V_{0011} - 1\ \text{LSB}$

$0010 = V_{0010}$, $0001 = V_{0001}$: $DNL2 = V_{0010} - V_{0001} - 1\ \text{LSB}$

$0001 = V_{0001}$, $0000 = V_{0000}$: $DNL1 = V_{0001} - V_{0000} - 1\ \text{LSB}$

$V_{OS} = V_{0000}$

Figure 5.7: *Major-Carry Bit Tests for 4-Bit Binary-Decoded DAC Where Superposition Holds*

Notes

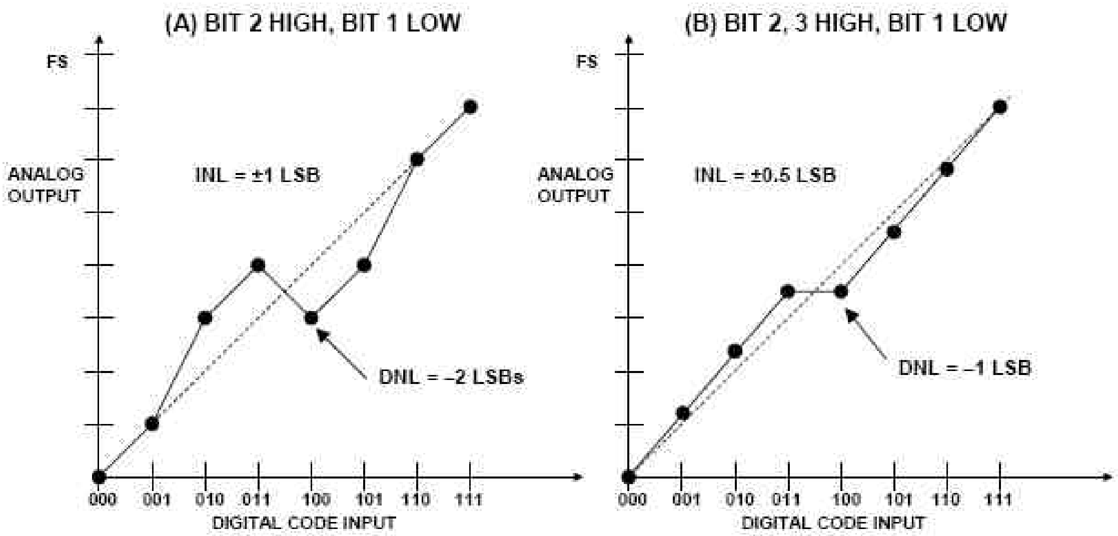


Figure 5.8: *Linearity Errors in Binary-Decoded 3-Bit DACs Where Superposition Holds*

Notes

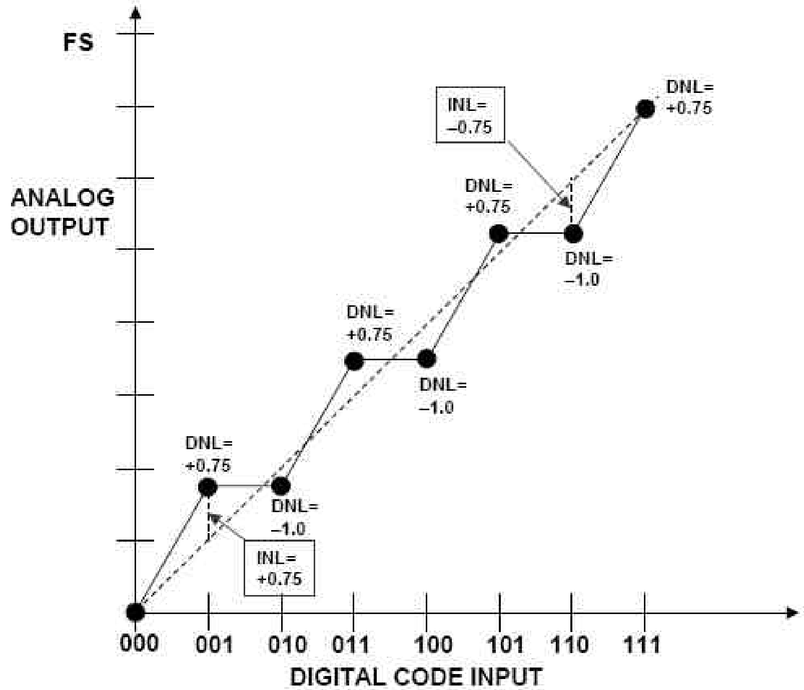


Figure 5.9: *DNL Specification of < ±1 LSB Does Not Guarantee INL < ±0.5 LSB*

Notes

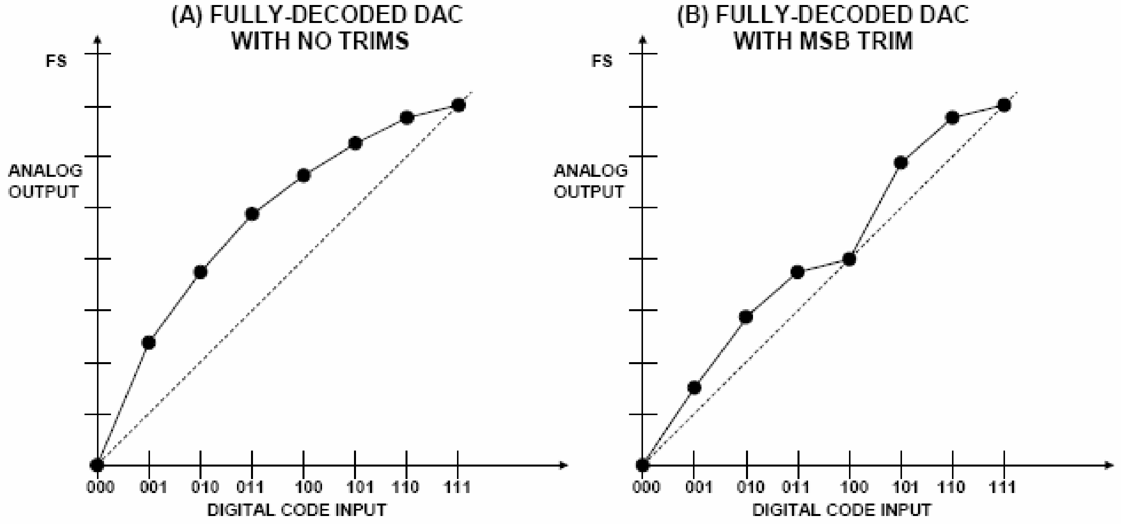


Figure 5.10: *INL of Fully-Decoded 3-Bit DACs (String DACs)*

Notes

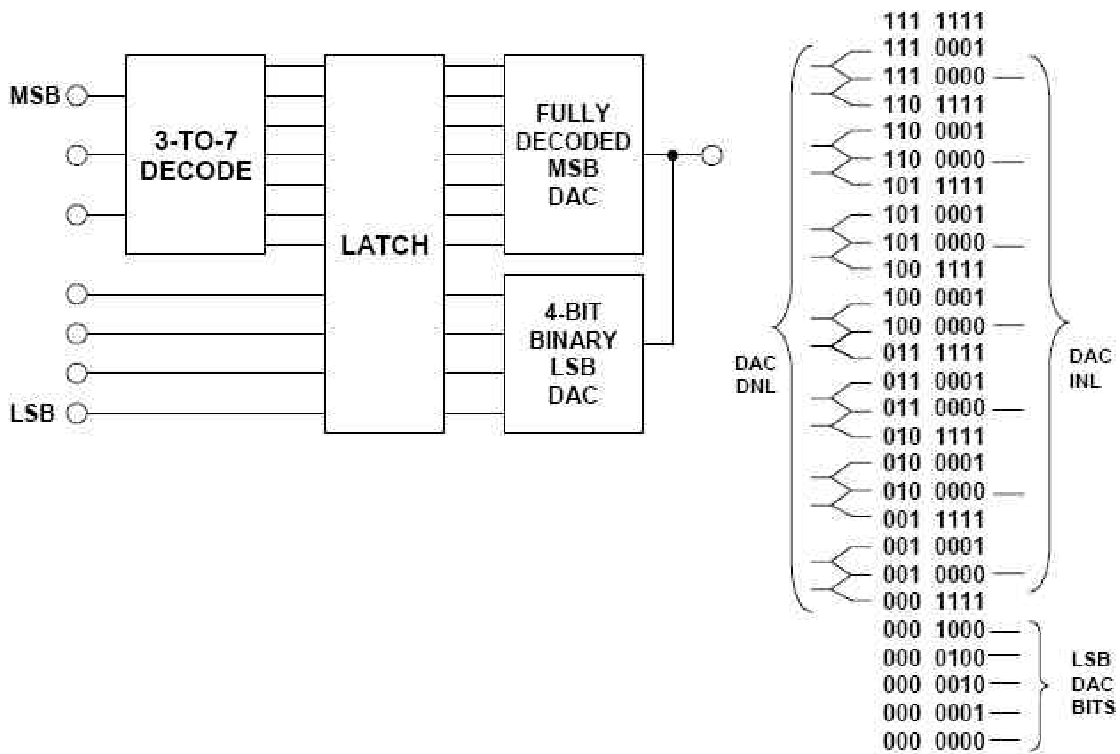


Figure 5.11: *3-Bit×4-Bit Segmented 7-Bit DAC Test Codes*

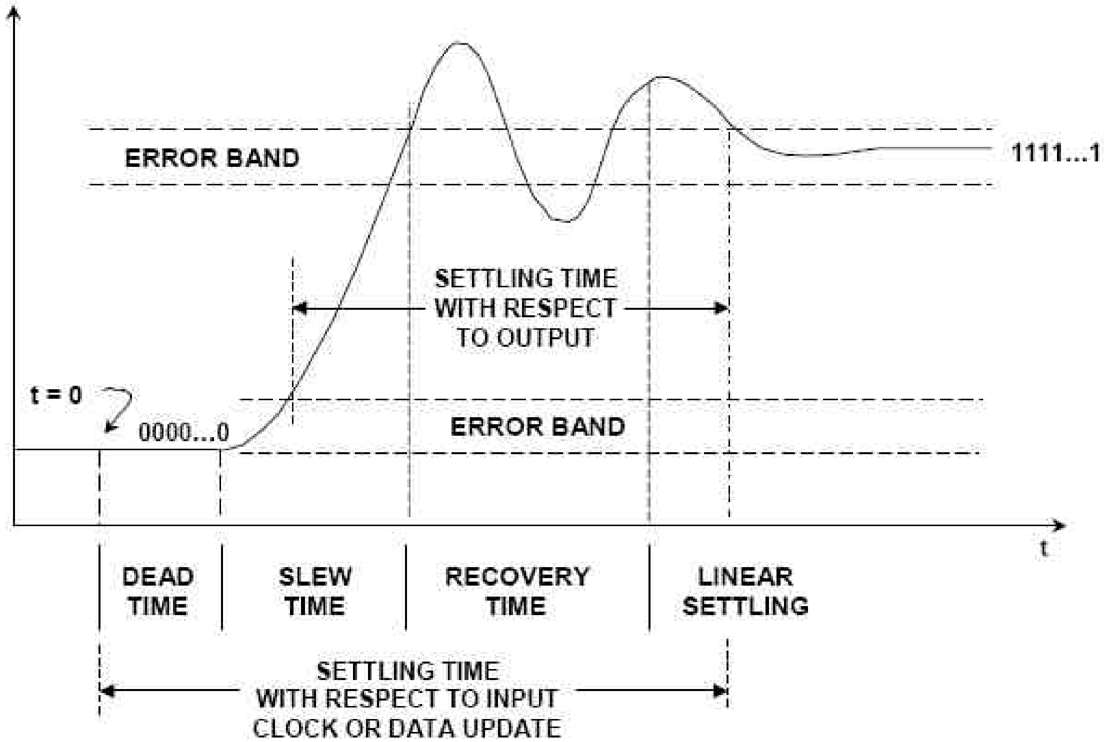


Figure 5.12: *DAC Full-Scale Settling Time Measurement*

Notes

Notes

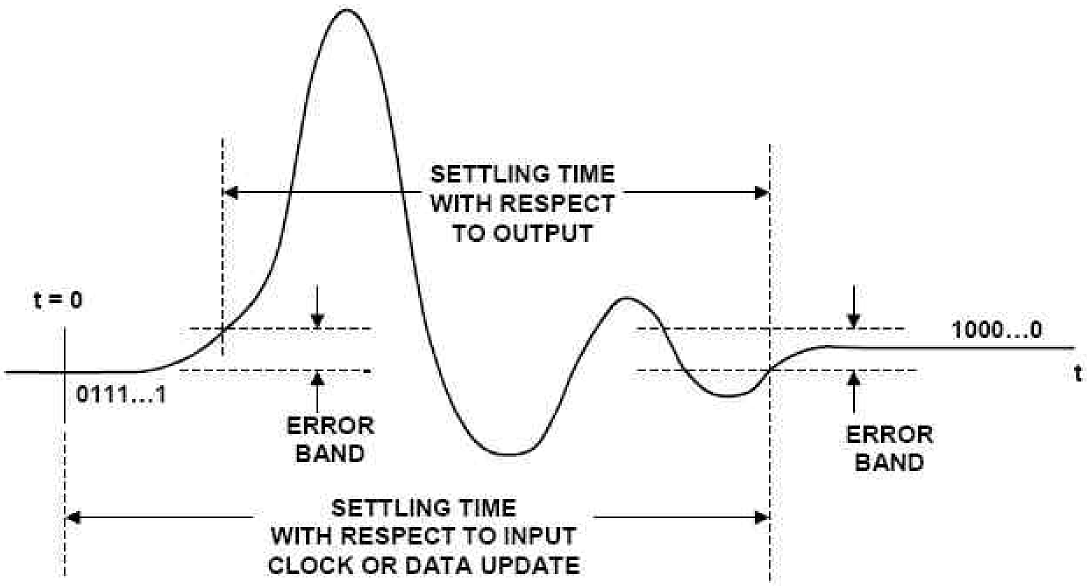


Figure 5.13: *DAC Mid-Scale Settling Time Measurement*

Notes

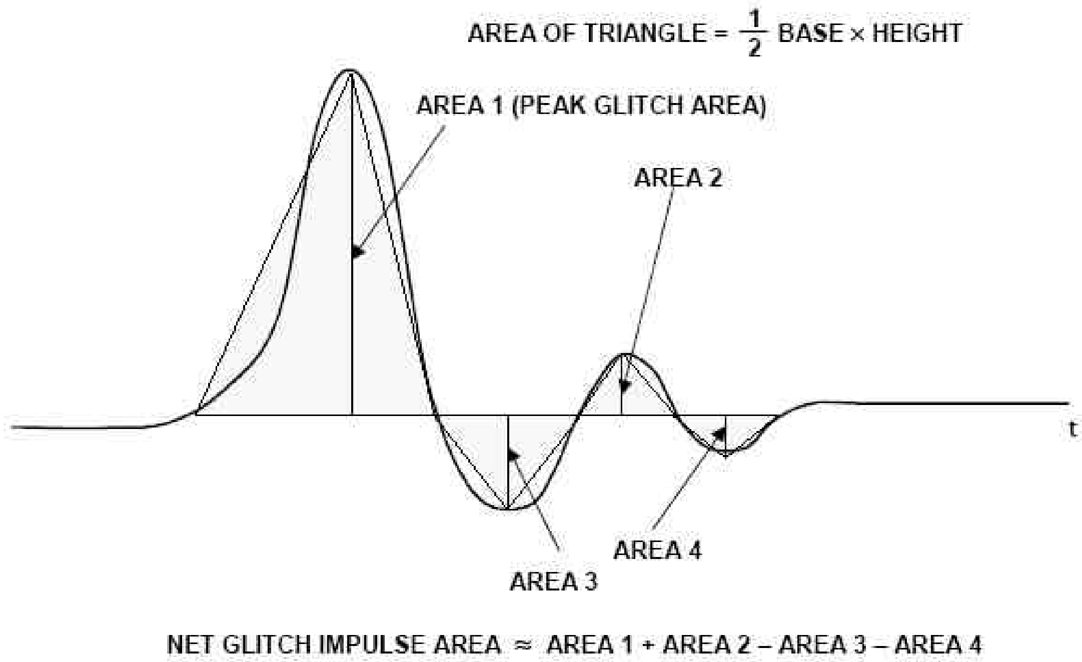


Figure 5.14: *Glitch Impulse Area Measurement*

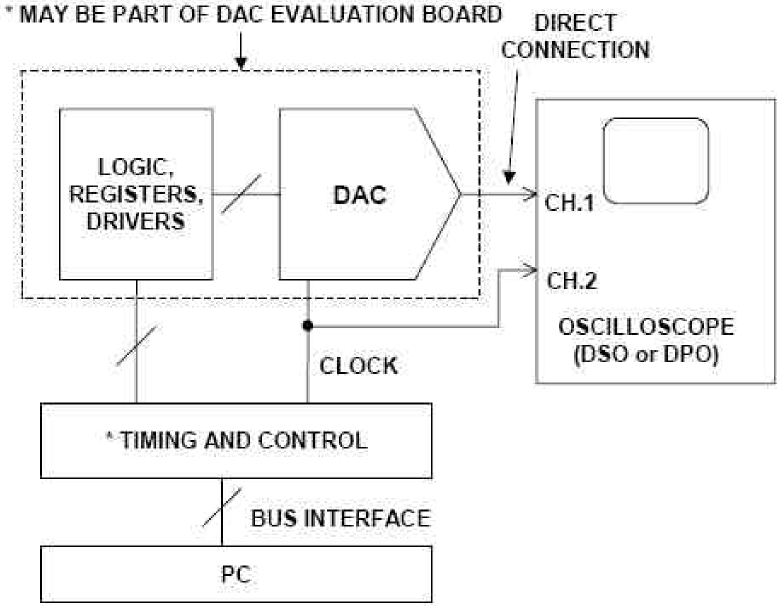


***Figure 5.15:** Test Setup for Measuring Settling Time and Glitch Impulse Area*

Notes

Notes

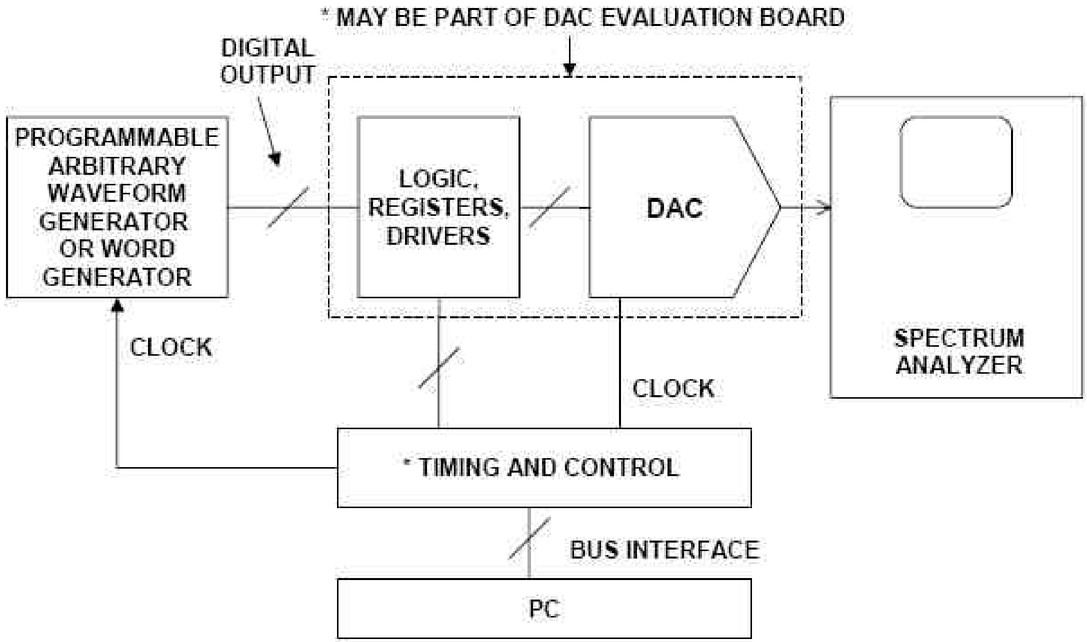


Figure 5.16: *Test Setup for Measuring DAC Distortion and Noise*

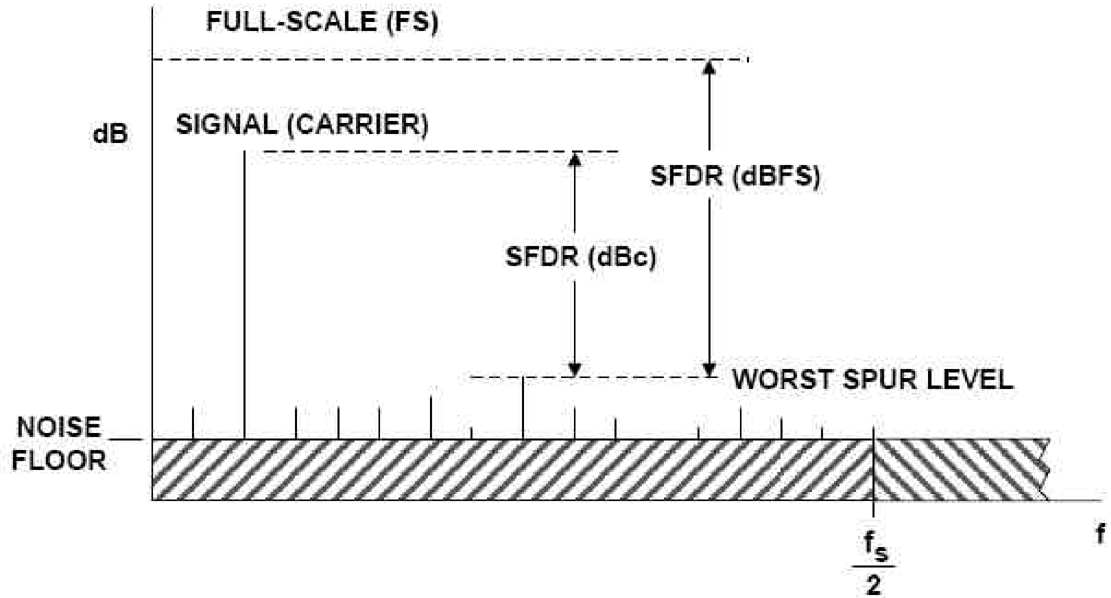
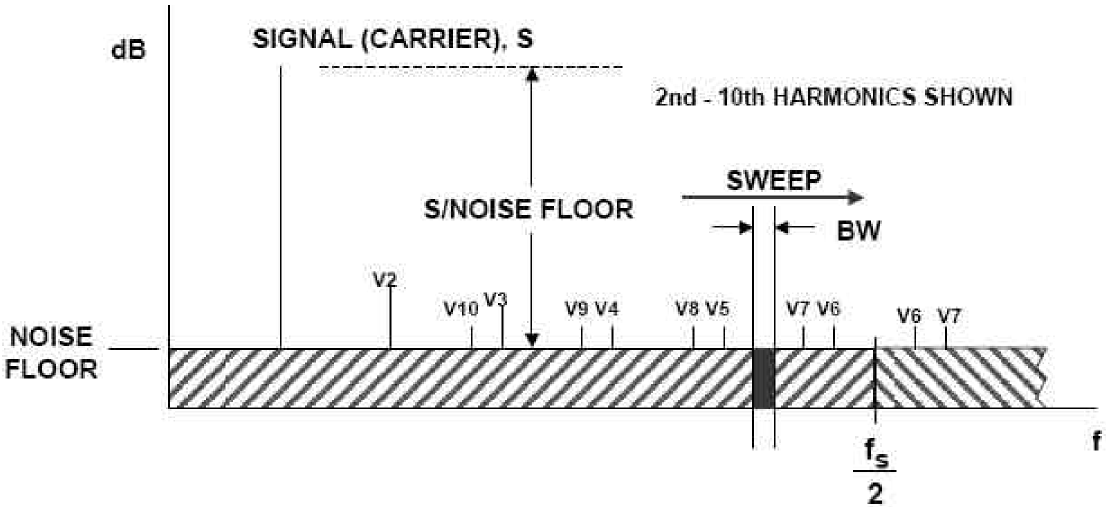


Figure 5.17: *Measuring DAC Spurious Free Dynamic Range (SFDR)*

Notes

Notes



- BW = ANALYZER RESOLUTION BANDWIDTH
- $SNR = S/NOISE\ FLOOR - 10 \log_{10}\left[\frac{f_s/2}{BW}\right]$

Figure 5.18: *Measuring DAC Distortion and SNR with an Analog Spectrum Analyzer*

Notes

- $$\text{SNR} = \text{S/NOISE FLOOR} - 10\log_{10}\left[\frac{f_s/2}{\text{BW}}\right]$$

- $$\text{THD} = 20\log_{10}\sqrt{\left[10^{-V2/20}\right]^2 + \left[10^{-V3/20}\right]^2 + \cdots + \left[10^{-V6/20}\right]^2}$$

- $$\text{SINAD} = 20\log_{10}\sqrt{\left[10^{-\text{SNR}/20}\right]^2 + \left[10^{-\text{THD}/20}\right]^2}$$

NOTE: NOISE FLOOR, SNR, THD, SINAD, V2, V3, … , V6 in units of dBc

Figure 5.19: *Calculating S/(N+D) (SINAD) from SNR and THD*

Notes

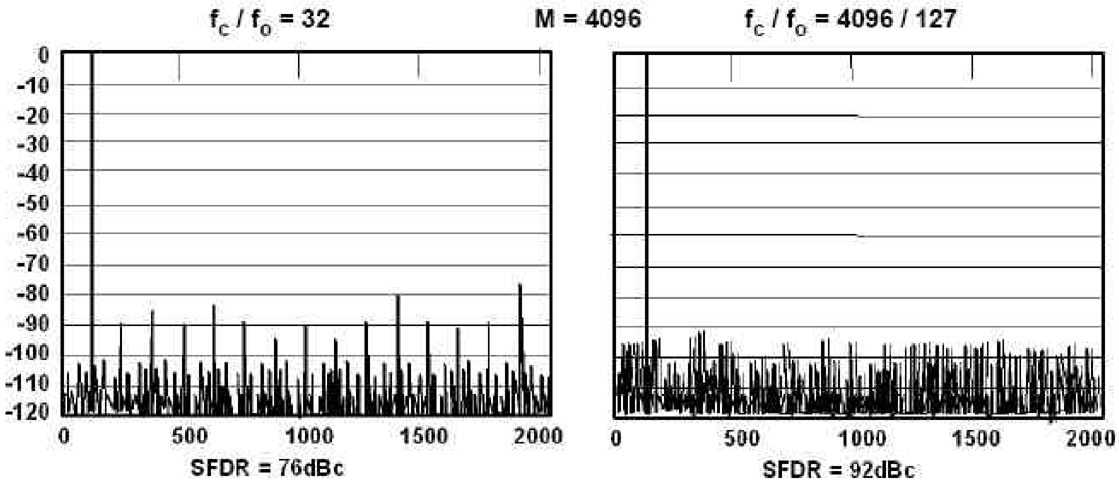


***Figure 5.20:** Effect of Ratio of Sampling Clock f_c to Output Frequency f_o on SFDR for Ideal 12-bit DAC*

Notes

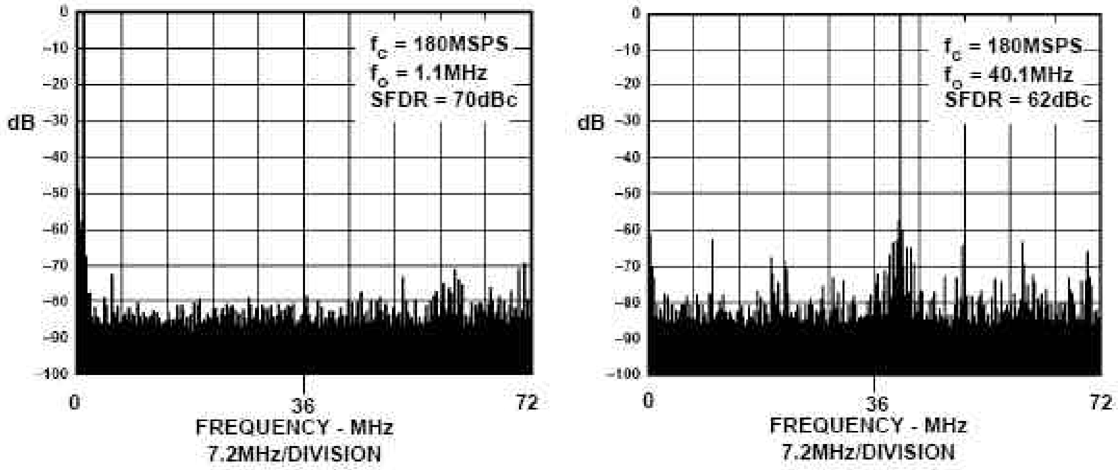


Figure 5.21: *AD9851 10-Bit, 180-MSPS DDS Spectral Output*

Notes

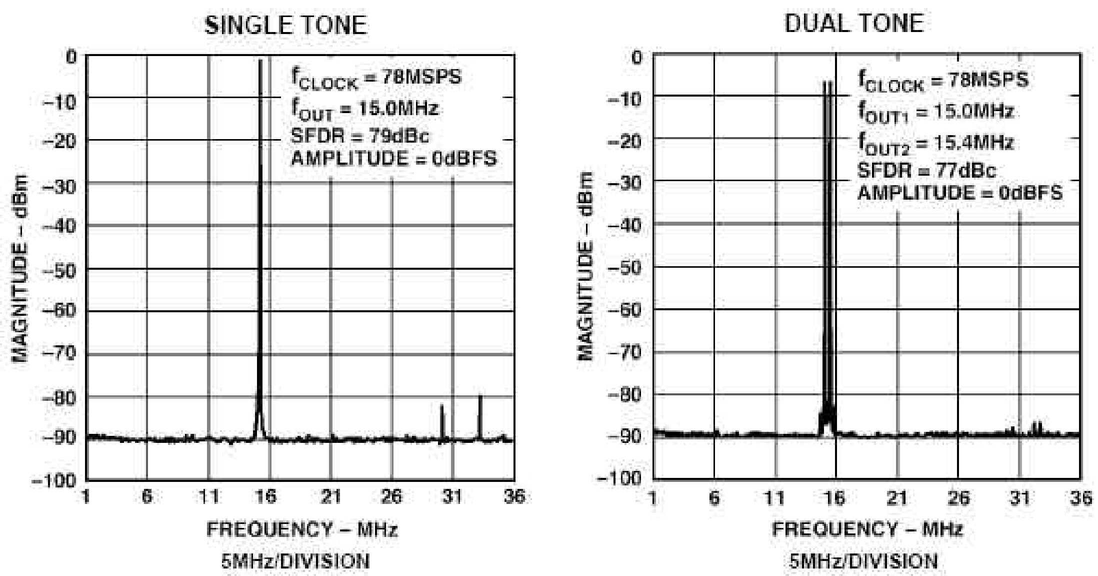


Figure 5.22: *AD9744, 14-Bit, 165-MSPS TxDAC® Spectral Output*

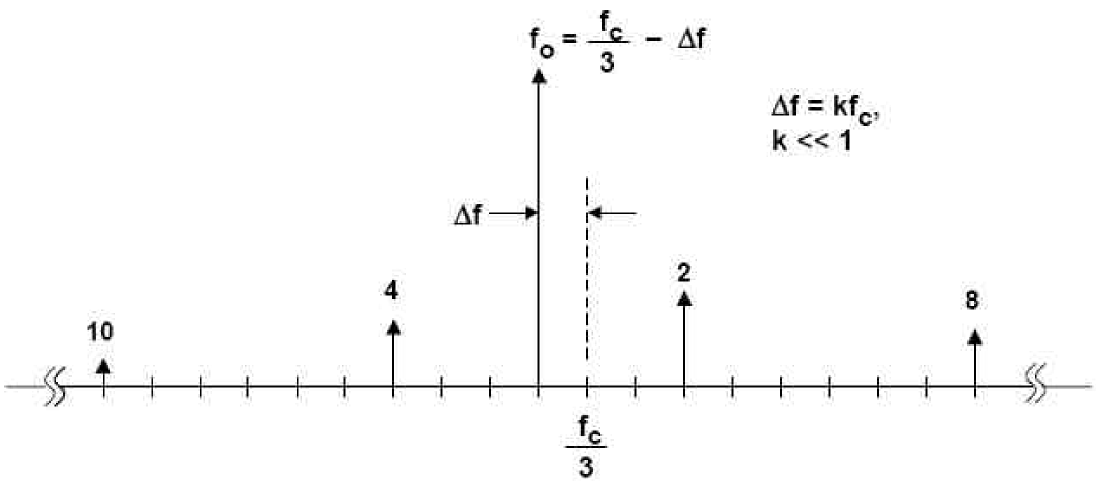


Figure 5.23: *Location of Even Harmonics for* $f_o = f_c/3 - \Delta f$

Notes

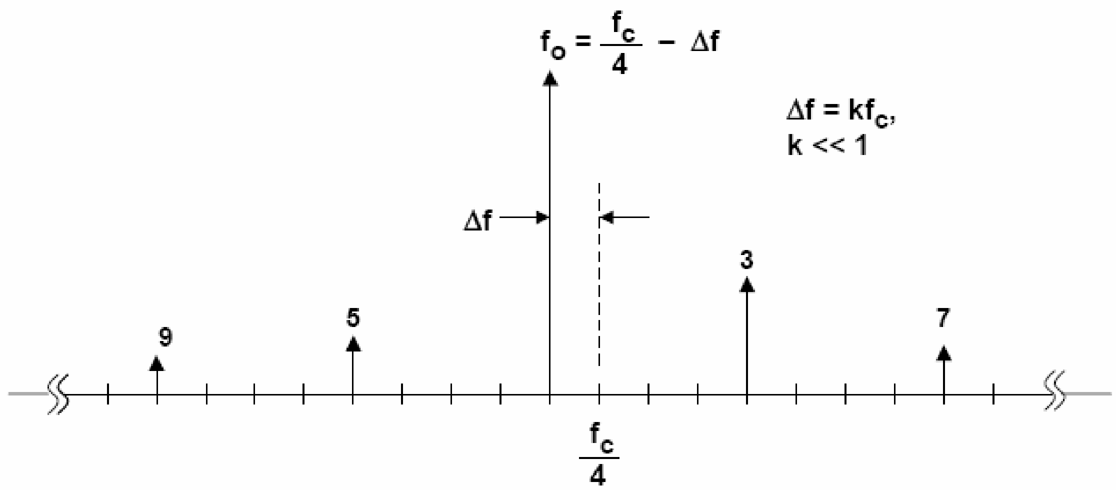


Figure 5.24: *Location of Odd Harmonics for* $f_o = f_c/4 - \Delta f$

Notes

Figures from Chapter 5: Testing Data Converters in *Analog-Digital Conversion* by Walt Kester, Analog Devices Inc.

Notes

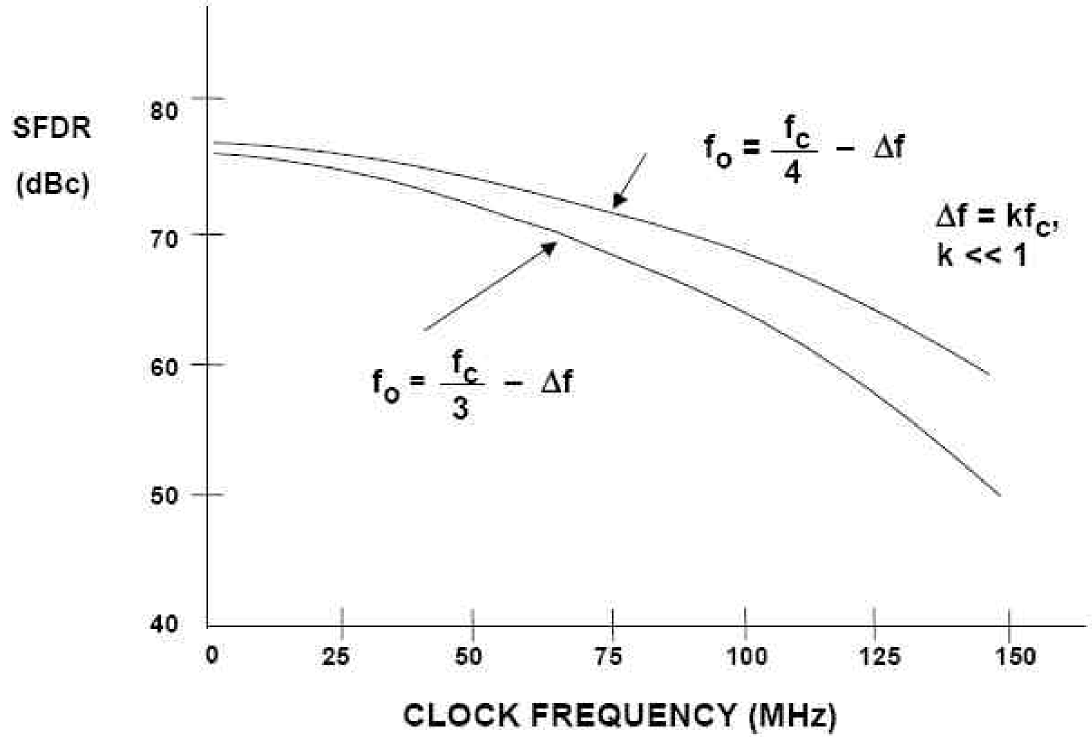


Figure 5.25: *Worst Harmonic vs. Clock Frequency for* $f_o = f_c/3 - \Delta f$ *and* $f_o = f_c/4 - \Delta f$

Notes

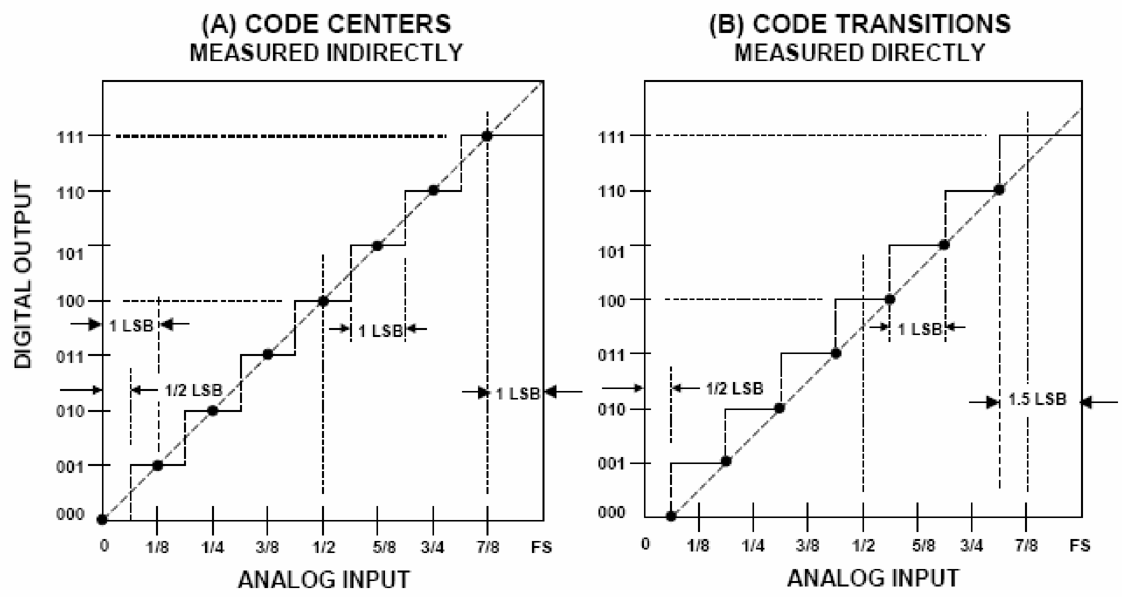


Figure 5.26: *Measuring ADC Code Transistions to Determine Code Centers*

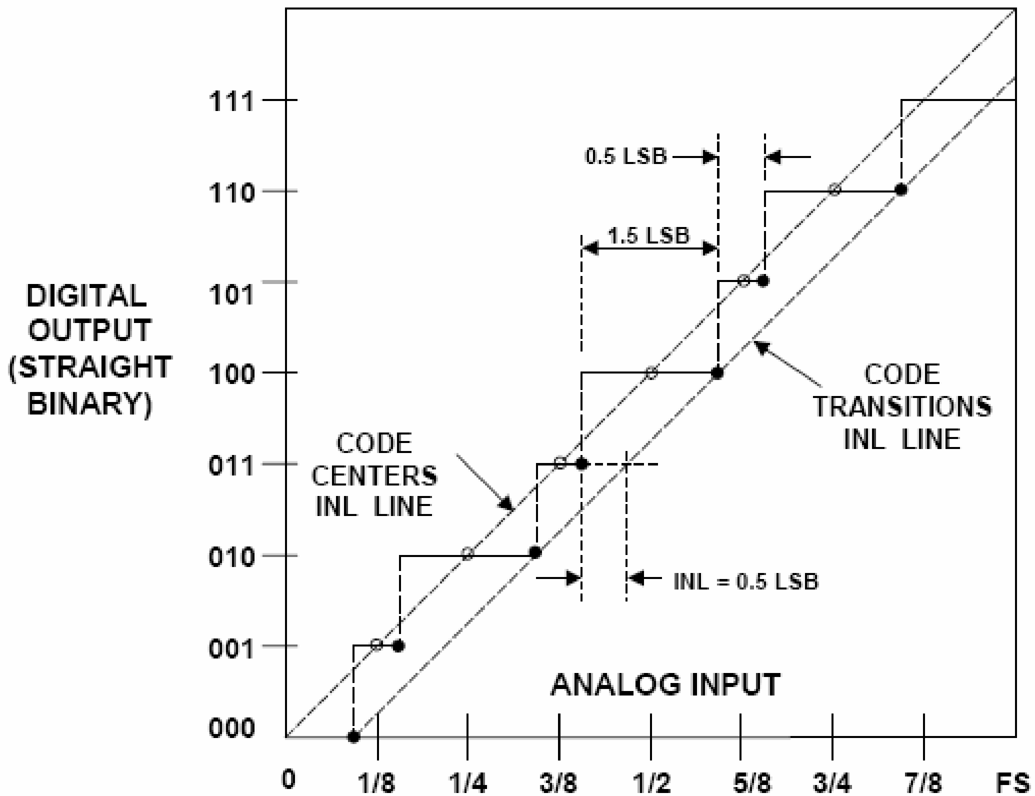


Figure 5.27: *Code Transitions Preferable to Code Centers for Measuring ADC DNL and INL*

Notes

Notes

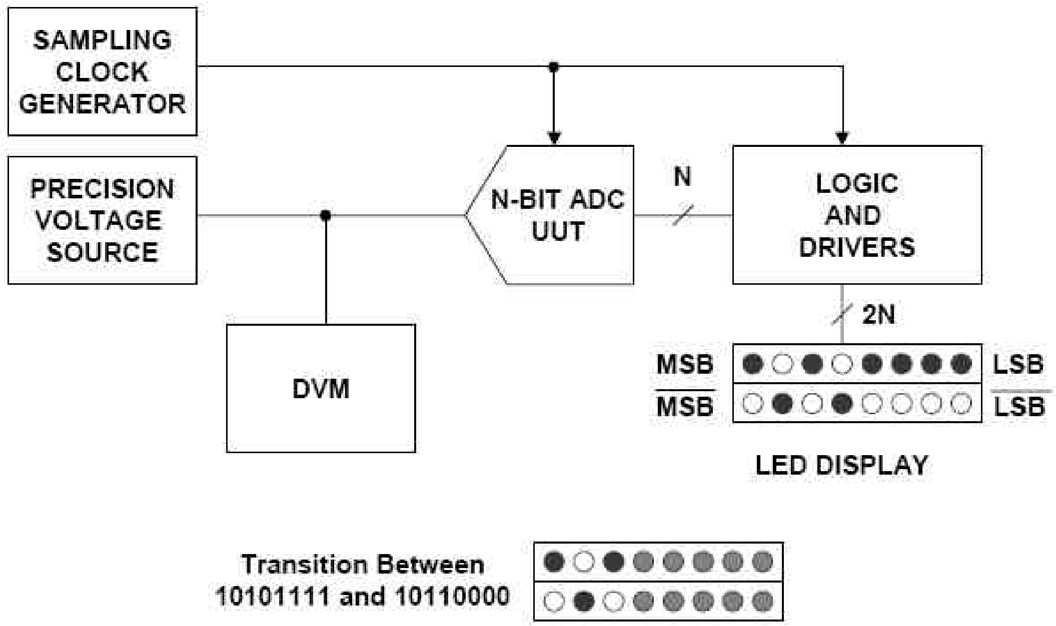


Figure 5.28: *Simple Test Setup for Measuring ADC Code Transitions*

Notes

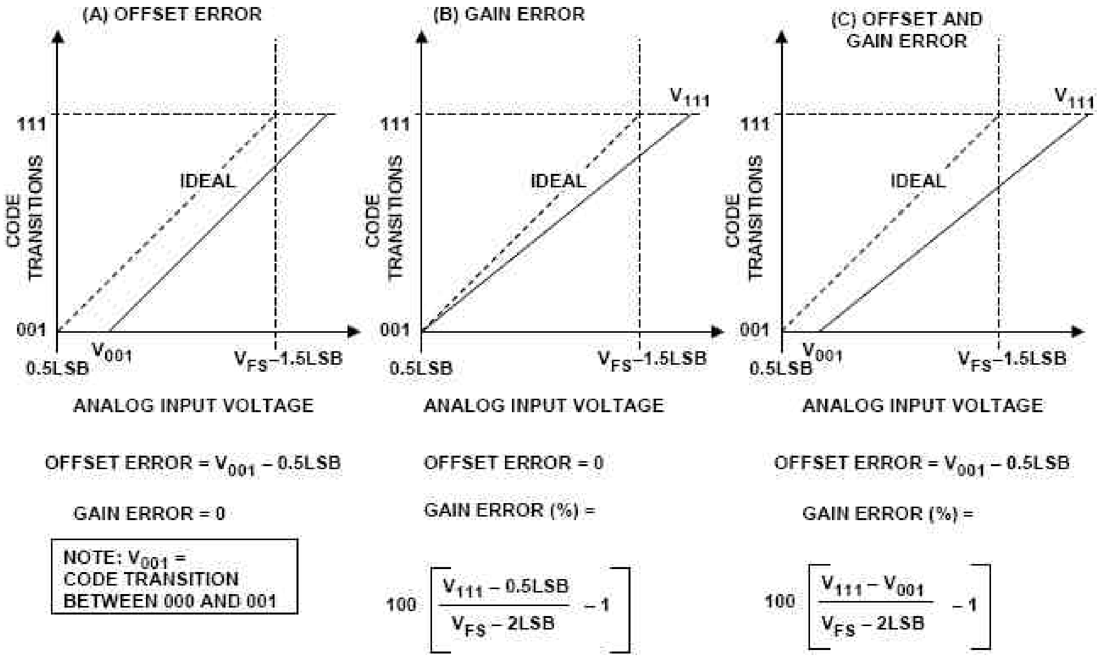


Figure 5.29: *Measuring ADC Offset and Gain Error*

Notes

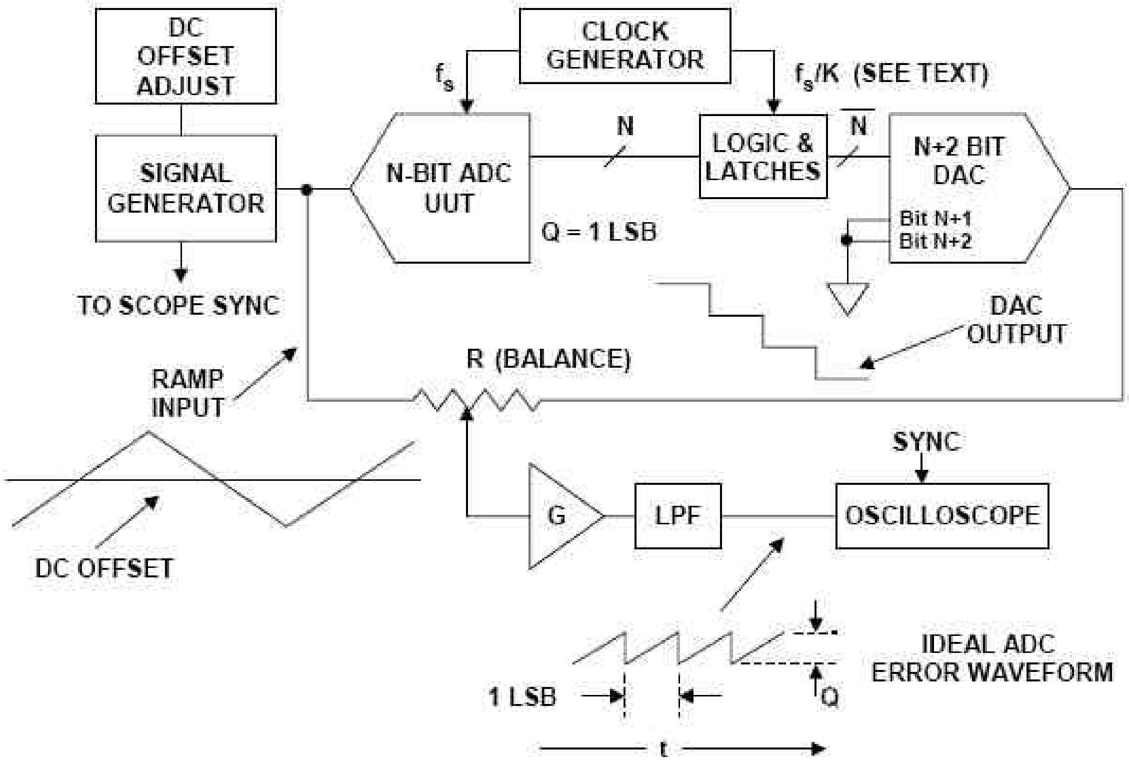


Figure 5.30: *ADC/DAC Back-to-Back Static Testing*

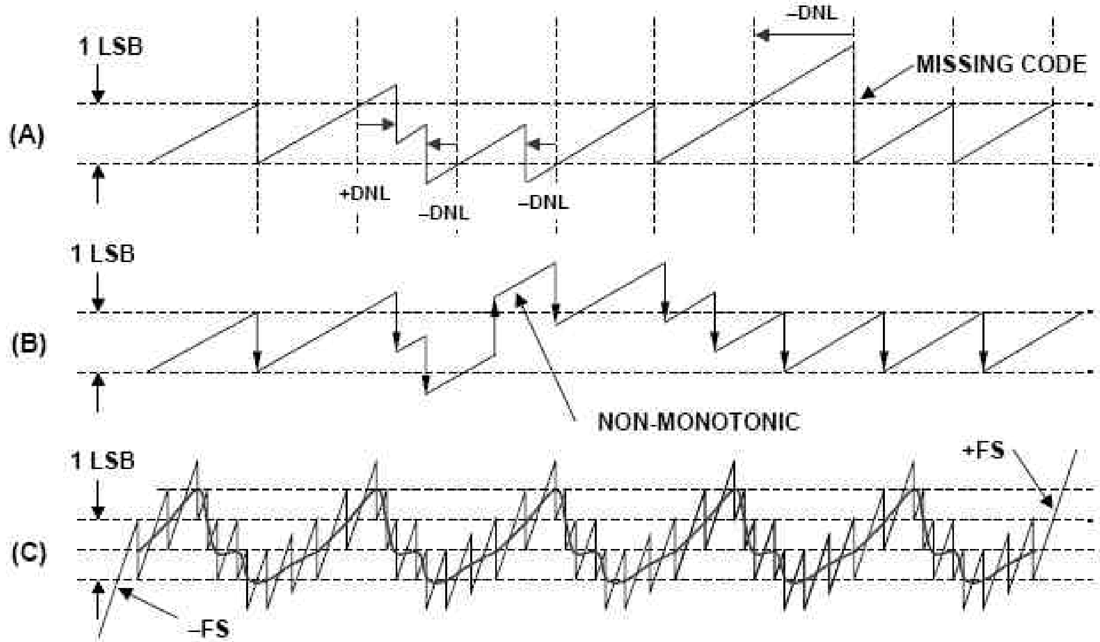


Figure 5.31: *ADC Error Waveforms Using "Back-to-Back" Test Setup*

Notes

Notes

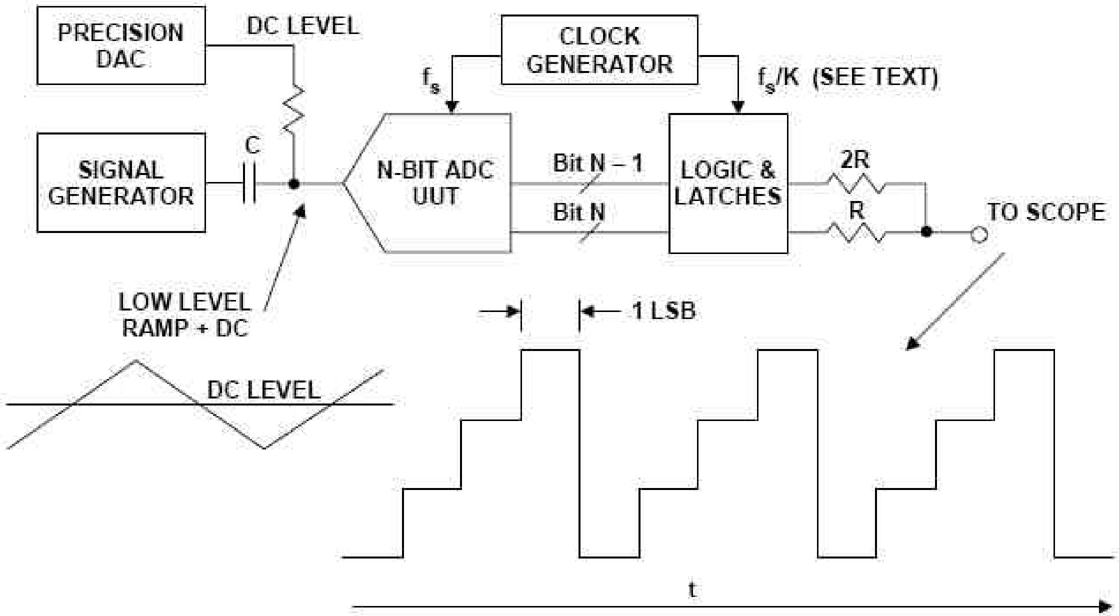


Figure 5.32: ADC Crossplot Test

Notes

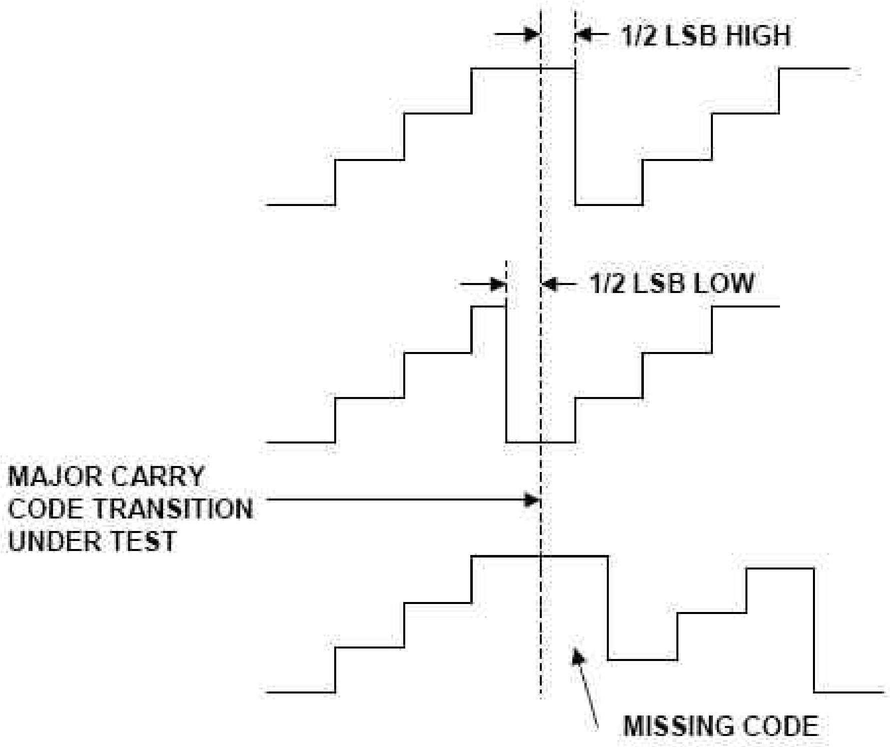


Figure 5.33: *Crossplot Waveforms Showing ADC Static Errors Around Major Code Transitions*

Notes

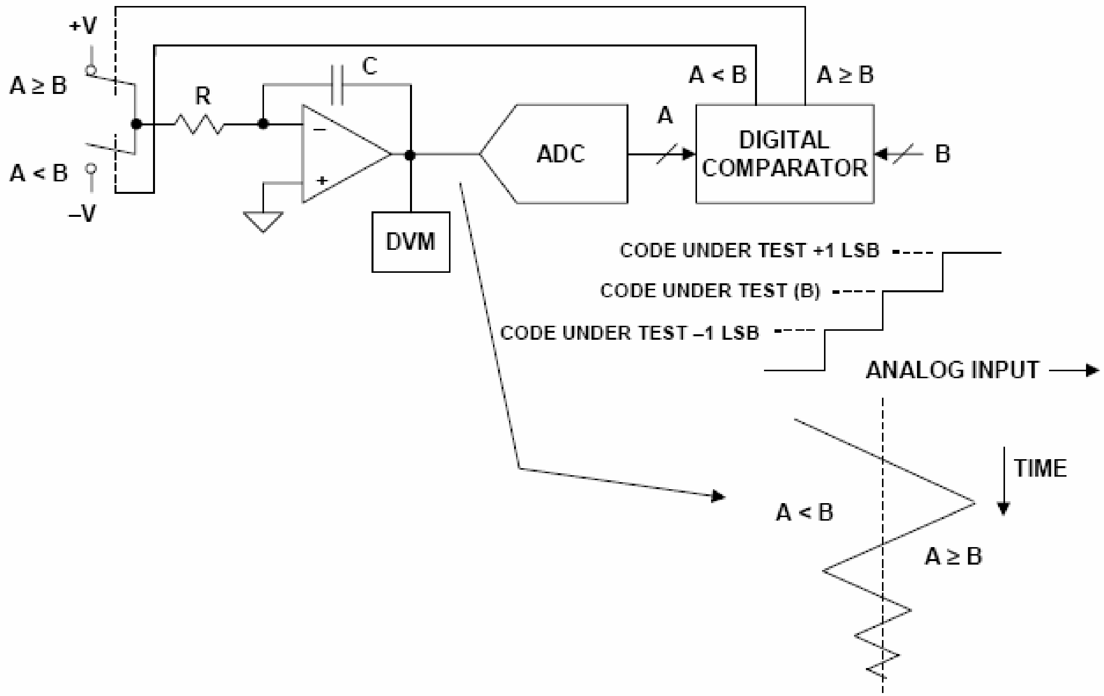


Figure 5.34: *Integrating Servo-Loop ADC Tester*

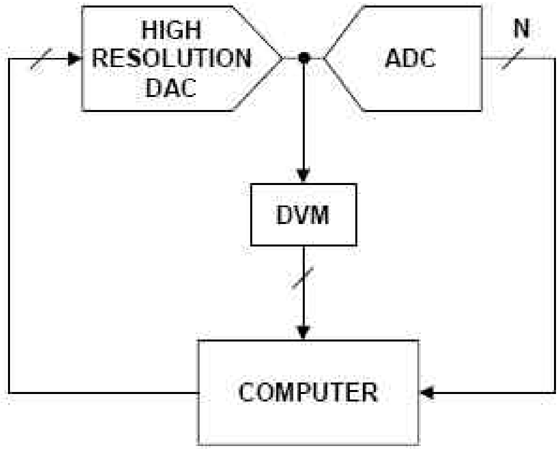


Figure 5.35: *Generalized Computer Controlled Servo-Loop ADC Tester*

Notes

Notes

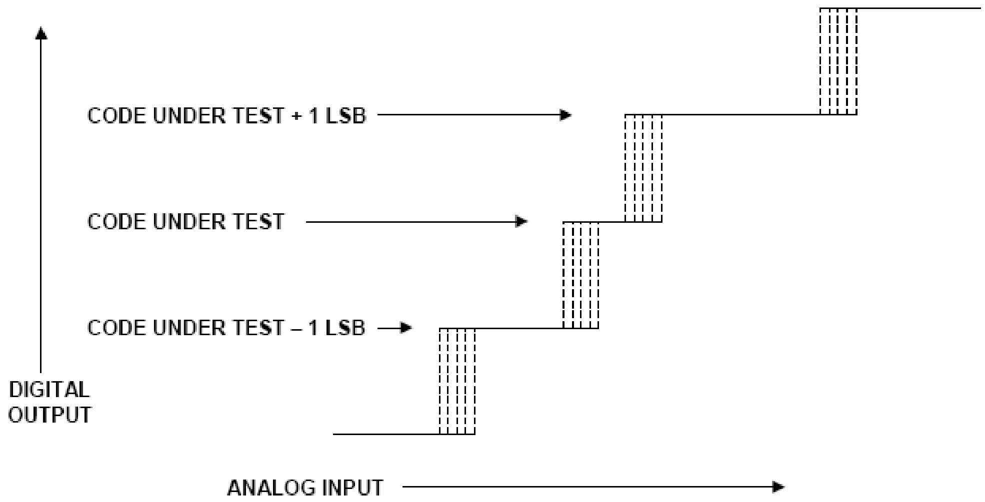


Figure 5.36: *ADC Transfer Function With Relatively Low Input-Referred Noise*

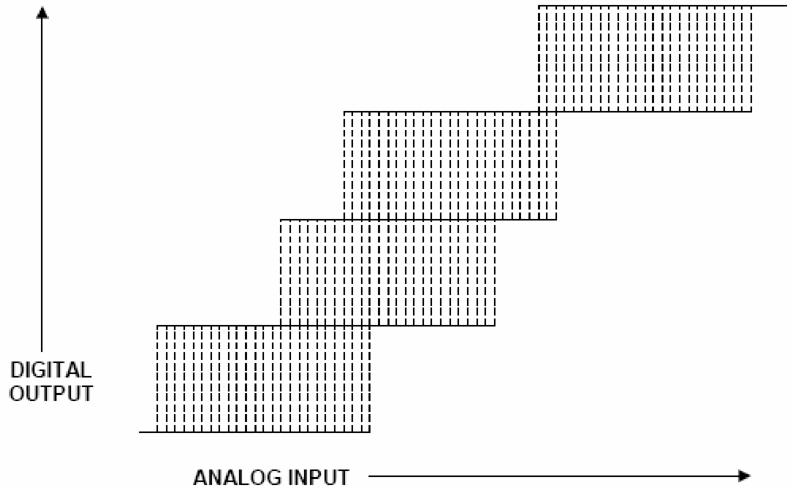
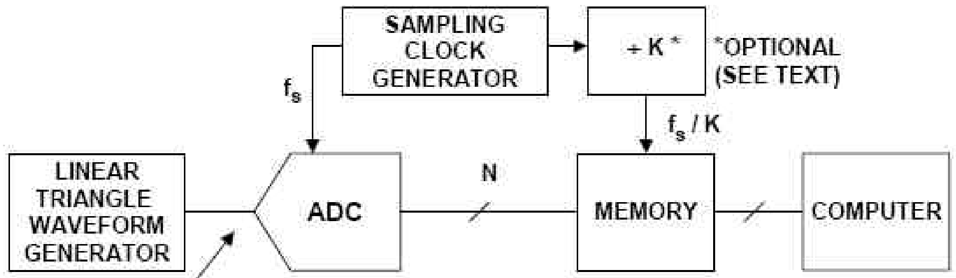
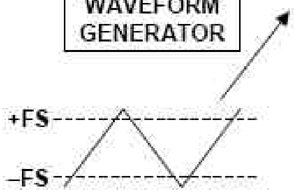


Figure 5.37: *ADC Transfer Function With Relatively High Input-Referred Noise*

Notes





- Collect M_T total samples for codes 1 to $2^N - 2$
- Count number of occurrences (hits) of each code, $h(n)_{ACTUAL}$, where n is the number of the code
- For FS triangle input, theoretical number of hits is:
  $h(n)_{THEORETICAL} = M_T / (2^N - 2)$
- Calculate DNL of each code for n = 1 to $n = 2^N - 2$:

$$DNL(n) = \frac{h(n)_{ACTUAL}}{h(n)_{THEORETICAL}} - 1$$

- Integrate DNL to obtain INL

Figure 5.38: *Histogram (Code Density) Test Setup*

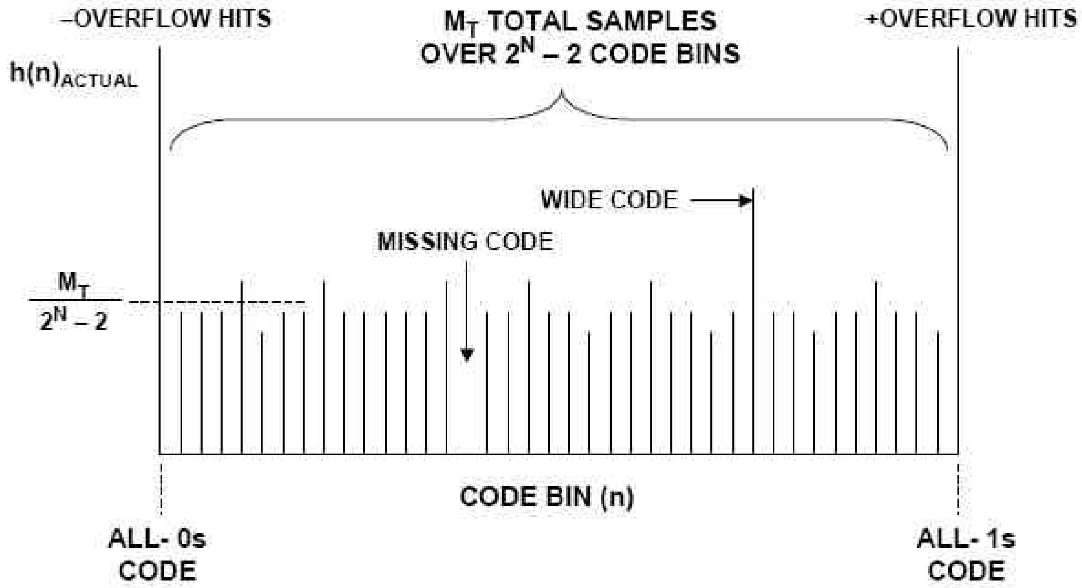


Figure 5.39: *Histogram for Linear Ramp Test*

Notes

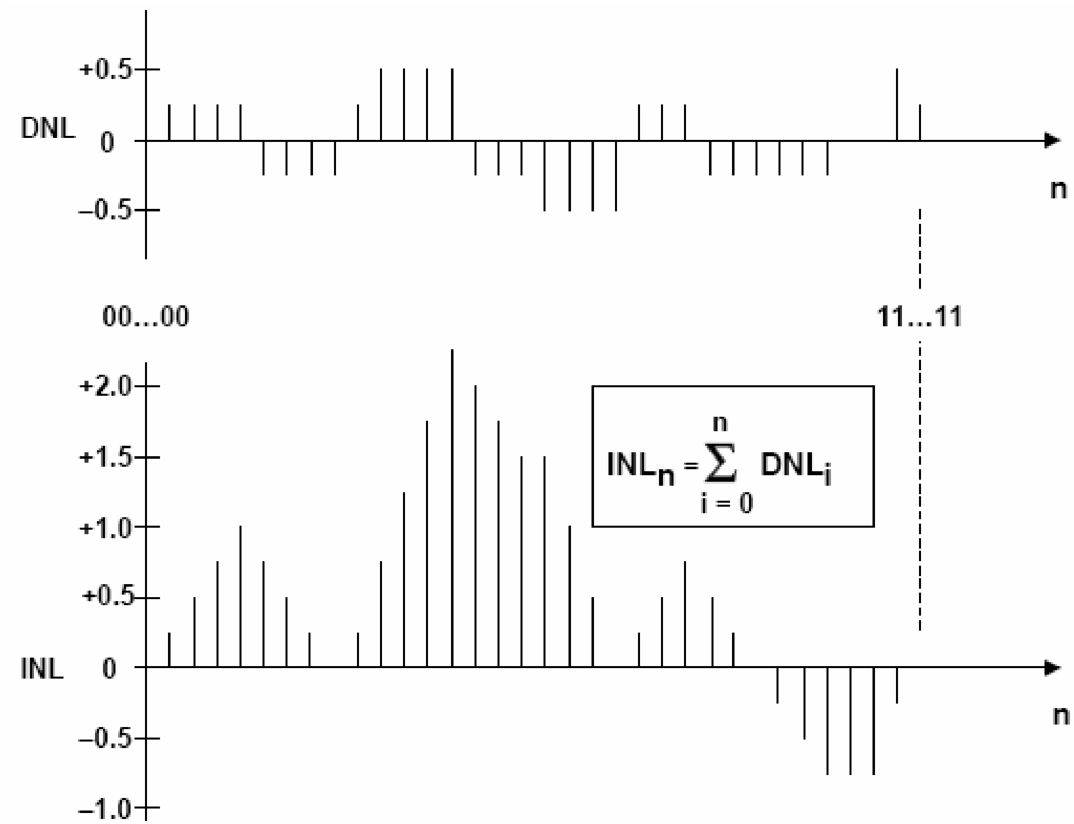
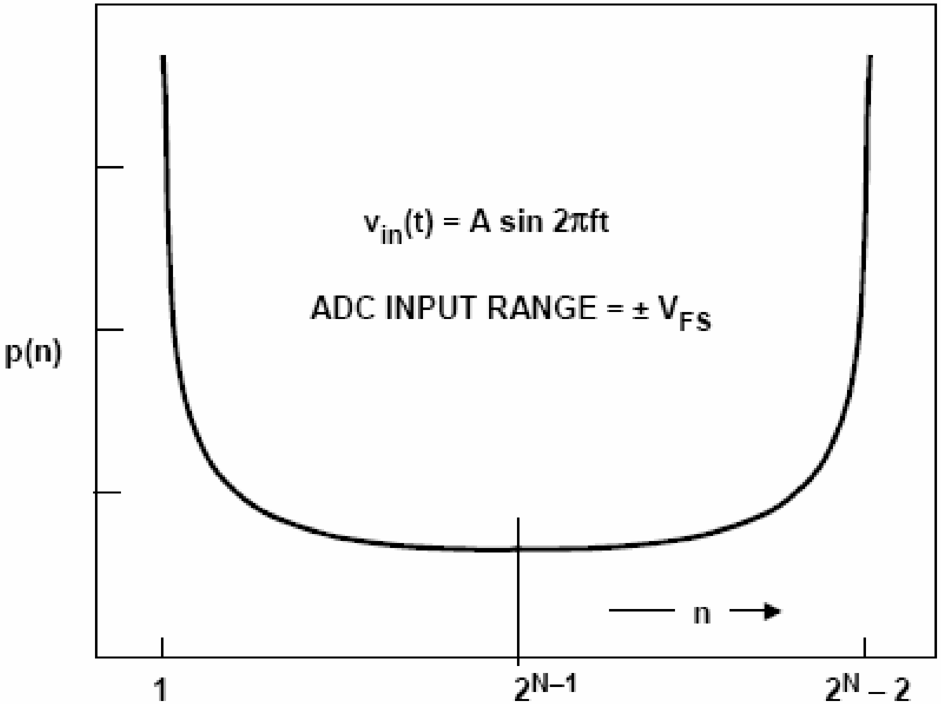


Figure 5.40: *Integration of DNL Data Yields INL*

Notes

Figures from Chapter 5: Testing Data Converters in *Analog-Digital Conversion* by Walt Kester, Analog Devices Inc.

Notes



$$p(n) = \frac{1}{\pi}\left[\sin^{-1}\left(\frac{V_{FS}\,(n - 2^{N-1})}{A\cdot 2^N}\right) - \sin^{-1}\left(\frac{V_{FS}\,(n - 1 - 2^{N-1})}{A\cdot 2^N}\right)\right]$$

Figure 5.41: *Sinewave Probability Density Function*

Notes

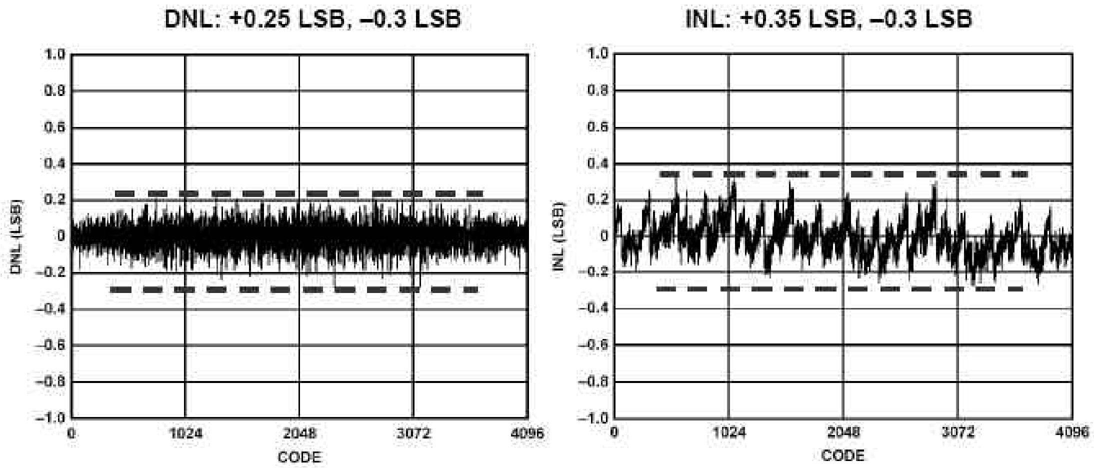


Figure 5.42: *Typical Static DNL and INL Histogram Plots for AD9236 12-Bit, 80-MSPS ADC*

Notes

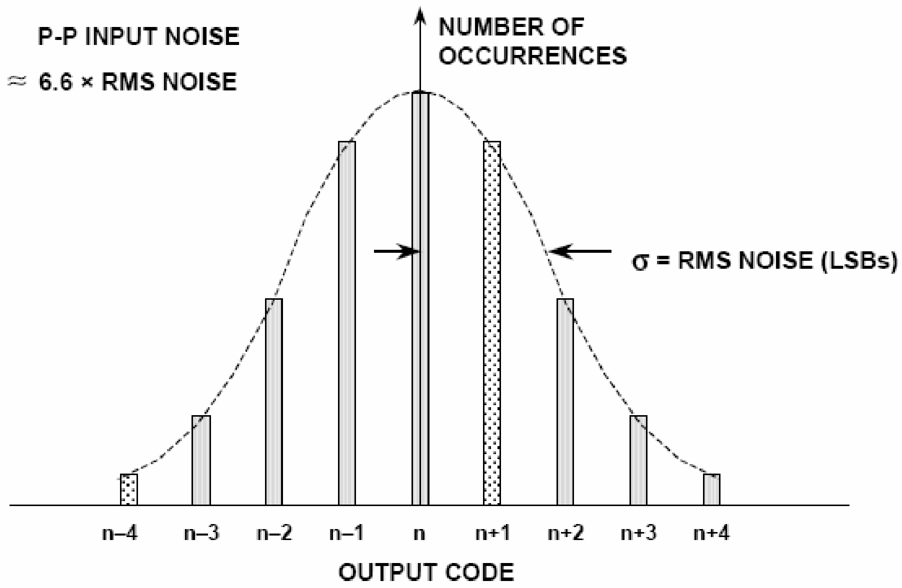


Figure 5.43: *Measuring Input-Referred Noise Using "Grounded Input" Histogram*

Notes

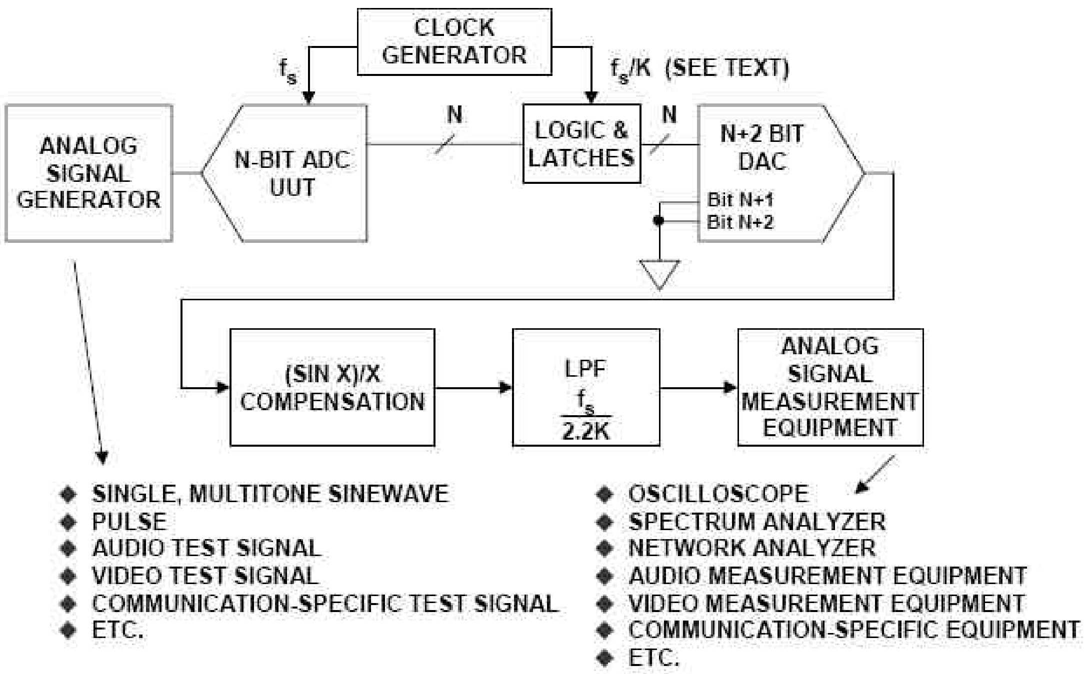


Figure 5.44: *"Back-to-Back" Setup for ADC Dynamic Testing*

Notes

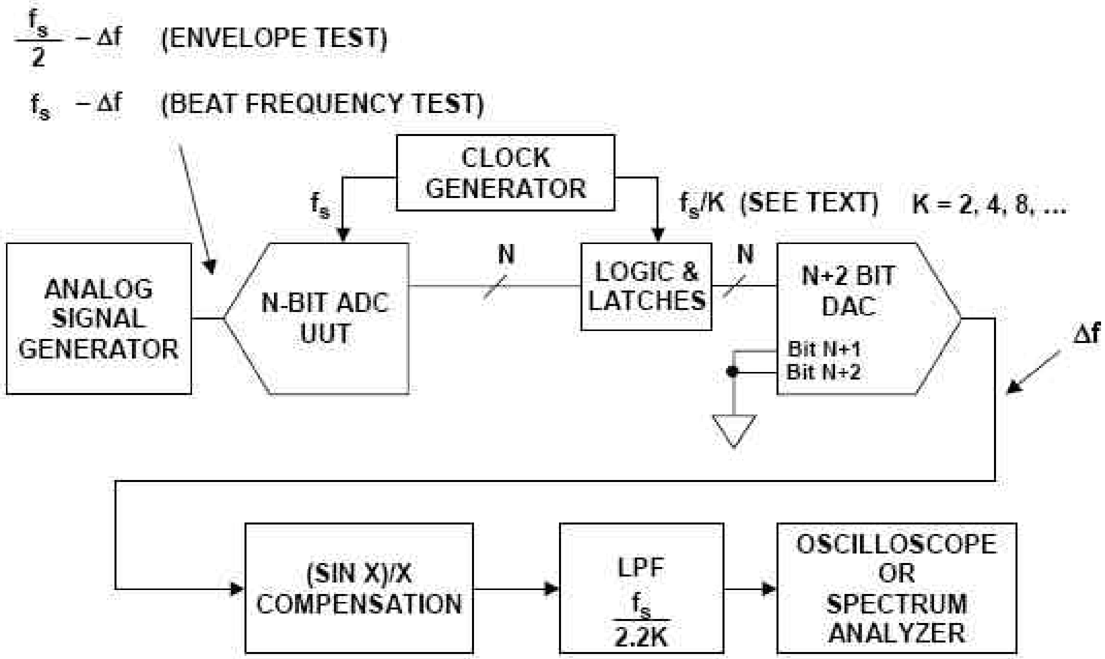
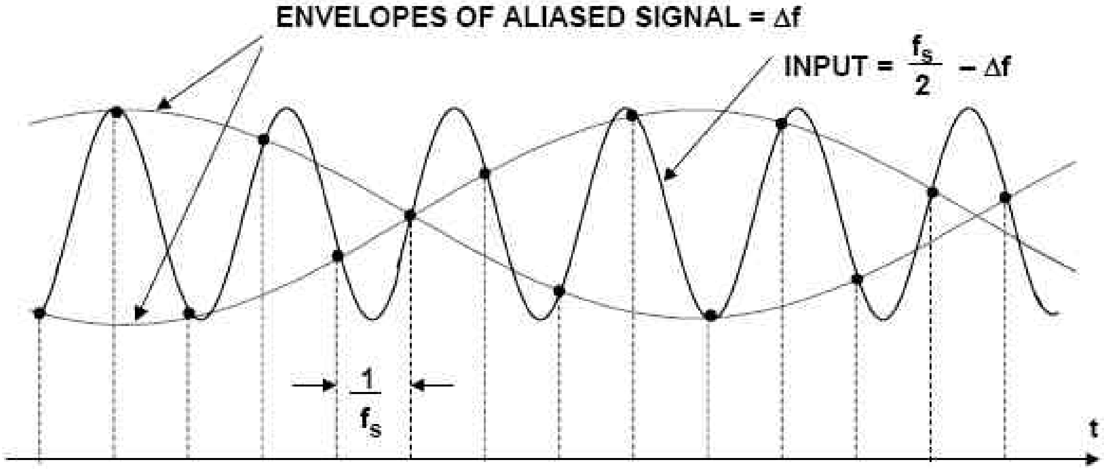


***Figure 5.45:** Envelope and Beat Frequency Test Setup*



NOTE: INPUT IS SLIGHTLY LESS THAN $f_s/2$

TAKE EVERY OTHER SAMPLE TO OBTAIN SINGLE WAVEFORM AT Δf

Figure 5.46: *Envelope Test with Input Frequency Near $f_s/2$*

Notes

Notes

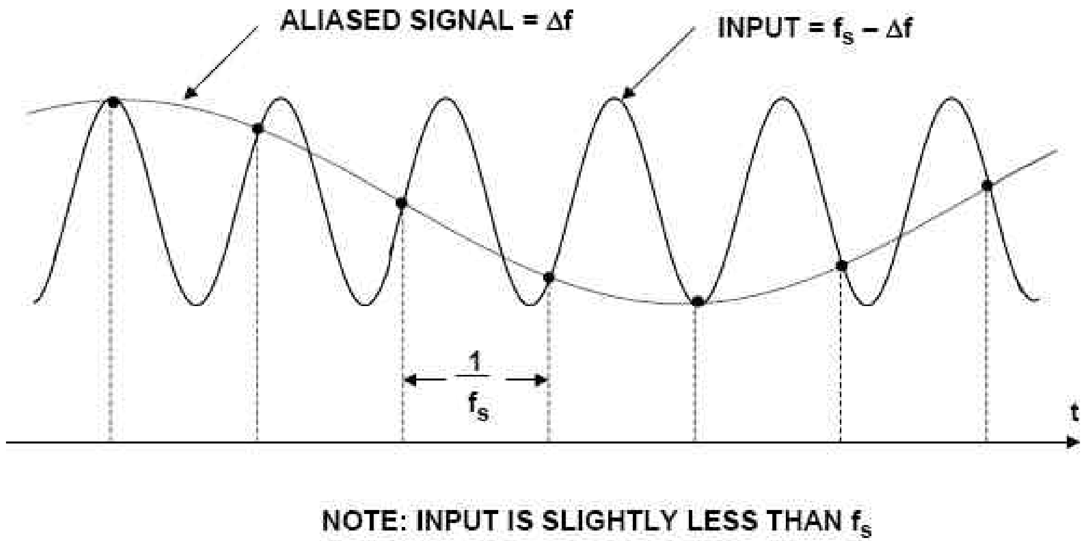
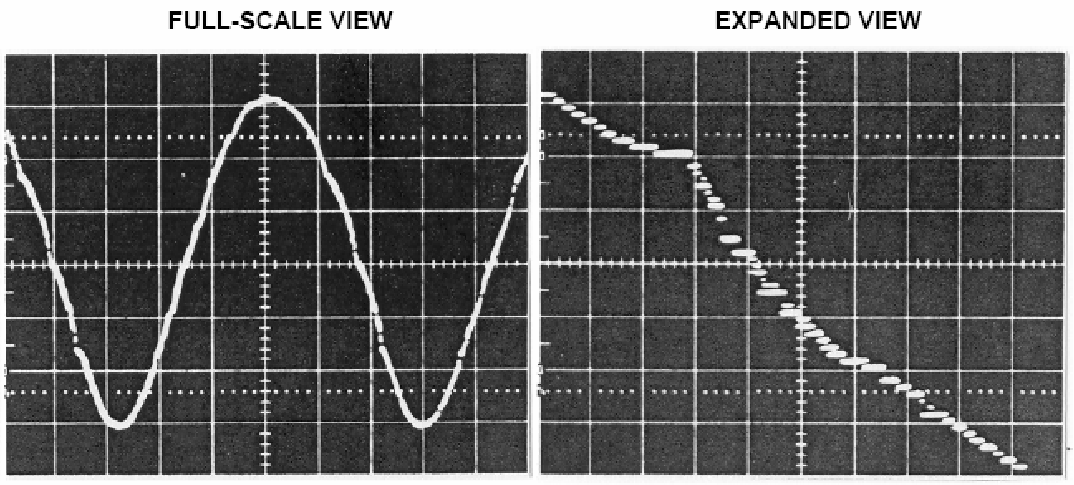


Figure 5.47: *Beat Frequency Test with Input Frequency Near f_s*

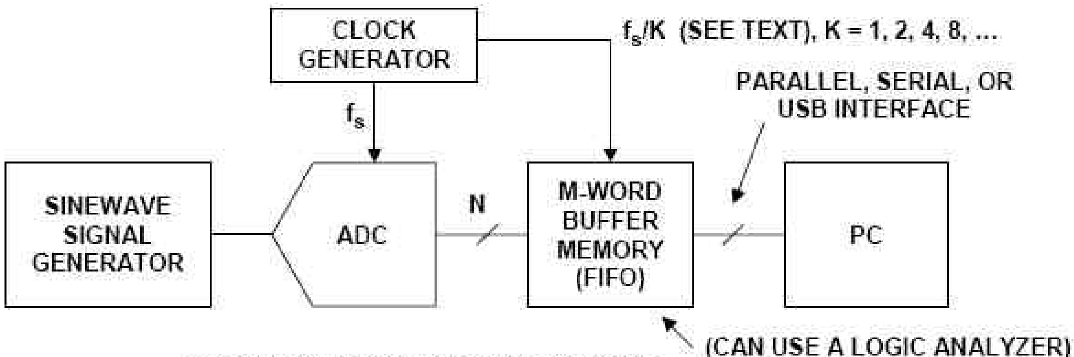
Notes



DATA FOR 8-BIT, 20-MSPS FLASH ADC,
f_s = 20 MSPS, f_{in} = 19.98 MHz, Δf = 20 kHz

Figure 5.48: *Beat Frequency and Envelope Tests Show ADC AC Nonlinearities*

Notes



- COLLECT M SAMPLES OF SINEWAVE
- CALCULATE BEST FIT SINEWAVE FROM DATA POINTS
- CALCULATE Q_A = ACTUAL RMS ERROR FROM BEST FIT SINEWAVE
- Q_T = THEORETICAL N-BIT RMS QUANTIZATION ERROR = $q/\sqrt{12}$
- $\text{ENOB} = N - \log_2\left[\frac{Q_A}{Q_T}\right]$

Figure 5.49: *Sinewave Curve Fit Test Setup for Measuring ADC ENOB*

Notes

- Digital Spectral Analysis
  - Spectrum Analyzers
  - Speech Processing
  - Imaging
  - Pattern Recognition
  - ADC Testing
- Filter Design
  - Calculating Impulse Response from Frequency Response
  - Calculating Frequency Response from Impulse Response
- The Fast Fourier Transform (FFT) is Simply an Algorithm for Efficiently Calculating the DFT

Figure 5.50: *Applications of the Discrete Fourier Transform (DFT)*

Notes

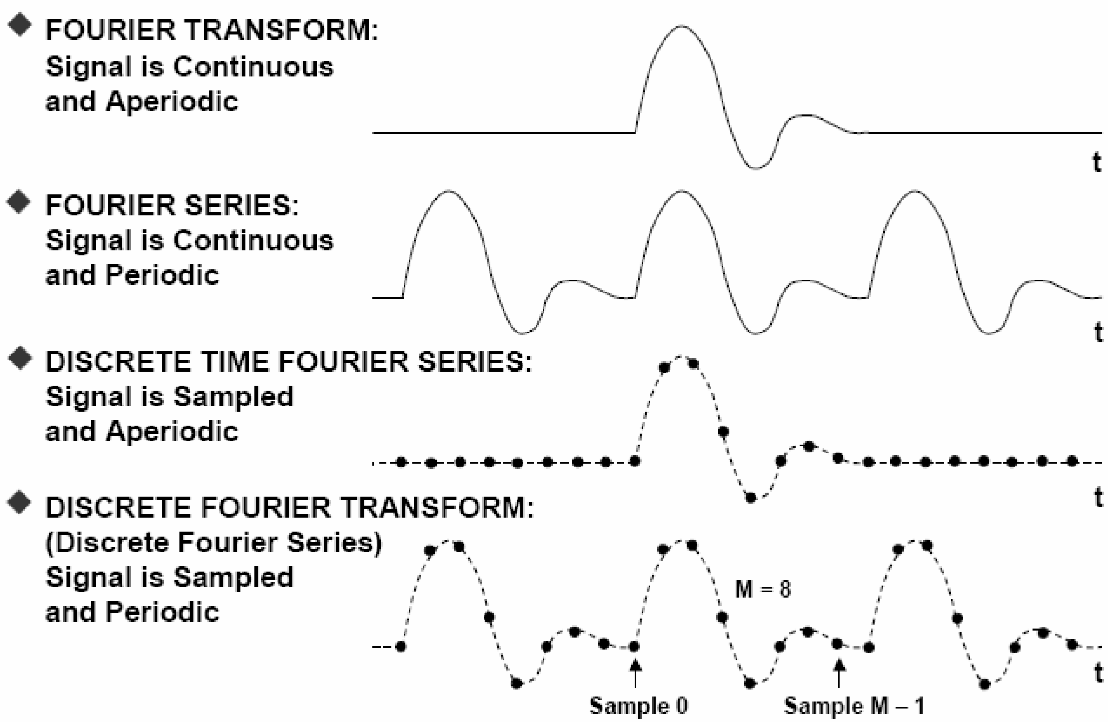


Figure 5.51: *Fourier Transform Family*

Notes

- A Periodic Signal Can be Decomposed into the Sum of Properly Chosen Cosine and Sine Waves (Jean Baptiste Joseph Fourier, 1807)
- The DFT Operates on a Finite Number (M) of Digitized Time Samples, x(n). When These Samples are Repeated and Placed "End-to-End", they Appear Periodic to the Transform.
- The Complex DFT Output Spectrum X(k) is the Result of Correlating the Input Samples with sine and cosine Basis Functions:

$$X(k) = \frac{1}{M}\sum_{n=0}^{M-1} x(n)\, e^{\frac{-j2\pi nk}{M}} = \frac{1}{M}\sum_{n=0}^{M-1} x(n)\left[\cos\frac{2\pi nk}{M} - j\sin\frac{2\pi nk}{M}\right]$$

$$0 \le k \le M-1$$

Figure 5.52: *The Discrete Fourier Transform (DFT)*

Notes

- $X(k) = \mathrm{Re}X(k) + j\,\mathrm{Im}X(k)$
- $\mathrm{MAG}[X(k)] = \sqrt{\mathrm{Re}X(k)^2 + \mathrm{Im}X(k)^2}$
- $\varphi[X(k)] = \tan^{-1}\dfrac{\mathrm{Im}X(k)}{\mathrm{Re}X(k)}$

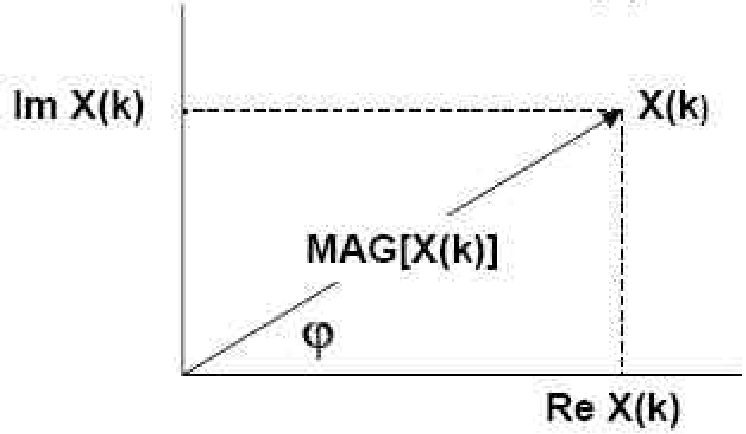


Figure 5.53: *Converting Real and Imaginary DFT Outputs into Magnitude and Phase*

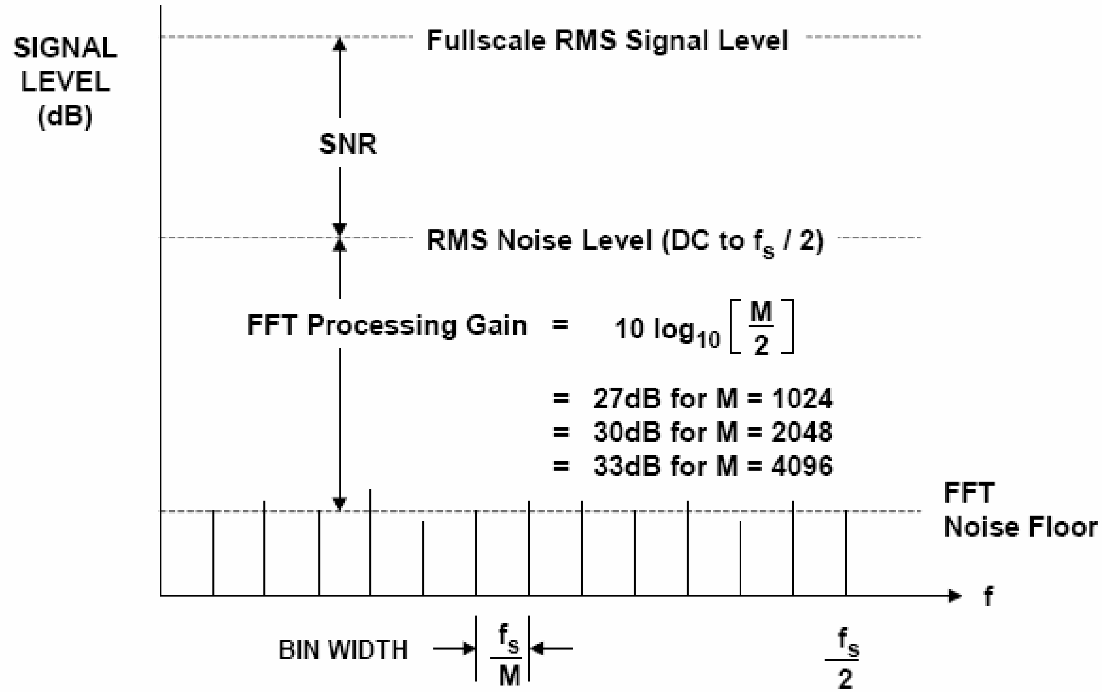


Figure 5.54: *FFT Output Shows Effects of Processing Gain*

Notes

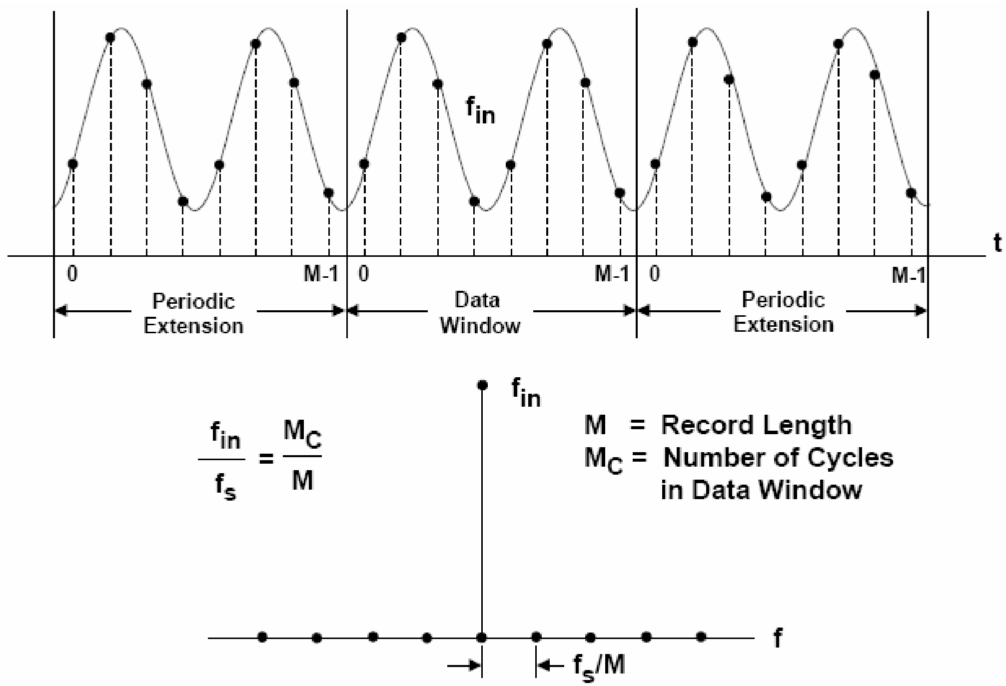


***Figure 5.55:** FFT of Sinewave Having Integral Number of Cycles in Data Window*

Notes

Notes

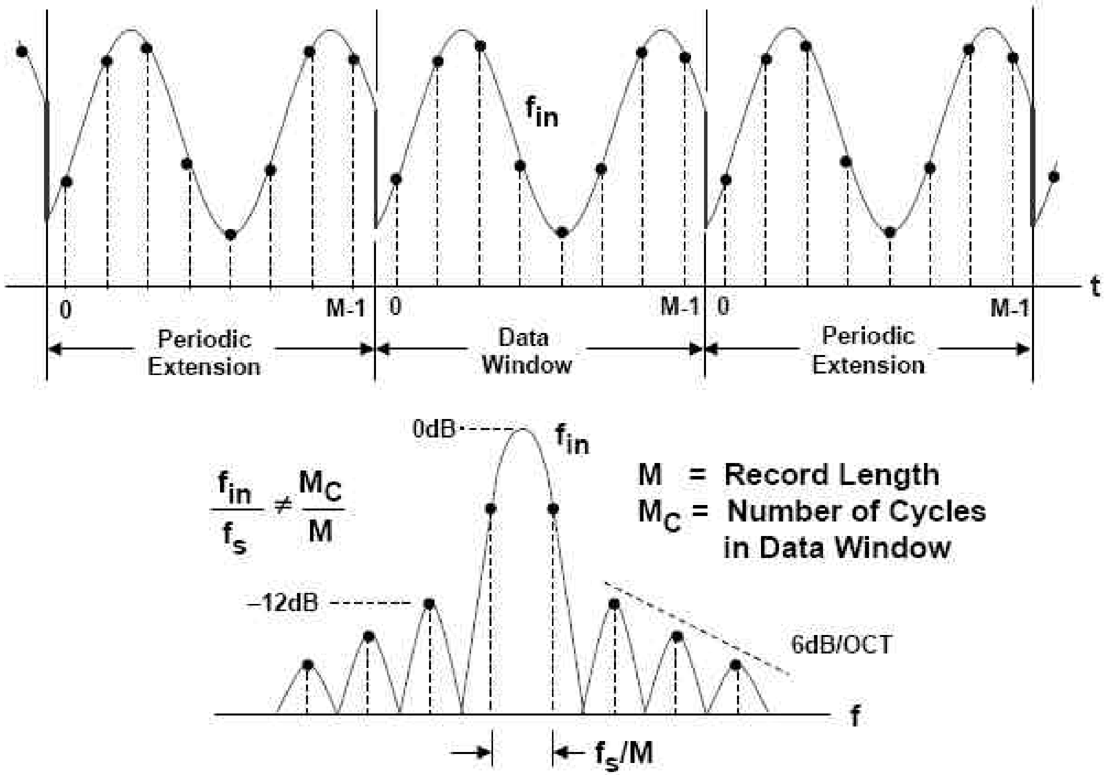


Figure 5.56: *FFT of Sinewave Having Non-Integral Number of Cycles in Data Window*

Notes

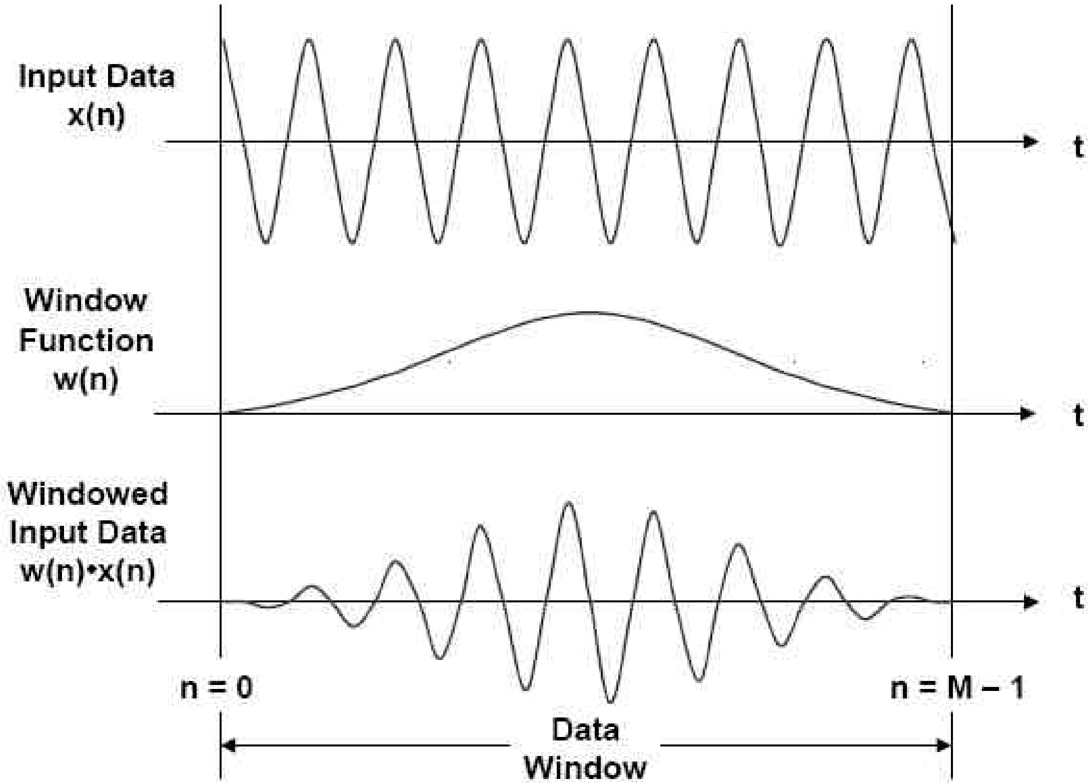


Figure 5.57: *Windowing to Reduce Spectral Leakage*

- **Hamming:** $w(n) = 0.54 - 0.46 \cos\left[\frac{2\pi n}{M}\right]$
- **Blackman:** $w(n) = 0.42 - 0.5 \cos\left[\frac{2\pi n}{M}\right] + 0.08 \cos\left[\frac{4\pi n}{M}\right]$
- **Hanning:** $w(n) = 0.5 - 0.5 \cos\left[\frac{2\pi n}{M}\right]$
- **Minimum 4-Term Blackman Harris** $w(n) = 0.35875 - 0.48829 \cos\left[\frac{2\pi n}{M}\right] + 0.14128 \cos\left[\frac{4\pi n}{M}\right] - 0.01168 \cos\left[\frac{6\pi n}{M}\right]$

$0 \leq n \leq M-1$

Figure 5.58: *Some Window Functions*

Notes

Notes

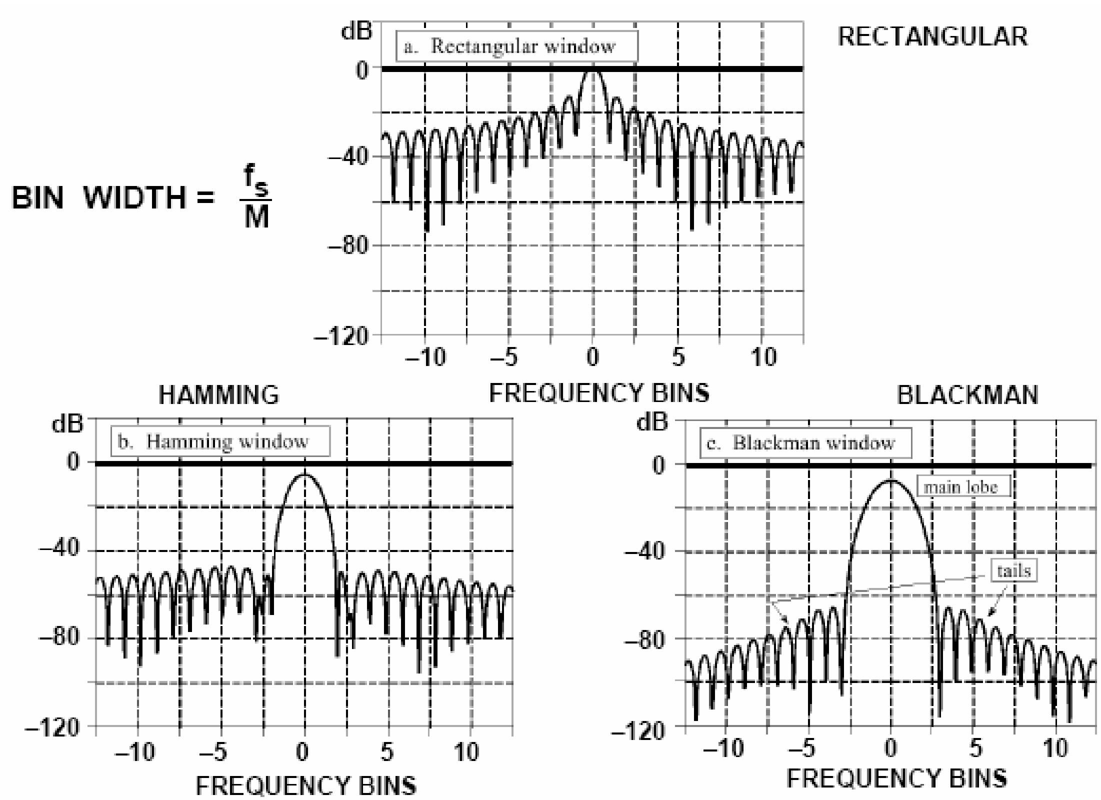


Figure 5.59: *Frequency Response of Rectangular, Hamming, and Blackman Windows for M = 256*

Notes

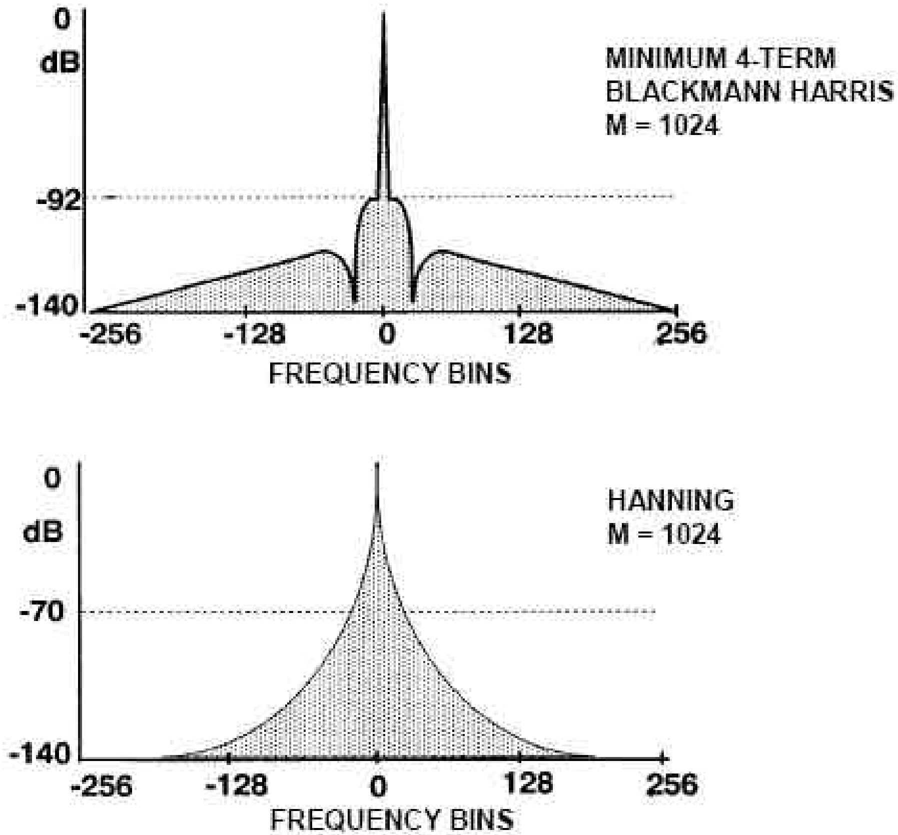


Figure 5.60: *Comparison of Two Popular Window Functions Used in ADC Testing*

Notes

WINDOW FUNCTION	3dB BW (Bins)	6dB BW (Bins)	HIGHEST SIDELOBE (dB)	SIDELOBE ROLLOFF (dB/Octave)
Rectangle	0.89	1.21	–12	6
Hamming	1.3	1.81	– 43	6
Blackman	1.68	2.35	–58	18
Hanning	1.44	2.00	–32	18
Minimum 4-Term Blackman-Harris	1.90	2.72	–92	6

Figure 5.61: *Popular Windows and Figures of Merit*

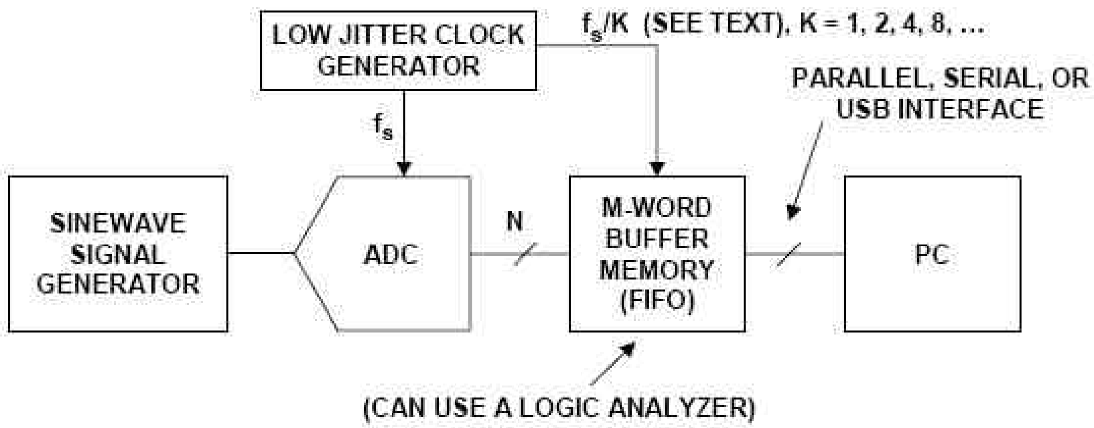


Figure 5.62: *FFT Test Setup*

Notes

Notes

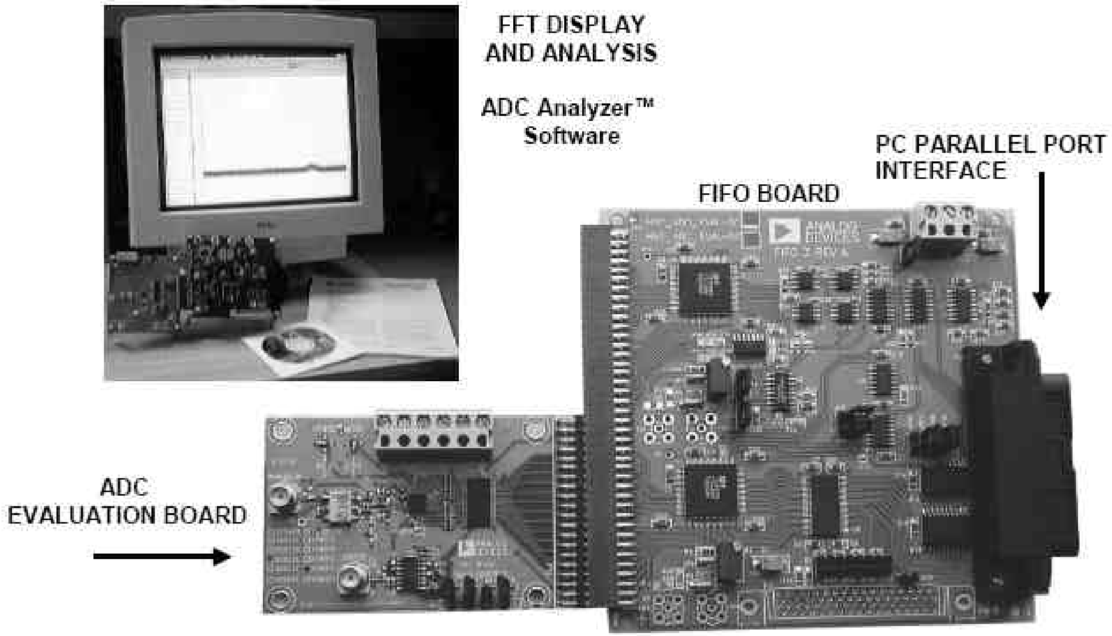


Figure 5.63: *Analog Devices' High Speed ADC FIFO Evaluation Kit*