ECE 225
High-Speed Digital IC Design
Lecture 9

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Dynamic Logic
Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or $V_{DD}$ via a low resistance path.
  - fan-in of $n$ requires $2n$ ($n$ N-type + $n$ P-type) devices

- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires only $n + 2$ ($n+1$ N-type and 1 P-type) transistors
Dynamic Gate

Two phase operation
- Precharge (CLK = 0)
- Evaluate (CLK = 1)
Dynamic Gate

Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)
Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on $C_L$. 
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is $N + 2$ (versus $2N$ for static complementary CMOS)

- Full swing outputs ($V_{OL} = \text{GND}$ and $V_{OH} = V_{DD}$)

- Non-ratioed - sizing of the devices does not affect the logic levels

- Faster switching speeds
  - reduced load capacitance due to lower input capacitance ($C_{in}$)
  - reduced load capacitance due to smaller output loading ($C_{out}$)
  - no $I_{sc}$, so all the current provided by PDN goes into discharging $C_L$
Properties of Dynamic Gates

- Overall power dissipation usually **higher** than static CMOS
  - no static current path ever exists between $V_{DD}$ and GND (including $P_{sc}$)
  - no glitching
  - higher transition probabilities
  - extra load on Clk

- PDN starts to work as soon as the input signals exceed $V_{Th}$, so $V_M$, $V_{IH}$ and $V_{IL}$ equal to $V_{Th}$
  - low noise margin ($NM_L$)

- Needs a precharge/evaluate clock
Dynamic Gate

Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)

Out = CLK + (AB)+C . CLK

To avoid contention at the dynamic node (Out)....
Conditions on Output

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Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is $N + 2$ (versus $2N$ for static complementary CMOS)
- Full swing outputs ($V_{OL} = \text{GND}$ and $V_{OH} = V_{DD}$)
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance ($C_{in}$) due to lower number of transistors per gate and single transistor load per fan-in (reduced logical effort, $2/3$ for a 2-input dynamic NOR)
  - reduced load capacitance due to smaller output loading ($C_{out}$)
  - no $I_{sc}$, so all the current provided by PDN goes into discharging $C_L$
Properties of Dynamic Gates

- Overall power dissipation usually **higher** than static CMOS
  - no static current path ever exists between $V_{DD}$ and GND (including $P_{sc}$)
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- $V_{OH}=V_{DD}$, $V_{OL}=Gnd$
- PDN starts to work as soon as the input signals exceed $V_{Tn}$, so $V_M$, $V_{IH}$ and $V_{IL}$ equal to $V_{Tn}$
  - low noise margin ($NM_L$)
- Needs a precharge/evaluate clock
Issues in Dynamic Design 1: Charge Leakage

Leakage sources: reverse biased diode and subthreshold

Dominant component is subthreshold current

Note: leakage of precharge PMOS can partially compensate for the charge loss at the dynamic node
Solution to Charge Leakage

Same approach as level restorer for pass-transistor logic

Keeper: reduces output impedance

Contention between keeper and PDN---keeper size should be optimized….

eliminates static power
**Issues in Dynamic Design 2: Charge Sharing**

Charge stored originally on $C_L$ is redistributed (shared) over $C_L$ and $C_A$ leading to reduced robustness.

Output node voltage drops and cannot be recovered due to the dynamic nature of the circuit.
Charge Sharing

Initial conditions: $V_{out}(t=0)=V_{DD}$ and $V_x(t=0)=0$

2 possible scenarios:

**case 1) if $\Delta V_{out} < V_{Tn}$**

$$C_L V_{DD} = C_L V_{out}(t) + C_a (V_{DD} - V_{Tn}(V_X))$$

or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = \frac{C_a}{C_L} (V_{DD} - V_{Tn}(V_X))$$

**case 2) if $\Delta V_{out} > V_{Tn}$**

$$\Delta V_{out} = -V_{DD} \left( \frac{C_a}{C_a + C_L} \right)$$

Which of these scenarios is valid?
Initial conditions: $V_{out} (t=0) = V_{DD}$ and $V_x(t=0) = 0$

2 possible scenarios:

$\Delta V_{out} < V_{Tn}$ ....case I

$\Delta V_{out} > V_{Tn}$ ....case II

Which of these scenarios is valid?

First find the capacitance ratio: $C_a/C_L$

The boundary condition between the two cases can be determined by setting $\Delta V_{out} = V_{Tn}$.

Hence,

$$\frac{C_a}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}}$$

Case I holds when the $C_a/C_L$ ratio is smaller than the value defined above, otherwise Case II holds.

Overall, it is desirable to keep $\Delta V_{out} < |V_{Tp}|$ ---since the output of dynamic gate might be connected to a static inverter---low level of $V_{out}$ will cause static power consumption. Also, $V_{out}$ must not go below $V_M$ of the inverter.
Charge Sharing Example

Dynamic 3-input EXOR gate

\[ Out = A \oplus B \oplus C \]

\[ C_a = 15 \text{fF} \]
\[ C_b = 15 \text{fF} \]
\[ C_c = 15 \text{fF} \]
\[ C_d = 10 \text{fF} \]

Worst case change in Output is obtained by exposing the maximum number of internal capacitances to the output: this happens for \( \overline{A}BC \) or \( A\overline{B}C \).
Precharge internal nodes (to $V_{DD}$) using a clock-driven transistor (at the cost of increased area and power)
Issues in Dynamic Design 3: Backgate Coupling

High impedance node—sensitive to crosstalk effects

Capacitive coupling between dynamic node Out1 and H-L transition at Out2 through the gate-drain and gate-source capacitance of M4
Coupling causes dynamic node Out1 to drop significantly, which further prevents Out2 from dropping all the way to zero---static power dissipation.
**Issues in Dynamic Design 4: Clock Feedthrough**

Coupling between Out and Clk input of the precharge device due to *gate to drain* capacitance. So voltage of Out can rise above $V_{DD}$ on the L-H Clk transition (assuming PDN is off). The fast rising (and falling edges) of the clock couple to Out.

*Dynamic circuits need careful simulation!*

Clk feedthrough can cause normally reverse biased junction diodes of the precharge transistor to become forward biased---causing electron injection into the substrate that can be collected by a nearby high-impedance node in the 1 state, eventually resulting in faulty operation.
Clock Feedthrough

Clock feedthrough

Clock feedthrough

In & Clk

Out

Clock feedthrough

Time, ns

Voltage
Other Effects

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)
Cascading Dynamic Gates

Simple cascoding doesn’t work...

During precharge both Out1 and Out2 should stay high...

If In goes to 1, Out1 discharges to 0 and Out2 should remain high...

However, Out1 discharges to 0 within a finite time... and Out2 drops...

Out2 reaches some intermediate voltage... can’t be recovered... reduced NM and malfunctioning

As long as Out1 > V_M (~V_Tn) of the second inverter, Out2 will decrease leading to reduced NMs

Solution: Set all inputs to 0 during precharge
For correct operation only 0 → 1 transitions should be allowed at inputs!
**Domino Logic**

An n-type dynamic logic followed by a static inverter...

All inputs (are outputs of other Domino gates) are set to 0 at the end of precharge phase

Only 0 to 1 transition at the inputs during evaluation phase: during evaluation, dynamic gate conditionally discharges and the output of the inverter makes a conditional transition from 0 to 1.
Domino Logic

An n-type dynamic logic followed by a static inverter…

The static inverter reduces the capacitance of the dynamic output node by separating internal and load capacitances.

The inverter can also be used to drive a keeper device to combat leakage and charge redistribution.
Why Domino?

Domino chain

Precharge: all inputs=0

Evaluation: Output of domino1 either stays at 0 or makes a transition from 0 to 1, affecting the second gate. This effect ripples through the whole chain… like a line of falling dominos!
Properties of Domino CMOS Logic

- Only non-inverting logic can be implemented
  - Major limitation
  - Can be overcome using dual-rail domino (an expensive solution)

- Very high speed
  - Only rising edge delays, and $t_{\text{PHL}} = 0$
  - Static inverter can be skewed to match the fanout, which is already much smaller than in the complimentary case, since only a single gate capacitance needs to be accounted for per fan-out gate.
  - Input capacitance reduced – smaller logical effort
Differential (Dual Rail) Domino

Solves the problem of non-inverting logic
Designing with Domino Logic

Inputs = 0 during precharge

Time taken to precharge equals the critical path delay!
Better to use the evaluation device....
Footless Domino

While In2 remains high, Out2 can not be precharged….

Similarly, third gate has to wait for Out2 to precharge…and so on

Precharge is rippling – short-circuit current---extra power dissipation
A solution is to delay the clock for each stage
np-CMOS

Alternative to cascading dynamic gates…uses n-type and p-type dynamic logic
Exploits duality between n-tree and p-tree logic gates to eliminate cascading problem
No extra inverter at the output….unless output of n-tree needs to be connected to another n-tree gates

Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN

Drawback: p-tree gates are slower than the n-tree gates…needs proper skewing of PMOS….area penalty
No buffers---so dynamic nodes can only be routed between gates