ECE225
High-Speed Digital Integrated Circuit Design

University of California, Santa Barbara
Department of Electrical and Computer Engineering
Winter 2006

Course Description:
Advanced digital VLSI design: CMOS scaling, nanoscale issues including variability, thermal management, interconnects, reliability; non-clocked, clocked and self-timed logic gates; clocked storage elements; high-speed components, PLLs and DLLs; clock and power distribution; memory systems; signaling and I/O design; low-power design.

Class Room / Schedule: PHELP 1437 Tue & Thu 4:00PM-5:50PM

Instructor: Prof. Kaustav Banerjee, Room 4151, Engineering I
Email: kaustav@ece.ucsb.edu
URL: http://www.ece.ucsb.edu/Faculty/Banerjee/
Office Hours: Fri 1:00PM-2:00PM or appointment by email.

Text: *Digital Integrated Circuits: A Design Perspective* (2nd Edition), Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Prentice Hall, 2003.

References: To be posted on the class homepage:
http://www.ece.ucsb.edu/courses/ECE225/225-W06Banerjee/default.html

Software: MMI: Max and Sue VLSI layout tools, Avanti HSPICE, Mentor Graphics: XCallibre, and Model Sim Suites

Prerequisites: ECE124A or equivalent, ECE 132 or equivalent

Grading:

Homework	20%
Midterm	20%
Project	25%
Final Exam	35%

Note:

- Late homeworks will be penalized (20% per day).
- Must complete all homeworks and project to pass.