ECE225/125
High-Speed Digital Integrated Circuit Design

University of California, Santa Barbara
Department of Electrical and Computer Engineering
Winter 2007

Course Description:
Advanced digital VLSI design: CMOS scaling, nanoscale issues including variability, thermal management, interconnects, reliability; non-clocked, clocked and self-timed logic gates; clocked storage elements; high-speed components, PLLs and DLLs; clock and power distribution; memory systems; signaling and I/O design; low-power design.

Class Room/Schedule: PHELP 1437 Tue & Thu 4:00PM-5:50PM

Instructor: Prof. Kaustav Banerjee, Room 4151, Engineering I
Email: kaustav@ece.ucsb.edu
URL: http://www.ece.ucsb.edu/Faculty/Banerjee/
Office Hours: Fri 1:00PM-2:00PM or appointment by email.

Text: Several books will be used for different sub-topics. The ECE 124A text book (by Weste and Harris) is recommended as a reference.

References: To be posted on the class homepage:
http://www.ece.ucsb.edu/courses/ECE225/225_W07Banerjee/default.html

Software: MMI: Max and Sue VLSI layout tools, Avanti HSPICE, Mentor Graphics: XCallibre, and Model Sim Suites

Prerequisites: ECE124A or equivalent, ECE 132 or equivalent

Grading: Will be based on assignments, exams and final project

Note:

- Late assignments will be penalized (20% per day).
- Must complete all assignments and project to pass.