Are Carbon Nanotubes the Future of VLSI Interconnections?

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ABSTRACT

Increasing resistivity of copper with scaling and rising demands on current density requirements are driving the need to identify new wiring solutions for deep nanometer scale VLSI technologies. Metallic carbon nanotubes (CNTs) are promising candidates that can potentially address the challenges faced by copper and thereby extend the lifetime of electrical interconnects. This paper examines the state-of-the-art in CNT interconnect research and discusses both the advantages and challenges of this emerging nanotechnology.

Categories and Subject Descriptors: B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, VLSI.*

General Terms

Performance, Design, Reliability, Experimentation, Theory.

Keywords: Carbon nanotubes, interconnects, VLSI.

1. INTRODUCTION

Since their accidental discovery by Sumio Iijima of NEC in 1991 [1], carbon nanotubes (CNTs) have aroused a tremendous amount of interest in their use as building blocks of future integrated circuits due to their outstanding electrical properties [2]. Alongside research efforts into developing *semiconducting* carbon nanotube based transistors [3], *metallic* CNTs have also been suggested as an interconnect material due to their high current carrying capacity and mechanical stability [4]. Since then, several groups have reported on fabrication of CNT interconnects (see Section 2). Recently, performance and thermal analysis of CNT interconnects reported by the authors in [5] have shown that CNT based interconnects can potentially offer significant advantages over copper. This paper examines the state-of-the-art of CNT interconnects while analyzing the advantages as well as the challenges of this emerging technology. The imminent challenges of copper interconnect technology are first highlighted in the remainder of this section. Section 2 provides a brief introduction to CNTs and outlines various fabrication and integration challenges for CNT interconnects. Section 3 summarizes recent efforts into the modeling of CNT interconnects from a circuit perspective including derivation of the equivalent circuit parameters for a *CNT bundle* interconnect. Section 4 compares the performance, power dissipation and thermal/reliability aspects of CNT interconnect to scaled copper interconnects. Section 5 highlights the concept of *hybrid CNT/Cu* interconnects—employing CNT vias in tandem with copper interconnects, and shows its remarkable advantages from a reliability/thermal-management perspective. Concluding remarks are made in Section 6.

1.1 Imminent Challenges for Cu Interconnects

The resistivity of copper interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu at room temperature) in current and imminent technologies [8], is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layer (**Fig. 1**) [6, 9]. The steep rise in parasitic resistance of copper interconnects not only increases interconnect delay at the global level but also at the local level [7]. More importantly, in combination with the decreasing thermal conductivity of low-k dielectrics and increasing current density demands from small dimension interconnects, the rising Cu resistivity also poses a reliability concern due to Joule heating induced significant metal temperature rise [6]. The large metal temperature rise, which exponentially degrades interconnect electromigration (EM) lifetime, severely limits the maximum current carrying capacity of future Cu interconnects as shown in **Fig. 2**.

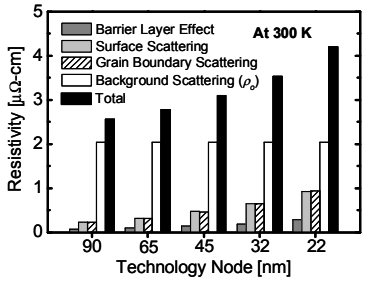

Fig. 1. Scaling of metal resistivity for the ITRS intermediate tier wires (at 300K), mainly as a result of the increasing impact of surface and grain boundary scattering of electrons [6]. The impact is even higher for local tier wires and vias (or contacts) that have the smallest cross-sectional dimensions among all on-chip interconnects.

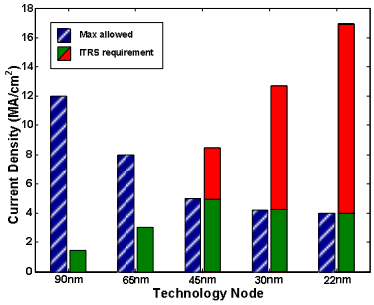

Fig. 2. Maximum allowed current density (duty ratio=0.001) in local vias from self-consistent electromigration lifetime estimation vs. the ITRS (2003) requirement for current density in local vias, even with most optimistic scaling scenario for via height at various nodes [7].

2. CARBON NANOTUBES

A carbon nanotube is a one-atom thick sheet of graphite (called *graphene*) rolled up into a seamless cylinder with diameter of the order of a nanometer. CNTs exhibit extraordinary strength and unique electrical properties, and are efficient conductors of heat. There are two main types of carbon nanotubes: *single-walled* nanotubes (SWCNTs) and *multi-walled* nanotubes (MWCNTs). In SWCNTs the cylindrical structure consists of a single layer of graphene, while MWCNTs consist of multiple concentric cylinders or the graphene sheet is simply rolled in around itself resembling a scroll of parchment, and are metallic in nature.

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2.1 Single-Walled Carbon Nanotubes

SWCNTs are a very important variety of CNT because they exhibit important electric properties that are not shared by MWCNTs. The remarkable properties (**Table 1**) of SWCNTs stem from the symmetry and unusual electronic structure of graphene [10]. It has a bandgap in most directions in **k**-space, but has a vanishing bandgap along specific directions and is called a zero-bandgap semiconductor. When wrapped to form a nanotube, the momentum of the electrons moving around the circumference of the tube is quantized. The result is either a one-dimensional (1-D) *metal* or *semiconductor* (see **Fig. 3**), depending on how the allowed momentum states compare with the preferred directions for conduction. Metallic SWCNTs have a Fermi velocity $v_F = 8\times10^5$ m/s that is comparable to typical metals.

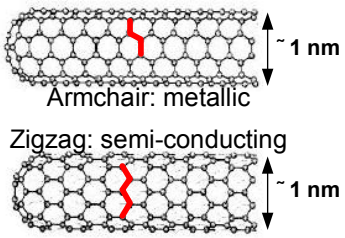

Fig. 3. Different configurations and resulting electrical conduction types of carbon nanotubes depending on the direction along which the graphene sheets are rolled up (chirality) [11].

Table 1. Electrical and thermal properties of SWCNTs vs copper. Although the current density values reported in [12] are based on MWCNTs but SWCNTs exhibit similar current carrying capacity [45].

Properties	CNT	Cu
Mean free path (nm) @ room temp	>1000 [11]	40
Max current density (A/cm^2)	>1x10^{10} [12]	~1x10^6
Thermal conductivity (W/mK)	5800 [13]	385

2.2 Carbon Nanotubes in Interconnect Applications

Metallic CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future [4, 14, 15] because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [12, 16, 17, 18]. An isolated CNT can carry current densities in excess of 10^{10} A/cm^2 without any signs of damage even at an elevated temperature of 250 ^{0}C [12], thereby eliminating EM reliability concerns that plague Cu interconnects.

However, the high resistance associated with an isolated CNT (greater than 6.45 KΩ) [11] necessitates the use of a *bundle* (rope) of CNTs conducting current in parallel to form an interconnection [4, 15]. Moreover, due to the lack of control on *chirality*, any bundle of CNTs consists of metallic as well as semi-conducting nanotubes (the semi-conducting CNTs do not contribute to current conduction in an interconnect). In practice, the observed d.c. resistance of a CNT (at low bias) is much higher than the resistance derived above. This is due to the presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance. As observed in [19], making a reliable contact to a CNT is very challenging, and the resistance arising from these imperfect contacts is often so high that it masks the observation of intrinsic transport properties. The observed resistance for CNTs has typically been in the range of 100 KΩ [19, 20], although in a few cases the lowest observed resistance has been seen to approach the theoretical limit of ~7 KΩ [20].

2.2.1 Fabrication and Integration Challenges

The pioneering work by Kreupl et al. [4] proposed a method for growing MWCNT bundles by Chemical Vapor Deposition (CVD) from the bottom of vias and contact holes decorated by an iron-based catalyst. The high temperature (700 ^{0}C) step involved in [4] during the CNT growth has been lowered to 540 ^{0}C in [21] by employing a hot-filament (HF)–CVD technique. Additionally, advances in reducing the metal-nanotube contact resistances for such MWCNT bundles deposited in contact holes have also been reported [14]. However, CNTs deposited as such on a substrate or inside a trench appear as entangled "noodles" which is undesirable. Moreover, this approach has the problems associated with etching of high aspect ratio vias and seeding the bottom of a deep trench with a catalyst for CNT growth. The work in [15] on the other hand provides an alternative bottom-up process in which MWCNTs are first grown (using HF-CVD) at pre-specified locations, then gap-filled with oxide and finally planarized. **Fig. 4** shows a schematic of the sequence for this process which may alleviate the traditional problems associated with etching high aspect ratio vias. A Si (100) wafer covered with 500 nm thermal oxide and 200 nm Cr (or Ta) lines is used to deposit 20 nm thick Ni as a catalyst. Ion beam sputtering is used to deposit Ni on patterned spots for local wiring or contact hole applications. For global wiring, Ni can be deposited as a 20 nm thick micron-scale film. Plasma enhanced chemical vapor deposition (PECVD) is then used to grow a low density MWCNT array by an inductively coupled plasma process or dc plasma-assisted hot-filament CVD. Next, the free space between the individual CNTs is filled with SiO_2 by CVD using tetraethylorthosilicate (TEOS). This is followed by CMP to produce a CNT array embedded in SiO_2 with only the ends exposed over the planarized solid surface.

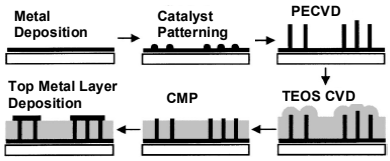

Fig. 4. Schematic of process sequence for bottom-up fabrication of CNT bundle vias [15].

Nevertheless, the fabrication of CNT interconnects poses several challenges because of the need for low thermal-budget, dense metallic SWCNT bundles. It is important to note that although MWCNTs are metallic in nature, they are less favourable for interconnects because they typically exhibit ballistic conductance over very short lengths (few nanometers) [22, 23] as compared to SWCNTs which have typical mean free paths of the order of a micron [11]. Until recently it has been difficult to grow bundles of SWCNTs for interconnects because the fertility of the catalyst particles for SWCNT growth was low [24]. Although recent progress has been made in growing bundles of SWCNTs by addition of water or oxygen to increase the fertility of the growth catalyst [25, 26], this approach has not yet been applied to the fabrication of interconnects.

3. MODELING & ANALYSIS OF CNT INTERCONNECTS

The first reported work comparing CNT interconnects to copper [7] highlighted the imminent thermal/reliability problems of minimum dimension Cu interconnects, vias and contacts and examined the advantages as well as the process technology requirements for CNT bundle based vias. However, several studies comparing only the performance of CNT interconnects to that of Cu have been contradictory. In [27] it is suggested that CNT interconnects do not offer any performance benefit over copper and hence are not suitable for VLSI. However, the analysis in [27] does not consider realistic CNT interconnect configurations (a flat array of CNTs will have very high resistance). A similar analysis in [28] arrives at the same conclusion but is also not practical as it fails to account for the influence of realistic drivers and loads on interconnect delay. On the

other hand, [29, 30, 31] suggest that CNT bundle interconnects have superior performance compared to Cu but the assumptions in these works are unrealistic. They do not consider the density of nanotubes in a CNT bundle nor do they analytically model the equivalent circuit parameters of CNT bundle interconnects. Realistic drivers/loads are not considered either and the imperfect metal-nanotube contact resistance (R_c, which is often so high as to overshadow the intrinsic resistance R_F [19]) is completely ignored. Moreover, while [29] avoids the calculation of CNT bundle capacitance by unjustifiably assuming that the capacitance is the same as that for copper interconnects, [31] does not explain how the same interconnect analysis program can be used to extract capacitances for copper interconnects as well as for CNT bundles. Finally, [31] concludes that a flat array of metallic CNTs performs better than a Cu interconnect, a result that directly contradicts [27, 28]. Additionally, all these works [27-31] unjustifiably include a *kinetic inductance* term in their delay models that can lead to large errors. The work in [32] addresses these drawbacks and performs a comprehensive analysis of the performance of CNT bundle VLSI interconnects vis-à-vis copper interconnects, presenting both the advantages as well as the limitations of CNT interconnects. In the rest of this section, the state-of-the-art in modeling of resistance, capacitance and inductance of SWCNTs along with an equivalent circuit for SWCNT bundle interconnect are presented.

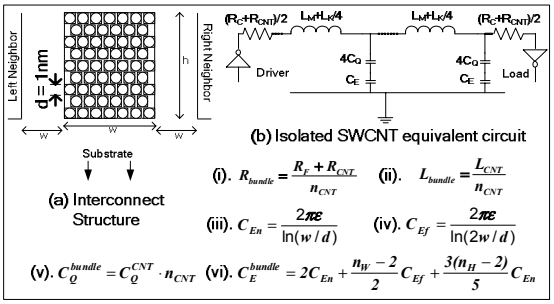

Fig. 5. (a) CNT bundle interconnect structure and **(b)** equivalent circuit [33] for isolated SWCNT. Equations i-vi: equivalent circuit parameters for a CNT bundle. C_{En} and C_{Ef} are the parallel plate capacitances of isolated CNT with respect to near and far neighboring interconnects respectively [32].

3.1 R-L-C Formulae for CNT Interconnects

3.1.1 CNT Resistance

Fig. 5 depicts a CNT bundle interconnect structure along with the equivalent circuit [33] for an isolated single-walled carbon nanotube (SWCNT) of length less than the mean free path of electrons in a CNT (λ_{CNT}) which is typically > *1μm*. Due to spin degeneracy and sub-lattice degeneracy of electrons in graphene, each nanotube has four 1-D conducting channels in parallel. Hence, the maximum conductance of an isolated ballistic single-walled CNT (SWCNT) assuming perfect contacts, given by the Landauer-Buttiker formula, is $4e^2/h = 155\ \mu S$ [11]. In other words, the resistance of a carbon nanotube of length $L < \lambda_{CNT}$ with ideal coupling to the two metal contacts at its ends is given by [34]:

$$R_{CNT} = R_F = \frac{h}{4e^2} \approx 6.45K\Omega \tag{1}$$

where h is Planck's constant and e is electron charge. For lengths greater than the mean free path $L > \lambda_{CNT}$, scattering leads to an additional ohmic resistance of $(h/4e^2)L/\lambda_{CNT}$ [35], which yields a per unit length resistance of:

$$R_{CNT}(p.u.l.) = \left(\frac{h}{4e^2}\right)\frac{1}{\lambda_{CNT}} = \frac{R_F}{\lambda_{CNT}} \tag{2}$$

Moreover, in practice, the two metal-CNT contacts are never ideal, leading to an additional imperfect contact resistance (R_c) which can be as high as 100 *KΩ* [17]. It must be noted that although the current through a CNT saturates at high electrical fields, the voltage bias across an interconnect is low, and in this case, CNTs demonstrate excellent ohmic behavior.

3.1.2 CNT Capacitance

The capacitance of a CNT arises from two sources. The *electrostatic capacitance* (C_E) is calculated by treating the CNT as a thin wire, with diameter '*d*', placed a distance '*y*' away from a ground plane, and is given by the formula in Equation 3 (C_E per unit length) [33] for *y>2d*. The quantities *y* and *d* are shown in **Fig. 6**. For *d=1 nm*, *y=1 μm*, $C_E \approx 30$ aF/um. This is the intrinsic plate capacitance of an isolated CNT.

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{3}$$

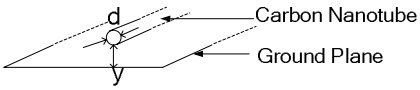

Fig. 6. Isolated conductor, with diameter 'd', over a ground plane at a distance 'y' below it.

The *quantum capacitance* (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Quantum capacitance is used to model the energy needed to add an electron at an available quantum state above the Fermi level. By equating this energy to that of an effective capacitance, the expression for the quantum capacitance (per unit length) is obtained as shown in Equation 4 [33], where h is the Planck's constant and v_F is the Fermi velocity.

$$C_Q = \frac{2e^2}{hv_F} \tag{4}$$

For a carbon nanotube ($v_F \approx 8\text{x}10^5$m/s), $C_Q \approx 100$aF/um [33]. Since a CNT has four conducting channels as described in the previous sub-section, the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$. The same effective charge resides on both these capacitances (C_E and $4C_Q$) when the CNT carries current, as is true for any two capacitances in series. Hence these capacitances appear in series in the effective circuit model.

3.1.3 CNT Inductance

The inductance associated with an isolated SWCNT can be calculated from the magnetic field of an isolated current carrying wire some distance away from a ground plane, as depicted in **Fig. 6**. In addition to this *magnetic inductance* (L_M), the *kinetic inductance* is calculated in [33] (following [36]) by equating the kinetic energy stored in each conducting channel of the CNT to that of an equivalent inductance (see **Fig. 7**). The four parallel conducting channels in a CNT give rise to an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are shown in Equation 5 below.

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right)$$
$$L_K = \frac{h}{2e^2 v_F} \tag{5}$$

For *d=1 nm* and *y=1 um*, L_M (per unit length) evaluates to ≈1.4 pH/um. On the other hand, L_K (per unit length) for a CNT evaluates to 16 nH/um.

It is important to note that although the kinetic inductance term L_K has been included in most works modeling CNT interconnects [27-31], this term had been derived originally in [36] assuming no voltage drop along the nanotube. Furthermore, experimental results in [10, 37] as well as theoretical studies in [38, 39] show that potential drop does exist along the nanotube length. Hence, when calculating interconnect delay using the equivalent circuit model for a CNT, the kinetic inductance term is valid only in the case where $L < \lambda_{CNT}$; i.e, under ballistic conduction--when there is no potential

drop along the length of the nanotube. As such, for nanotube lengths $L >> \lambda_{CNT}$, the inclusion of L_K may lead to significant errors in delay (since $L_K >> L_M$). Experimental studies on the high frequency characteristics of carbon nanotubes [40] have also shown that the large inductive effects expected due to L_K are not observed up to frequencies as high as 10 GHz.

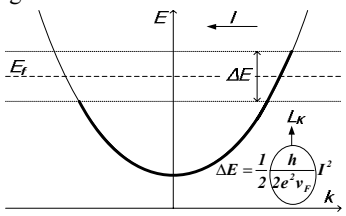

Fig. 7. Kinetic inductance in nanotubes of length less than mean free path arises from the kinetic energy stored in the electrons carrying current. E_f denots the Fermi level. The energy ΔE is the extra energy gained by the right moving ($k>0$) electrons in order to have a net flow of current (I).

3.2 Equivalent Circuit for CNT Bundles

The equivalent circuit parameters for a CNT bundle are shown in Eqs. (i)-(vi) (**Fig. 5**) [5, 32]. It is assumed that the n_{CNT} metallic nanotubes forming a bundle carry current independent of each other (as a large tunneling resistance ~MΩ exists between adjacent CNTs [41]). The presence of semi-conducting CNTs (which do not contribute to current conduction) and low packing density of metallic CNTs can be accounted for by considering a "sparsely populated" bundle. Electrostatic coupling capacitance between CNTs forming a bundle does not come into play as the CNTs are assumed to carry simultaneous and identical currents. Hence the electrostatic capacitance arises mainly from the interaction between each CNT near the edge of the bundle and the neighboring interconnects (assumed to be at ground potential). The expression for C_E^{bundle} (Eq. (vi), **Fig. 5**) is obtained empirically by using an electromagnetic field solver. Details of this capacitance model can be found in [32].

A dense CNT bundle local interconnect with ideal metal-nanotube contacts has resistance much lower than that of a Cu interconnect of identical dimensions [32]. With typical imperfect metal-nanotube contacts, resistance is higher than that of a Cu interconnect. This is because, for small lengths (L), especially for $L < \lambda_{CNT}$, the large contact resistance dominates the overall CNT resistance. However, for long interconnect lengths (global wires), the impact of imperfect contacts diminishes, because R_c is a constant resistance unlike the scattering resistance along the nanotube which increases linearly with length. Hence long CNT bundle interconnects will have smaller resistance than their Cu counterparts [32].

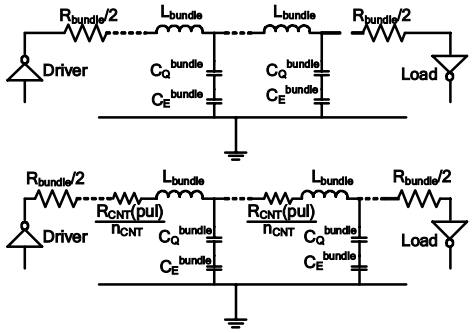

Fig. 8. Equivalent circuit diagram for CNT bundle interconnects of length (a) $L< \lambda_{CNT}$ with $L_{bundle}=(L_M+L_K/4)/n_{CNT}$ and (b) $L>>\lambda_{CNT}$ with $L_{bundle}=L_M/n_{CNT}$.

Since the CNTs are cylindrical, the surface area of the CNTs at the edge of a bundle exposed to the surrounding interconnects (and contributing to electrostatic capacitance) is larger than the corresponding surface area for a Cu interconnect with straight edges. Hence the electrostatic capacitance of such a CNT bundle is larger than that of a Cu interconnect of equivalent dimension [32]. It is found that in the case of all the scenarios considered in [5, 32], distributed RC models (**Fig. 8**) suffice since the effective inductance is small.

This is equivalent to saying that the RC charge-up time for these interconnects is larger than the wave propagation time. Using this delay model (along with driver parasitics and interconnect dimensions as predicted by the ITRS'04), the performance of CNT bundle interconnects, as compared to Cu interconnects of identical dimensions, is outlined in the following section.

It is important to realize that we have so far assumed non-interacting tubes since very little is known about the nature of the electromagnetic interactions in dense CNT bundles. Although one knows that SWCNTs are not isolated from each other but are attracted and glued to each other by Van der Waals forces, the consequences of this for the density of states, conductivity, etc are not known. While the high frequency properties of individual nanotubes as well as capacitive interactions between adjacent nanotubes in a flat array have been studied [42, 43], there is no experimental work or theoretical analysis yet about the nature of electromagnetic interactions between non-isolated (or tangled) nanotubes. Hence the existence of any mutual inductance or capacitance terms between SWCNTs in a CNT bundle is a question that merits rigorous investigation before these effects can be included in the equivalent circuit model.

4. Analysis of CNT Bundles vs Copper

4.1 Performance Analysis

At the local interconnect level, delay is largely impacted by interconnect capacitance because of the large driver resistances and small load capacitances. Hence, CNT bundle *local* interconnects have larger delay than Cu (**Fig. 9(a)**) due to their larger capacitance. However, delay of long length (intermediate and global level) interconnects is largely impacted by interconnect resistance since large drivers (large load capacitance and small driver resistance) are used to drive these interconnects. Hence, CNT bundle interconnects can reduce intermediate level interconnect delay by more than 60% (**Fig. 9(b)**) due to their lower resistance, in spite of imperfect metal-nanotube contacts.

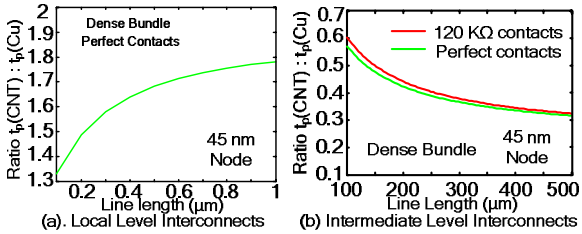

Fig. 9. Ratio of CNT bundle interconnect delay (assuming $\lambda_{CNT} = 1\ \mu m$ [10]) to that of Cu interconnect of same dimensions at **(a)** local and **(b)** intermediate levels.

Global interconnects are often designed by inserting buffers (repeaters) to drive signals faster. Classical buffer insertion is done by minimizing delay per unit length (τ/l). **Fig. 10** shows that the optimal delay per unit length $(\tau/l)_{opt}$ with optimally buffered CNT bundle interconnects is lower than that with Cu (20% less for $\lambda_{CNT} = 1\ \mu m$ and as much as 70% less for $\lambda_{CNT} = 10\ \mu m$, at 22 nm node) and decreases as technology scales (inset).

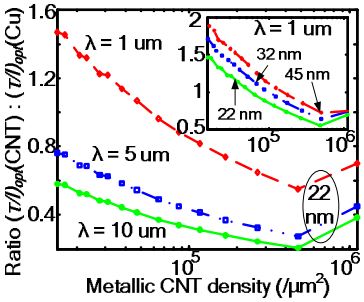

Fig. 10. Ratio of optimal delay per unit length for buffered CNT bundle global interconnect to that of Cu, as a function of density of metallic CNTs in the bundle: for different mean free paths (λ) at 22 nm node (main figure) and at different technology nodes (inset).

4.2 Power Analysis

For the buffered global interconnect with optimal delay, repeater power dissipation per unit length with CNT bundle interconnects is comparable to that with Cu for maximum metallic CNT density (**Fig. 11(a)**). In other words, global interconnect delay can be reduced considerably by using densely packed CNT bundle interconnects without incurring additional large power dissipation. Moreover, it is known that large power savings can be achieved by incurring a small delay penalty using sub-optimally buffered global interconnects with Cu [44]. Similar power optimal buffer insertion can be applied to CNT bundle interconnects as well (leading to > 20% power saving for 5% delay penalty at 45 nm node), as shown in **Fig. 11(b)** [5]. The % saving in power increases as technology scales (consistent with the trend for Cu [44]).

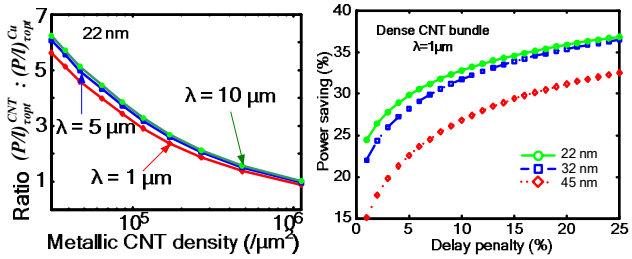

Fig. 11. (a) Ratio of repeater power dissipation per unit length for optimally buffered CNT-bundle global interconnect to that of Cu, as a function of metallic CNT density and for different mean free path lengths (λ_{CNT}). **(b)** Percent saving in repeater power dissipation per unit length for "power-optimal" buffer inserted CNT-bundle global interconnect as a function of delay penalty (% of $(\tau/l)_{opt}$).

4.3 Reliability and Thermal Analysis

Due to strong sp^2 bonding (like graphite), carbon nanotubes are much less susceptible to electromigration (EM) problems that plague copper interconnects and can carry very high current densities [12]. Metallic single-walled CNT bundles have been shown to be able to carry extremely high current densities of the order of 10^9 A/cm^2 [45]. Cu interconnects, on the other hand, have a current carrying capacity of ~10^6 A/cm^2 due to EM [46]. A 100 nm x 50 nm cross-section Cu interconnect can carry current up to 50 μA, whereas a 1 nm diameter CNT can carry upto 20-25 uA current [37]. Hence, from a reliability perspective, a few CNTs are enough to match the current carrying capacity of a typical Cu interconnect. However, the need to reduce interconnect resistance (and hence delay) makes it necessary to pack several thousands of CNTs in a bundle [5].

As mentioned earlier, at nanometer scale dimensions, increasing Cu interconnect resistivity (due to enhanced surface and grain boundary scattering) in addition to increasing current density (J) results in higher self-heating of interconnects. Moreover, low-k dielectrics with inherently lower thermal conductivity ($K_{th,ILD}$<*0.4 W/mK*) make heat conduction from interconnect layers to the heat sink difficult. Hence, even though vias and interconnects, which have higher thermal conductivity ($K_{th,Cu}$=*385 W/mK*), improve the effective thermal conductivity of the back-end, metal temperature (T_m) rises significantly above the junction temperature especially at the topmost interconnect layers [6]. All these factors adversely affect EM lifetime of Cu interconnects which depends quadratically on J and exponentially on T_m.

Estimations based on measured thermal conductivity (K_{th}) of mats of SWCNT bundles, combined with observations from electrical conductivity experiments, predict K_{th} for an SWCNT bundle in the range *1750-5800 W/mK* [13] at room temperature, while $K_{th,Cu}$=*385 W/mK*. This high value of $K_{th,CNT}$ is in the direction along the length of nanotubes (since thermal conductivity in CNT bundles is anisotropic [47] - see **Fig. 12**). Hence vias composed of CNT bundles will serve as more effective heat conduits than Cu vias and can potentially reduce the temperature gradient at the back-end.

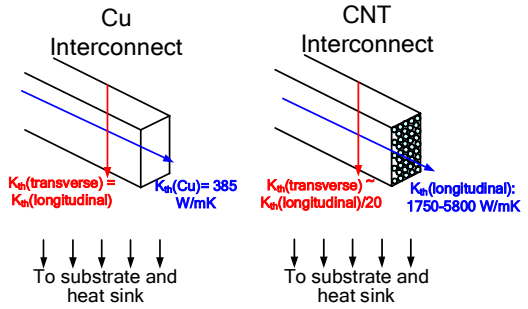

Fig. 12. Schematic showing heat conduction paths and thermal conductivity values in Cu and CNT bundle interconnects. For CNT bundles thermal conductivity is anisotropic and $K_{th,CNT}$ > 1750 W/mK along the length of the CNTs [47].

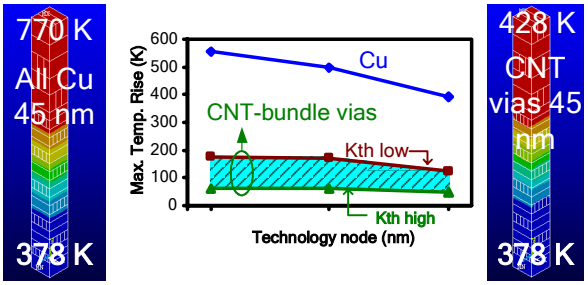

Fig. 13. Maximum temperature rise for Cu interconnects and vias vs CNT bundle vias integrated with Cu interconnects. For CNT bundles, the shaded region shows the range 1750 W/mK < K_{th} < 5800 W/mK [13]. Reference (substrate) temperature = 378 K.

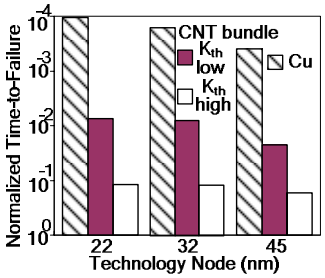

Fig. 14. Cu interconnect electromigration (EM) lifetimes as a result of high interconnect temperatures normalized to EM lifetime at reference temperature (378 K), when vias are composed of Cu and CNT bundles respectively.

5. Hybrid CNT/Cu Interconnects

The properties of CNTs described in the previous sub-section can be used to the advantage of even prevalent copper interconnect technology by hybridization of CNT vias forming vertical

interconnections between Cu metal layers. **Fig. 13** shows that even when CNT bundles are used *only as vias* integrated with Cu interconnects, maximum interconnect temperature rise is much smaller [5]. **Fig. 14** shows that the lower interconnect temperatures in hybrid CNT/Cu structures can lead to two orders of magnitude improvement in the EM mean-time-to-failure of Cu global interconnects. The Cu wire delay also improves by 30% [5].

6. CONCLUSIONS

In conclusion, applicability of CNTs in future VLSI interconnect applications has been examined. While the outstanding intrinsic properties of metallic single-walled CNTs in conjunction with encouraging performance, power and thermal/reliability analysis results of CNT bundles provide strong impetus for further investments in CNT interconnect research, several challenges remain to be overcome in the areas of fabrication and process integration. Although these challenges are not expected to cause any fundamental problems, LSI compatible low thermal-budget ($<400^0$C) dense single-walled CNT bundle technology is necessary for interconnect applications. Also, lowering of metal-nanotube contact resistance will be vital, especially for local interconnect and via applications. Moreover, rigorous characterization and modeling of: electromagnetic interactions in CNT bundles, 3-D (metal) to 1-D (CNT) contact resistance, impact of defects on electrical and thermal transport and high-frequency effects will be equally important.

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