Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation

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Abstract

We present a simulation-based analysis of device design at the 25 nm channel length generation. Double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's are considered. Dependencies of short-channel effects on channel thickness and ground-plane bias are illustrated. Two-dimensional field effects in the gate insulator (high k) and the buried insulator (low k) in single-gate SOI are studied.

Introduction

Experimental demonstration of working MOSFET's at the 25 nm channel length CMOS generation is currently being undertaken at several laboratories [1-3]. While the double-gate MOSFET is considered the most promising candidate for CMOS scaled to the ultimate limit of 20-30 nm channel lengths [4-6], device structures (Fig. 1) such as the ground-plane MOSFET and ultra-thin single-gated SOI, and even bulk CMOS [7], have also been proposed as candidates.

Previous work [4-5,8] has already identified basic device design considerations. In this paper, we examine in more detail the design trade-off's among double-gate, ground-plane, and ultra-thin SOI MOSFET's at the 25 nm channel length CMOS technology generation. Taking note of the recent advances in thin (< 1.5 nm) gate oxide growth [2,9-10] and high dielectric constant gate insulators [11] as well as silicon channel thickness uniformity control [1], we explore the design space for equivalent gate oxide thickness (t_{eq}) and silicon channel thickness (t_{Si}) further than previous work [4-5]. Effects such as source/drain extension series resistance, 2-D field effects in high k gate insulators and low k buried insulators, and the dependencies of threshold voltages and short-channel effects on channel thickness and ground-plane bias, which were ignored in previous analyses [4-5], are investigated in this work using device modeling tools.

Modeling Approach

We examine mainly electrostatic design issues with the n-MOSFET (Fig. 1) biased in the subthreshold regime at 300K. A drift-diffusion simulator (FIELDAY [12-14]) is suited for such purposes. We explore equivalent gate oxide thickness (t_{eq}) of 1.5 nm and 1 nm, since these thickness appear to be at the limits of conventional SiO_2 and insulators with a high dielectric constant (high k), respectively. Silicon channel thickness (t_{Si}) spans from 25 - 1.5 nm, which obviously exceeds present manufacturing capability but is informative to explore. The silicon channels are undoped to avoid threshold voltage fluctuation due to discrete, random dopant placement [15]. Gate material is assumed to have a mid-gap workfunction in this work.

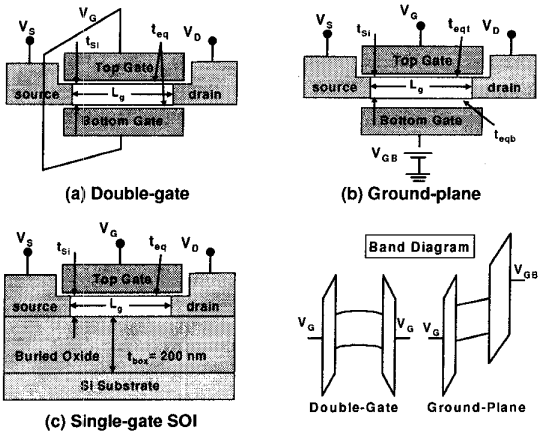

Figure 1 (a) Double-gate, (b) ground-plane, (c) single-gated SOI MOSFET. Gate material work-function is set at the mid-gap of the silicon band-gap. On-chip biasing of the ground-plane is assumed. The source/drain junction is abrupt. The channel length (L_g) is the metallurgical channel length.

Results

Double-gate: Figs. 2-3 show the threshold voltage roll-off (ΔV_{TH}) and drain-induced barrier lowering (DIBL) of double-gate for t_{eq} of 1 nm and 1.5 nm with t_{Si} from 5-25 nm. Short-channel effect control is acceptable for 25 nm (worse case) channel length using (a) t_{eq}=1.0 nm and t_{Si}=10 nm or (b) t_{eq}=1.5 nm and t_{Si}=5 nm, and for 20 nm (worse case) channel length using (c) t_{eq}=1.0 nm and t_{Si}=5 nm. Use of t_{eq}=1.5 nm in (a) & (c) appears marginal.

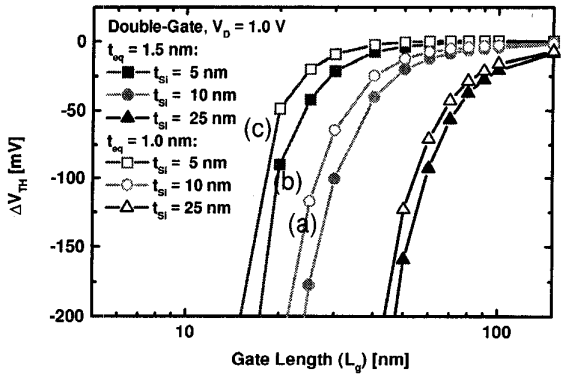

Figure 2 Threshold voltage roll-off for double-gate with t_{eq} = 1.5 nm and 1.0 nm.

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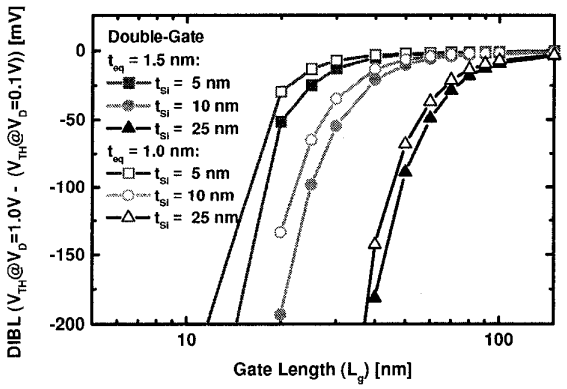

Figure 3 DIBL for double-gate with t_{eq} = 1.5 nm and 1.0 nm.

Single-gated ultra-thin SOI: Fig. 4 compares the V_{TH} roll-off for double-gate and single-gated SOI. Single-gated ultra-thin SOI with an undoped channel does not have the required short-channel control even for ultra thin t_{Si} (~1.5 nm). Doping the ultra-thin channel uniformly does not improve short channel behavior and only serves to shift the V_{TH}.

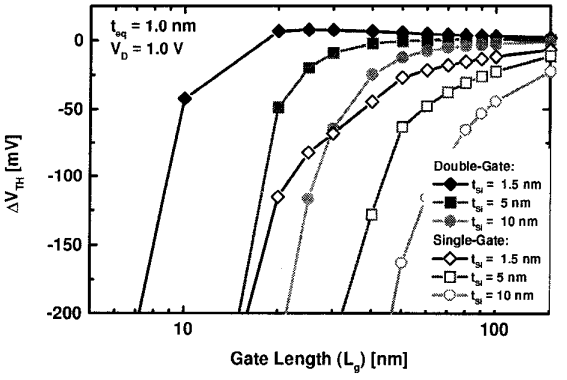

Figure 4 Threshold voltage roll-off for double-gate and single-gated MOSFET. Single-gate SOI will not meet short-channel effect requirements.

Ground-plane: The ground-plane MOSFET is similar to the double-gate MOSFET electrostatically, and yet has the extra flexibility of tuning the threshold voltage by means of the bottom gate bias (V_{gb}) [16]. The bottom gate of a ground-plane MOSFET is biased dynamically depending on circuit activity. The bottom gate insulator should be somewhat thicker than the top gate insulator to reduce drain-to-bottom-gate capacitance. Yet, this bottom gate insulator must be kept thin to allow effective tuning of the threshold voltage by a bottom gate bias not exceeding the power supply voltage. We choose a ratio of 1.5 times the top gate insulator thickness. Figs. 5-6 compare the V_{TH} roll-off and inverse subthreshold slope (S-factor) of ground-plane and double-gate MOSFET. The short-channel behavior of ground-plane and double-gate are similar (Figs. 5-6) as expected, with ground-plane being slight worse due to the thicker bottom gate oxide. The larger S-factor of the ground-plane MOSFET is mitigated by the adjustable V_{TH}.

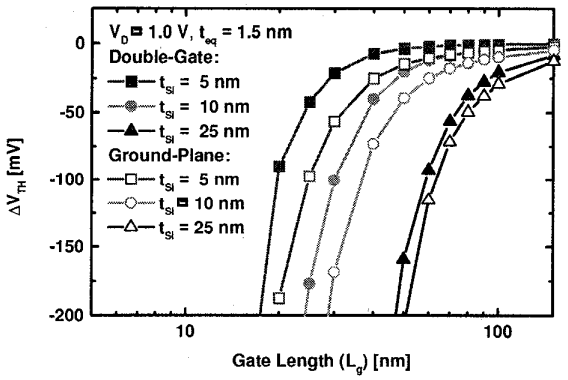

Figure 5 Threshold voltage roll-off for ground-plane and double-gate MOSFET is similar. Bottom gate insulator for ground-plane is 2.25 nm.

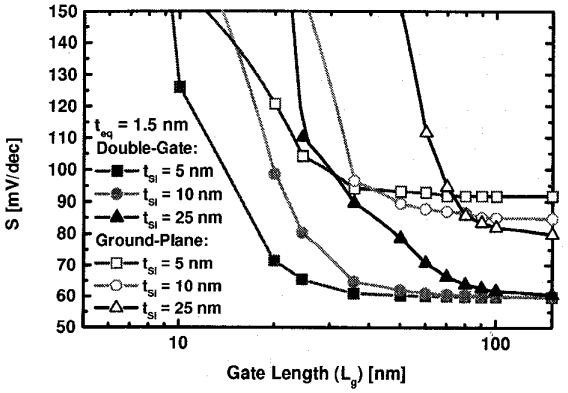

Figure 6 The S-factor of ground-plane is ~ 20 - 30mV/dec worse than double-gate. The fixed bottom gate potential results in a capacitor divider, reducing the control of top channel potential by the top gate. Bottom gate insulator for ground-plane is 2.25 nm.

The range over which the threshold voltage can be tuned by biasing the bottom gate is shown in Fig. 7. The slope change at V_{gb} > 0.25V results from inversion of the bottom channel which also leads to degradation of the subthreshold slope. This effectively limits the V_{TH} tuning range to V_{gb} < 0.25V. The threshold voltage dependence on silicon channel thickness (Fig. 8) for ground plane is larger than for double-gate. This is because the fixed bottom gate bias requires a larger top gate bias to achieve the same top channel surface potential for a smaller t_{Si}, due to a capacitor divider effect. The dependence of V_{TH} on channel thickness for ground plane MOSFET is increasingly larger for larger bottom gate reverse bias (see Fig. 7). The small increase of V_{TH} with decreasing t_{Si} is due to the use of a fixed current as the definition of threshold.

Effect of silicon channel thickness: Fig. 8 also shows the estimated threshold voltage shift due to quantum confinement in a thin silicon channel. The estimation assumes a simple 1-D particle in a box confinement. The V_{TH} shift due to QM confinement becomes too large below t_{Si}=2 nm and increases quadratically (ΔV_{TH} = - $(h^2/4qm^* t_{Si}^2)(\Delta t_{Si}/t_{Si})$) for a fixed

$\Delta t_{Si}/t_{Si}$ tolerance. To illustrate the short-channel effect reduction with t_{Si}, the DIBL vs. t_{Si} is shown for double-gate (Fig. 9). Ground plane exhibits a similar behavior with additional dependence on the bottom gate bias (Fig. 10). For very thin channels, the series resistance of the source/drain extension region overlapped by the gate may not be ignored, especially for source/drain with moderate active doping concentrations (Fig. 11). At t_{Si} = 5 nm, the additional resistance is small compared to the contact resistance.

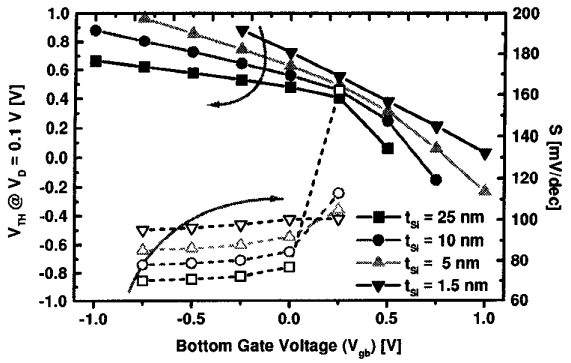

Figure 7 Range of threshold voltage tunable by biasing the bottom gate of a ground-plane MOSFET (left axis). The slope change at high V_{gb} results from inversion of the bottom channel. This is also reflected in the subthreshold slope degradation at high V_{gb} (right axis). This effectively limits the V_{TH} tuning range to $V_{gb} < 0.25$V.

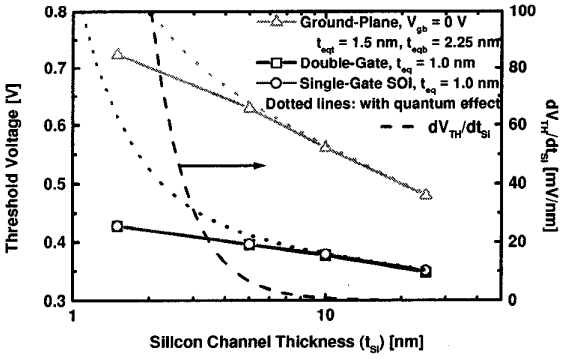

Figure 8 Left axis: Dependence of the threshold voltage (long channel, without QM effects) on the silicon channel thickness is larger for ground-plane because of capacitor divider effect. The estimated additional shift of the threshold voltage due to quantum confinement of the thin silicon channel is shown as dotted lines. Right axis: The sensitivity of V_{TH} to t_{Si} (dV_{TH}/dt_{Si}) due to quantum effect.

Threshold Voltage: The threshold voltage (Fig. 7 - 8) using a mid-gap workfunction gate material may not be optimal for certain applications. For double-gate with t_{Si}=5 nm, t_{eq}=1.5 nm, $\Delta V_{TH} / \Delta(N_A\text{-}N_D) \cong 0.22\times10^{-19}\ Vcm^3$ if the channel is doped uniformly with a net doping of $(N_A\text{-}N_D)$ (positive for p-type). For an n-channel V_{TH} to be around 0.25 V, the channel doping should be about $2.5\times10^{19}\ cm^{-3}$ (p-type) for n^+-poly gate, and $3\times10^{18}\ cm^{-3}$ (n-type) for a mid-gap metal gate. The V_{TH} for ground-plane in Fig. 7 is too high for some applications. For ground-plane, a suitable gate workfunction is n^+-poly (for n-channel) for the front gate and use a reverse bias on the bottom gate to tune (raise) the threshold voltage. This scheme allows a larger tuning range and improves DIBL since DIBL decreases with increasing reverse bias (Fig. 10).

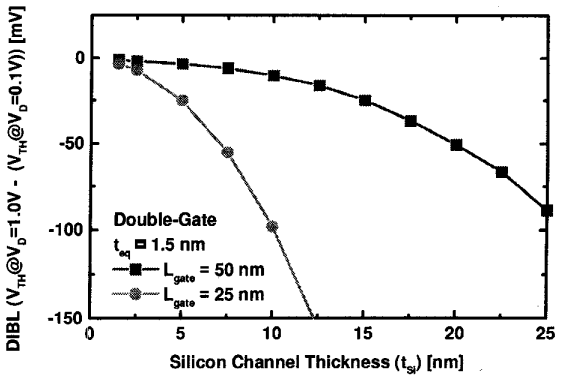

Figure 9 DIBL decreases with t_{Si}. The relation is not linear in accordance with analytical theory [16].

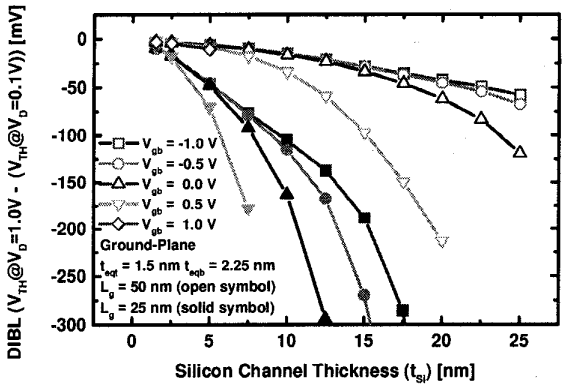

Figure 10 DIBL vs silicon channel thickness for various V_{gb}. DIBL decreases with increasing bottom gate reverse bias and decreasing t_{Si}. DIBL degrades when the positive bottom gate bias inverts the back channel.

Effect of insulator dielectric constant: The vertical component of the electric field is smaller (larger) for higher (lower) dielectric constant gate (buried) insulators because the vertical displacement (**D** field) is continuous across the silicon/insulator boundary. Consequently, the benefits of very high k insulators with a large physical thickness are limited [17] due to 2-D field effects at the gate insulator (Fig 12). In general, for each t_{Si} and t_{eq} combination, there is a maximum value of k before 2-D effects at the gate insulator begin to degrade the short-channel behavior. On the other hand, a low dielectric constant for the buried insulator of the single-gated SOI improves short-channel behavior (Fig. 13). This improvement results from reduced drain field penetration to the source via the buried oxide [18].

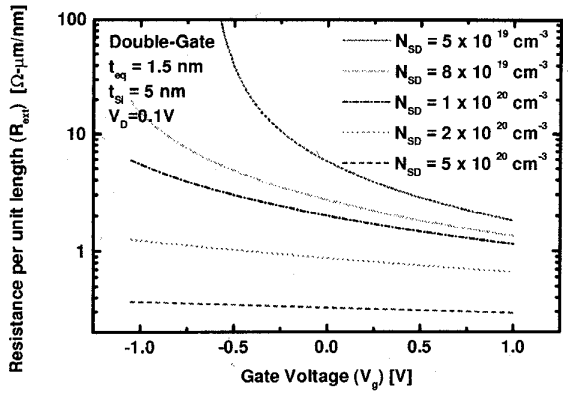

Figure 11 Series resistance per unit length of the source/drain extension region vs. the gate bias (n-FET) for various source/drain dopings (N_{SD}). At large reverse gate biases, a substantial fraction of the thin silicon channel is depleted and the resistance is non-negligible.

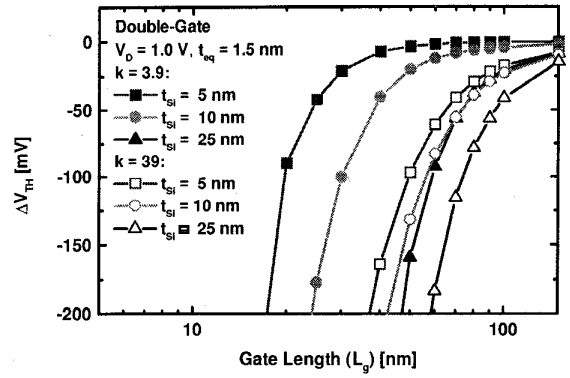

Figure 12 V_{TH} roll-off for a gate insulator with 10 times the physical thickness (k=39) is much worse for the same equivalent gate oxide thickness (t_{eq}) due to 2-D effects in the gate insulator.

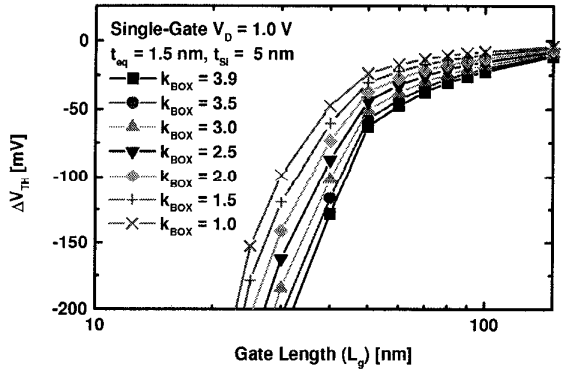

Figure 13 V_{TH} roll off for a single-gated ultra-thin SOI MOSFET with dielectric constant of the buried insulator (k_{BOX}) varied from 3.9 (SiO_2) to a theoretical minimum of 1.0 (vacuum).

Summary

We present a simulation-based analysis of device design at the 25 nm channel length generation. Double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's are considered. Our analyses show that despite the increased channel potential control offered by ultra-thin silicon channel, single-gated SOI MOSFET with an undoped or uniformly doped channel does not provide adequate short-channel immunity for 25 nm channel length devices. Both double-gate and ground-plane can meet the electrostatic design requirements. Ground-plane MOSFET's offer the flexibility of actively tuning the threshold voltage to reduce power consumption. Ground-plane MOSFET's also have stronger dependencies of the V_{TH} on the channel thickness and the tuning range is limited except for very thin t_{Si} ($\leqslant$ 5 nm). Dependence of short-channel effects on channel thickness is illustrated. Although the use of a very thin active silicon eliminates the need for shallow source/drain junctions, the need for a sharp lateral junction profile remains, and is expected to be similar to that required for bulk CMOS designs (< 4 - 5 nm/dec) [7]. 2-D field effects in the gate insulator limit high k insulator with physical thickness comparable to the silicon channel thickness while low k buried insulator for single-gated SOI improves short channel behavior.

Acknowledgments

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