Gate Leakage

- Increases with gate oxide (SiO2) scaling
- High-k gate oxides can be used to lower gate leakage
- Independent of temperature
Avalanche Breakdown

• Due to scaling, high-velocity electrons can impact the drain, dislodging holes—Called impact ionization
• Holes are swept towards grounded substrate → cause substrate current
• Also affects long-term reliability
• This is another factor which limits the process scaling → voltage must scale down as length scales
S/D Engineering in the Scaled Regime

- Scaling of S/D extension (SDE) depth and gate overlap
- Junction depth in 0.25 um technology node is 50-100 nm.

- Heavy doping needed for the S/D contact and for lowering the sheet resistance
- Lightly doped region to lower electric field and prevent hot-electrons
S/D Engineering

- Shallow junctions lead to high external resistance (sheet resistance is higher)
- Shallow junction improves the short channel characteristics by reducing the amount of charge controlled by the drain (note that gate has less control in regions further from the oxide/Si interface)
S/D Engineering

- Reducing SDE-to-gate overlap causes current to spread out into a lower doping location of SDE leading to higher resistance.
- By varying the thickness of the offset spacer, the SDE-to-gate overlap and vertical junction depth can be independently varied.
Channel Engineering

• Modifying doping profile in the channel:
  – Retrograde doping (for better electrostatics — well region has lower drain control; and to prevent punchthrough, since depletion width is smaller)
  – Halo doping (increases junction abruptness—good for electrostatics and preventing punchthrough)
$V_{cc}$ and $V_{th}$ Scaling

- To keep the gate overdrive ($V_{cc} - V_{th}$) high, the $V_{th}$ must be scaled.
- However, lowering $V_{th}$ at low gate lengths leads to high leakage.

![Graph showing $V_{cc}/V_T$ vs $L_{GATE}$](image)
Alternative Options in the Ultra-Scaled Regime

- Dual-Vth Architecture
- SOI
- FINFET
- Dynamic-Vth device
- High-k gate oxide
- Strained device
- Steep subthreshold slope devices
## Alternative Oxides

<table>
<thead>
<tr>
<th>OPTION</th>
<th>ISSUES / STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si$_3$N$_4$ / nitride</td>
<td>Small advantage especially with buffer layer (G. Lucovsky, T. P. Ma)</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>Need SiO$_2$ buffer/ no poly-silicon gate</td>
</tr>
<tr>
<td></td>
<td>Very early stages (S. Kamiyama)</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>Need SiO$_2$ buffer/ no poly-silicon gate</td>
</tr>
<tr>
<td></td>
<td>Very early stages (S. A. Campbell)</td>
</tr>
<tr>
<td>BST</td>
<td>Deep states/ buffer layer/ no poly-silicon gate</td>
</tr>
<tr>
<td></td>
<td>Early stages FET (large DRAM interest)</td>
</tr>
</tbody>
</table>
Gate Oxide Scaling Issues

- Currently, gate dielectric approaching thickness of a few atoms
  - Problem: Quantum Mechanics
  - Electron tunneling $\rightarrow$ gate current leakage
- With the number of transistors on a single chip growing exponentially, power dissipation becomes a big problem.
Problem with SiO$_2$

- SiO$_2$ layer is too thin.
  - 90nm node has a dielectric thickness of 1.2nm.
- Low relative dielectric constant.
- If there is to be any increase in performance, an alternative must be found.
Solution: High-K Dielectric

• Options:
  – Increase dielectric thickness.
  – Increase relative dielectric constant.

• High-k dielectrics are a logical solution.
Solution: High-K Dielectric

- Problems with high-k/poly-si:
  - Increased threshold voltage

Image courtesy of Intel.
Solution: High-K Dielectric

• Problems with high-k/poly-si:
  – Increased threshold voltage
  – Decreased channel mobility

Image courtesy of Intel.
Solution: High-K Dielectric

- Replace poly-si gates with doped, metal gates.
  - Improved mobility.
Introduction of High-k Dielectrics

- Polysilicon gate on high-k dielectric results in:
  1. Threshold voltage pinning: difficulty in adjusting $V_{th}$
  2. Phonon scattering: reduced carrier mobility

Solution is to replace polysilicon with metal gate
Integrating High K Dielectrics with Metal Gate Electrodes

- Replace poly Si with a metal gate whose work function minimizes Fermi level pinning
- Different metals are required for NMOS and PMOS

R. Chan, AVS 5th International Conference on Microelectronics and Interfaces, Santa Clara, California, March 1, 2004.
High-k/Metal Gate Technology

- High-k/metal gate devices offer lower gate leakage with small increase in gate capacitance.

Source: Intel
High-K Dielectric Performance

- Performance with high-k dielectric and metal gate:
Manufacturing Process

- Several types of high-k dielectric: HfO$_2$, ZrO$_2$, TiO$_2$.
- Chemical vapor deposition:
Summary for High-k Gate Oxide

• As transistors shrink in size, an alternative to SiO$_2$ must be found.
• HfO$_2$, in conjunction with metal gates, improves leakage current, gate capacitance, and speed.
• By replacing SiO$_2$ with HfO$_2$, transistors will be able to continue to shrink without sacrificing performance.
Strained Silicon MOSFET

- Silicon in channel region is strained in two dimensions by placing a Si-Ge layer underneath (or more recently adjacent to) the device layer.
- Strained Si results in changes in the energy band structure of conduction and valence band, reducing lattice scattering.
- Benefit: increased carrier mobility, increased drive current (drain current).
SOI and FINFET Devices
basic structures

Partially depleted (PD) body
(similar to bulk MOSFET but the body floats)
basic structures

deployment region

Front gate (Gf)

Thin body

FOX S B D FOX

BOX

Substrate (Gb)

Fully depleted (FD) body
Partially Depleted vs. Fully-Depleted

- Recall that depletion region empty of free carriers forms in the BULK beneath the gate
- Partially-depleted SOI
  - The body is thicker than the depletion region, so bulk voltage can vary depending on the amount of charge present
  - **This varying charge changes Vt because of the body effect**
- Fully-depleted SOI
  - Body is thin, depletion region spans bulk
  - Body charge is fixed, body voltage does not change
  - Harder to make because of thin body
Another View

Source: Weste/Harris
benefits of SOI

- Simple IC processing (isolation)
- Higher density
- Reduced S/D junction capacitance (speed/power)
- Low soft-error rate
- No latch-up
- No (normal) body effect
benefits of SOI

Parasitic bipolar devices → “latchup”
Transient currents flowing in substrate during startup can cause VSUB to rise, turning on Vsub. This will turn on Vwell, which turns on Vsub harder in a positive feedback loop, causing large current to flow between Vdd/GND (destructive current!).

Keep Rwell, Rsub low, also place numerous well taps to collect stray charge.
benefits of SOI

No parasitic bipolar devices → no latchup
soft errors in bulk CMOS

alpha particles

Vdd

input

output

Vss

N-well

P-substrate

Alpha particles

“soft” errors
Alpha Particles

- **Sources**
  - Cosmic Rays (aircraft electronics vulnerable)
  - Decaying uranium and thorium impurities in integrated circuit interconnect

- **Generates electron-hole pairs in substrate**
  - Excess carriers collected by diffusion terminals of transistors
  - Can cause upset of state nodes – floating nodes, DRAM cells most vulnerable
soft errors in SOI

Not as much substrate to generate charge in!

Low soft error rate
layout for bulk CMOS

n-well
layout for SOI

Vdd

P+

N+

Vss

Simpler isolation  simpler process  smaller layout
Another subtle advantage: Lower $V_t$

- In bulk-CMOS, $V_t$ varies with channel length
  - variations in polysilicon etching shows up as variations in threshold voltages
  - $V_t$ must be high enough in the worst case (lowest $V_t$) to limit subthreshold leakage, so nominal threshold must be higher
- SOI has lower $V_t$ variations than bulk-CMOS
  - So nominal $V_t$ can be lower, resulting in faster circuits, esp. for lower $V_{DD}$
SOI Disadvantages

- **Floating body** causes the *History Effect*
  - Body voltage depends on if device has been idle or switching
  - This changes $V_t$, which changes the delay of the circuit
  - Circuit delay changes with its “history” of switching activity!
  - Matches matching transistors for analog designs difficult because even if transistors are next to each other, can have different characteristics because of changing $V_t$

- **Self-heating**
  - The oxide is good thermal insulator as well as electrical insulator
  - Heat accumulates in switching transistors rather than spreading throughout the substrate, slow them down.
  - A problem for large transistors that switch fast, i.e., clock buffer transistors.
Why Multi-Gate SOI MOSFETs?

- Higher current drive ⇒ better performance
- Prophesized to show higher tolerance to scaling
- Better integration feasibility, raised source-drain structure, ease in integration
- Larger number of parameters to tailor device performance
What does FinFet look like?

Fig. 1. Schematic of a FinFET structure.

3D view of multi-fin FinFET
UC Berkeley Results – FinFET/ Double Gate (2000-04)

Gate Length = 30nm, Oxide thickness = 2.1nm

Gate Length = 30nm, Fin Width = 20nm

Gate Length = 20nm
INTEL’s TriGate SOI (SSDM 2002)

Highest ever performance reported for NMOS and PMOS devices on a single substrate !!
TSMC’s $\Omega$-gate Device (SSDM-2002)
Multi-Body Single-Gate Devices

- Multi-Body Single gate devices - an attractive option.
- Increased current drive using a single gate.
- Total current nearly equals the current thru one body multiplied by the number of body regions.
- Fabrication feasibility.
- Feasible for the Dual-Gate, Tri-Gate and Ω-gate devices.
Multi-Gate SOI MOSFETs (3-D Views)

- **Double Gate/FinFET**
- **Ω-Gate**
- **TriGate**
- **QuadGate**