Final Exam, ECE 137A

Wednesday March 19, 2014 7:30-10:30 PM

Name: ___________________________

Closed Book Exam: Class Crib-Sheet and 3 pages (6 surfaces) of student notes permitted
Do not open this exam until instructed to do so. Use any and all reasonable approximations (5% accuracy), ***after stating & justifying them***.
Show your work:
Full credit will not be given for correct answers if supporting work is missing.

Good luck

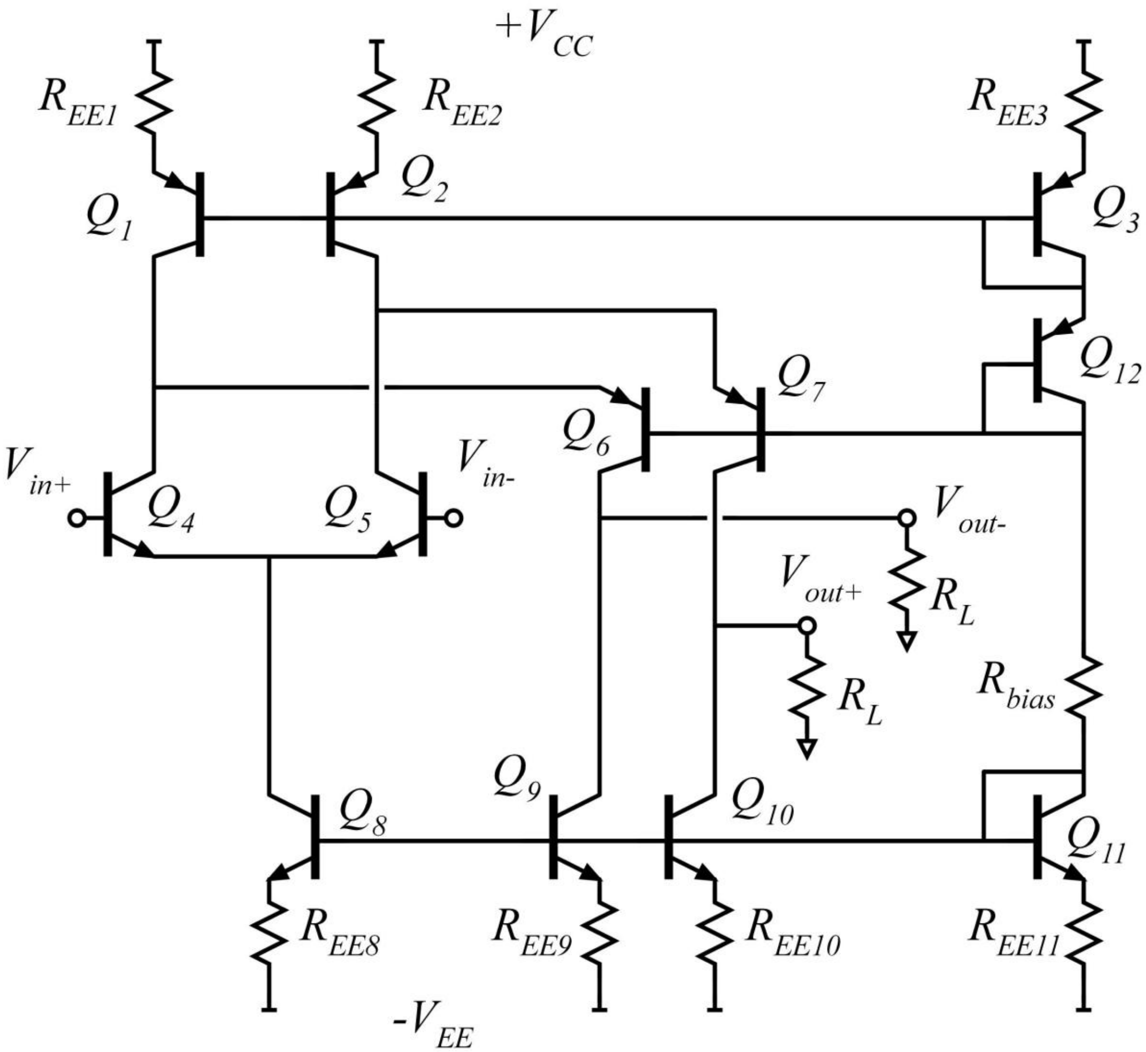
Time function	LaPlace Transform
$\delta(t)$ impulse	1
$U(t)$ unit step-function	$1/s$
$e^{-\alpha t}U(t)$	$\frac{1}{s+\alpha}$
$e^{-\alpha t}\cos(\omega_d t)U(t)$	$\frac{s+\alpha}{(s+\alpha)^2+\omega_d^2}$
$e^{-\alpha t}\sin(\omega_d t)U(t)$	$\frac{\omega_d}{(s+\alpha)^2+\omega_d^2}$

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		5	2c		15
1b		6	2d		10
1c		4	3a		7
1d		10	3b		8
1e		10	3c		7
2a		10	3d		8
2b		10			
total		100			

b

Problem 1, 35 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts



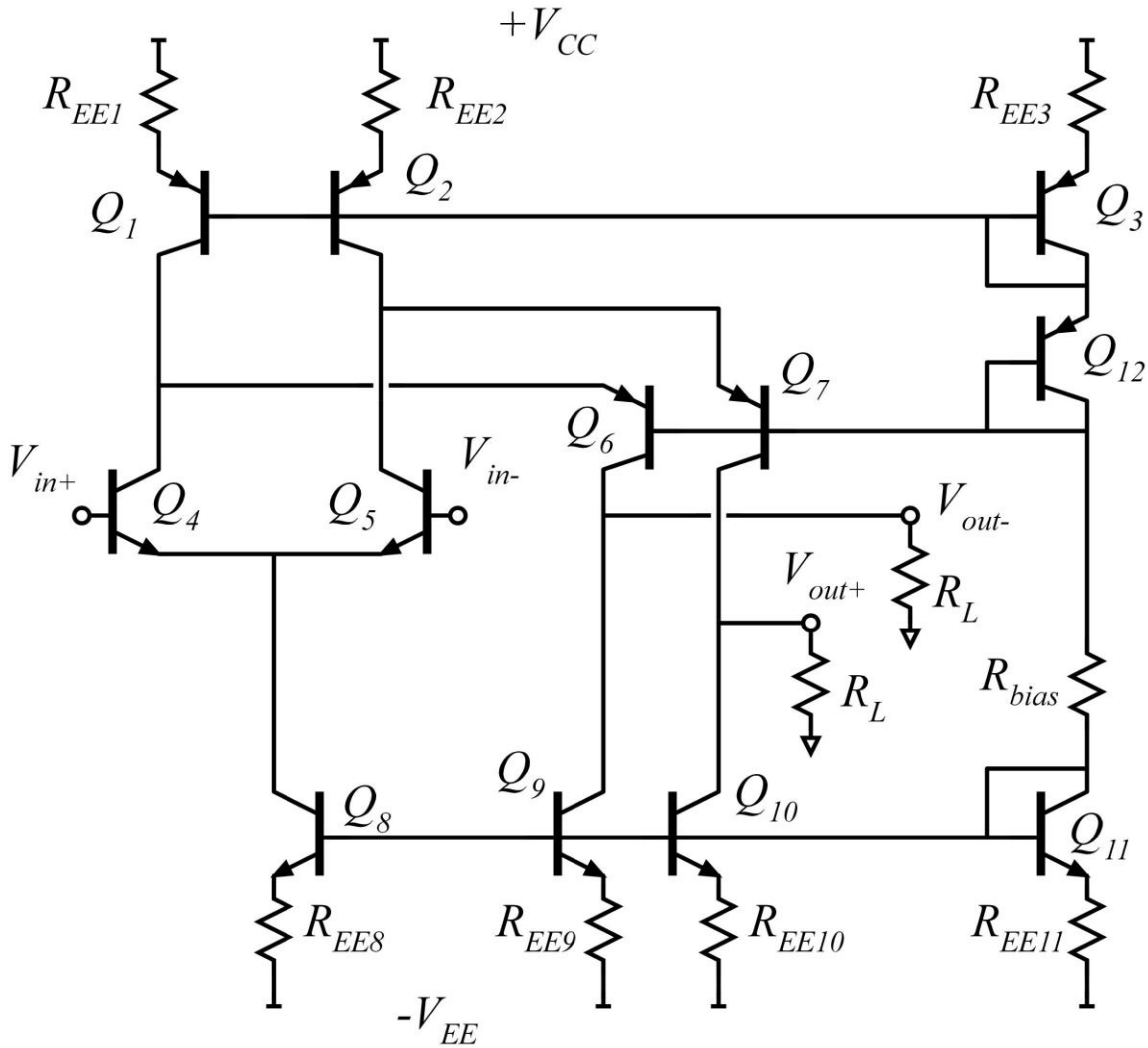
All the transistors have the same (matched) I_S, have $\beta = \infty$, and $V_A = \infty$ Volts. $V_{CE(sat)} = 0.5\text{V}$. V_{be} is roughly 0.7 V, but use $V_{be} = (kT/q)\ln(I_E / I_S)$ when necessary and appropriate. The supplies are +4.5 Volts and -4.5 Volts. The DC voltage drops across Ree3 and Ree11 are both 500mV.

The DC collector currents of Q3,4,5,6,7,11,12 are all 2.0 mA. $R_L = 250\Omega$

b

Part a, 5 points

DC bias:



On the circuit diagram above, label the DC voltages at **ALL nodes**, the DC currents through **ALL resistors,** and the DC drain currents of **all transistors**.

Part b, 6 points
DC bias:

Find the value of all resistors.
Rbias=______ Ree1=______ Ree2=______ Ree3=______
Ree8=______ Ree9=______ Ree10=______ Ree11=______

b

Part c, 4 points

Find the transconductance of the transistors below:
gm4=_____ gm5=_____ gm6=_____ gm7=_____

Part d, 10 points.

The circuit is fully differential. Assuming a differential input signal, $V_{in,diff} = V_{i+} - V_{i-}$, and defining a differential output signal $V_{out,diff} = V_{0+} - V_{0-}$, compute the differential gain $A_d = V_{out,diff} / V_{in,diff}$

$A_d =$______________________

b

Part e, 10 points

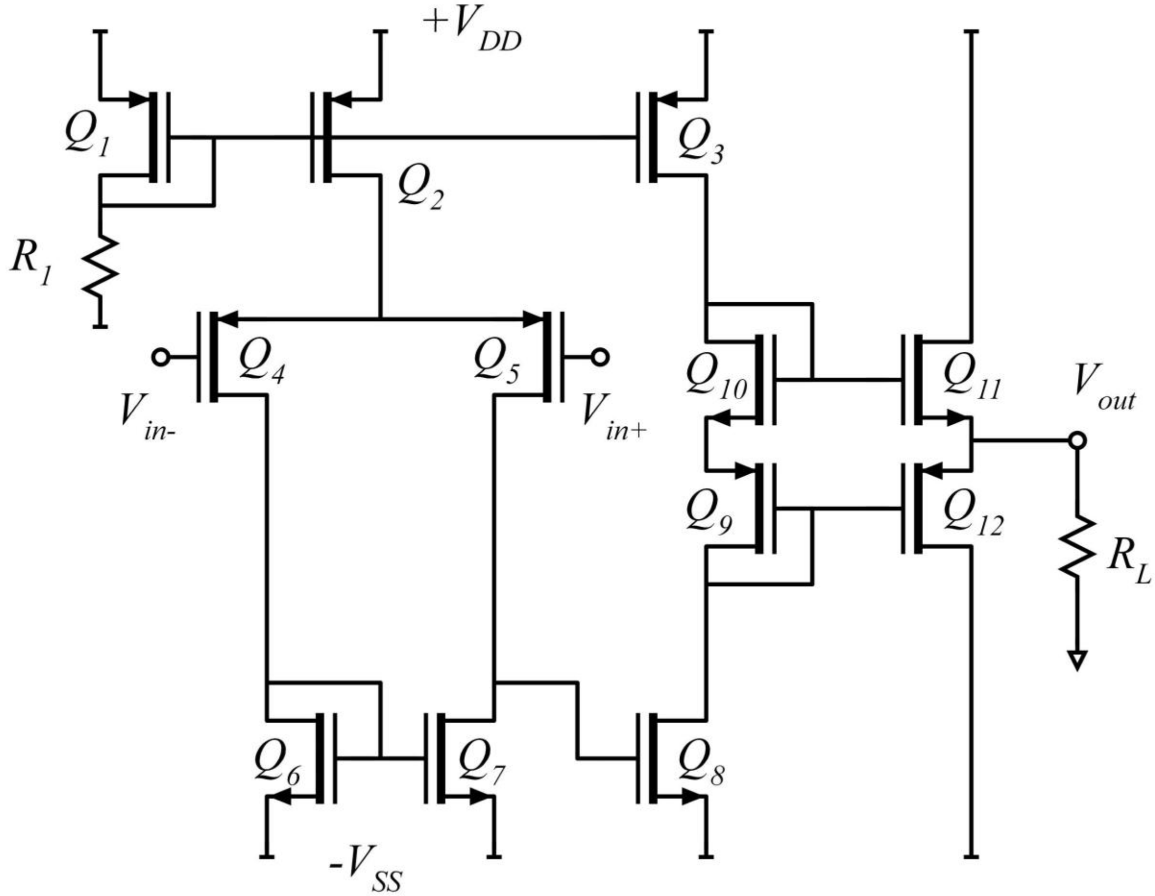
Maximum peak-peak output voltage at the positive output Vo+ (***show all your work***)

	magnitude and sign of maximum output signal swing due to ***cutoff***	magnitude and sign of maximum output signal swing due to ***saturation***
Transistor Q1		
Transistor Q4		
Transistor Q6		
Transistor Q9		

Be warned: In some cases a limit is not relevant at all. Mark those answers "not relevant". But, give a 1-sentence statement below as to why it is not relevant.

Problem 2, 35 points

This is an Op-Amp---analyze the bias under the assumption
that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.



All NMOS: $I_D = 1(\mathrm{mA/V})(W_g/1\mu\mathrm{m})(V_{gs} - V_{th} - \Delta V)(1+\lambda V_{DS})$

$\Delta V = 0.1\mathrm{V}$, $V_{th} = 0.2\mathrm{V}$, $1/\lambda = 5\mathrm{V}$

All PMOS: Also velocity-limited, with $g_m = 0.5(\mathrm{mA/V})(W_g/1\mu\mathrm{m})$

$\Delta V = -0.1\mathrm{V}$, $V_{th} = -0.2\mathrm{V}$, $1/\lambda = 5\mathrm{V}$

V_{DD} =+1 V, $-V_{SS}$ = -1 V, The load resistor is R_L =10 kΩ

b

Part a, 10 points

DC bias.

Approximation: ignore the term $(1+\lambda V_{DS})$ in DC bias analysis.

Analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.

Q1 is to be biased at 0.2 mA drain current.

The transistor gate widths are as follows

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12
2μm	4μm	4μm	2μm	2μm	1μm	1μm	2μm	4μm	2μm	10μm	20μm

Find:

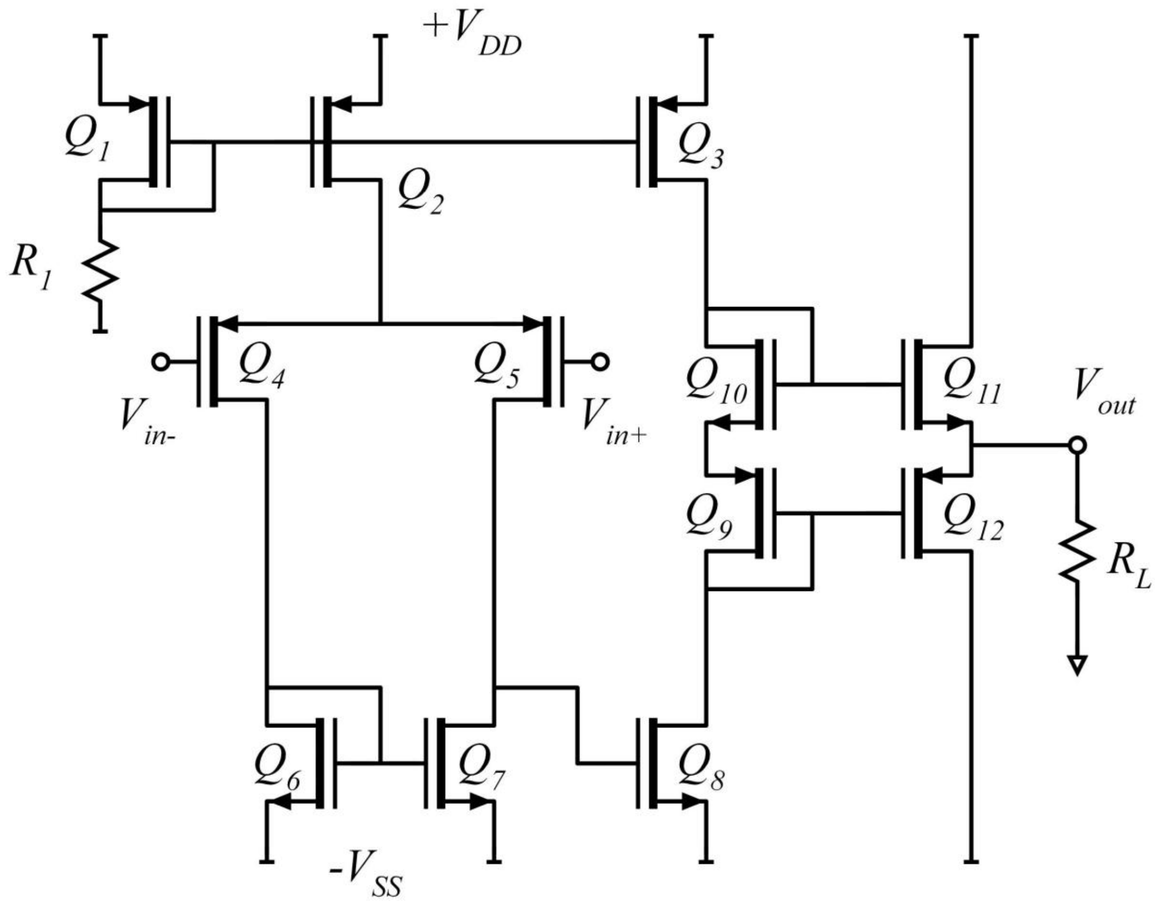
ID1=______ ID2=______ ID3=______ ID4=______ ID5=______ ID6=______

ID7=______ ID8=______ ID9=______ ID10=______ ID11=______ ID12=______

R1=_______

Part b, 10 points

DC bias

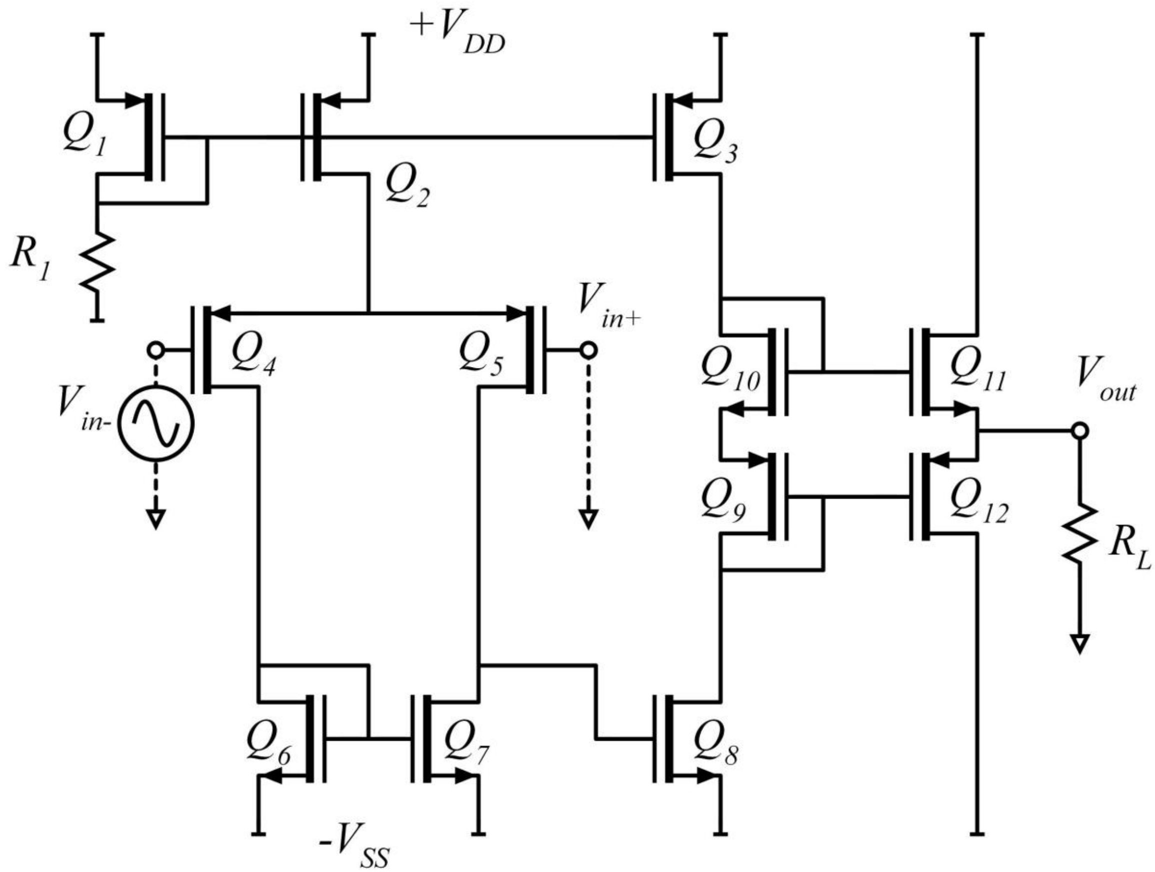


On the circuit diagram above, label the DC voltages at **ALL nodes** and the drain currents of **ALL transistors**

b

Part c, 15 points.

To compute the op-amp differential gain, we will ground the positive input and apply a signal to the negative input. Assume that the DC bias conditions do not change when we do this.



Find the following

	Voltage Gain	Input impedance
Transistor combination Q4,5,6,7		
Transistor Q8		
Transistor combination Q11,12		
Overall differential Vout/Vin		

b

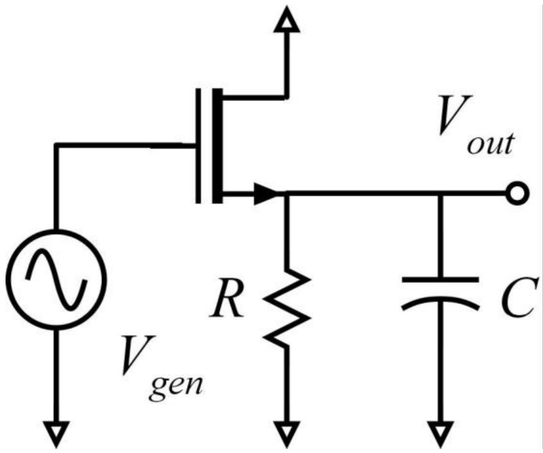
Part d, 10 points

Maximum peak-peak output voltage at the positive output Vo+ (***show all your work***)
Recall that the FETs are velocity-limited, hence $V_{DS,knee} = \Delta V$ =0.1V.

	magnitude and sign of maximum output signal swing due to ***cutoff***	magnitude and sign of maximum output signal swing due to: ***knee voltage*** (saturation)
Transistor Q3		
Transistor Q8		
Transistor Q11		
Transistor Q12		

Be warned: in some cases a limit is not relevant. Mark those answers "not relevant". But, give a 1-sentence statement why below.

Problem 3, 30 points

	You will be working on the circuit to the left Ignore DC bias analysis. You don't need it. The transistor has transconductance gm. Its output resistance Rds is infinity...so you don't need to include this element in the circuit diagram !

Part a, 7 points

Draw a small-signal equivalent circuit of the circuit.

Part b, 8 points

gm=9 mS. C=1 nF. R= 1000 Ohms

Find, by nodal analysis, a small-signal expression for Vout/Vin. Be sure to give the answer with **correct units** and in ratio-of-polynomials form, i.e.

$$\frac{V_{out}(s)}{V_{gen}(s)} = K \cdot \frac{1+b_1 s + b_2 s^2 + \ldots}{1+a_1 s + a_2 s^2 + \ldots} \text{ or (as appropriate) } \frac{V_{out}(s)}{V_{gen}(s)} = K \cdot (s\tau)^n \cdot \frac{1+b_1 s + b_2 s^2 + \ldots}{1+a_1 s + a_2 s^2 + \ldots}$$

Note that an expression like

$$\frac{V_{out}(s)}{V_{gen}(s)} = \frac{1}{1+(3\cdot 10^{-6})s} \text{ is dimensionally wrong; } \frac{1}{1+(3\cdot 10^{-6}\,\text{seconds})s} \text{ is dimensionally correct}$$

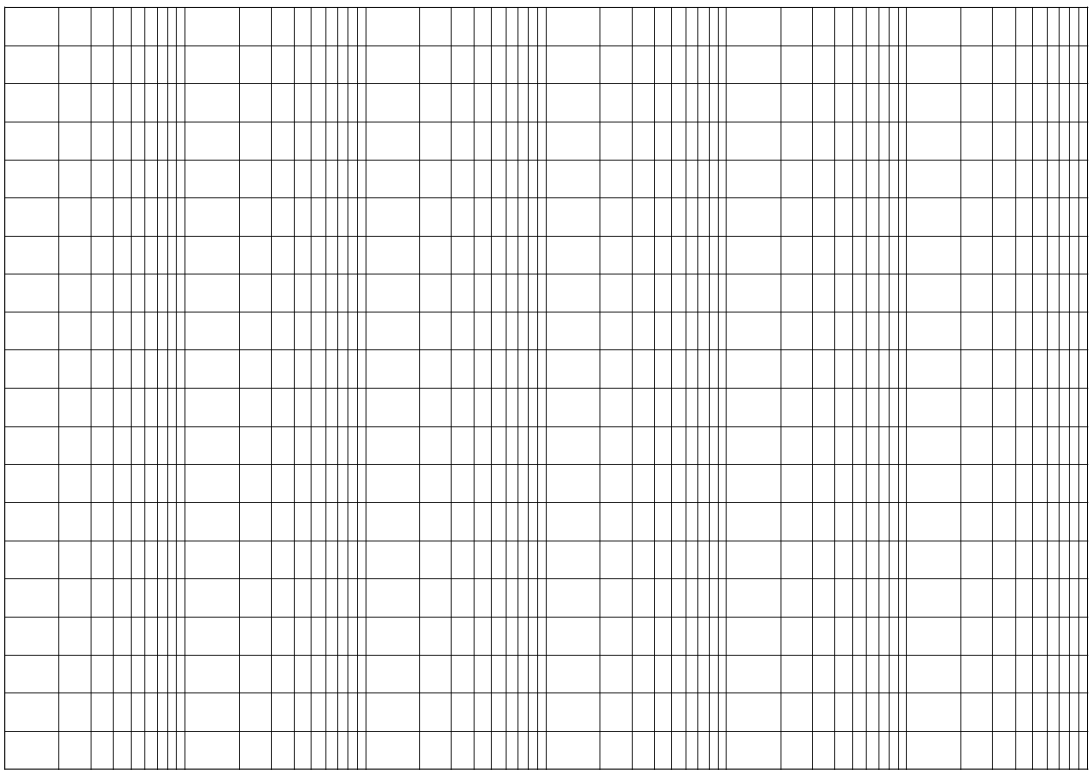
Vout(s)/Vin(s)= ___________________

Part c, 7 points

Find any/all pole and zero frequencies of the transfer function, in Hz:

______________,______________,______________,______________

Draw a clean Bode Plot of Vout/Vin,
LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes



Part d, 8 points

Vin(t) is a 0.2 V amplitude step-function.

Find Vout(t)=___________________________

Plot it below. Label axes, show initial and final values, show time constants.