ECE 137 A Mid-Term Exam

Thursday February 5, 2015

Do not open exam until instructed to.

Closed book: Crib sheet and 1 page personal notes permitted

There are 3 problems on this exam, and you have 75 minutes.

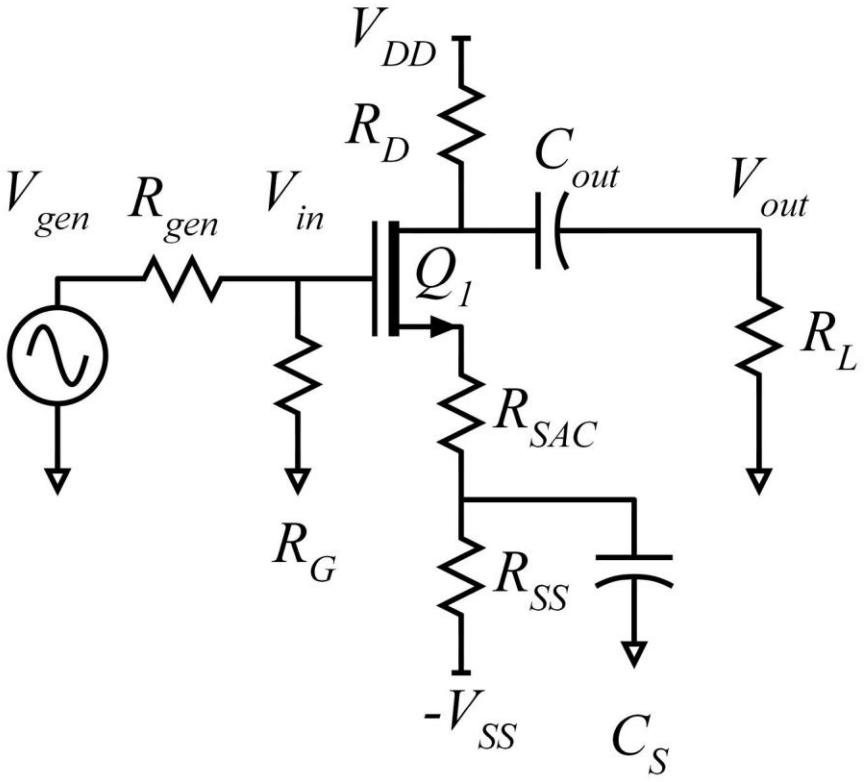
Use any and all reasonable approximations (5% accuracy is fine.) ,
AFTER STATING and approximately Justifying them.

Name: _____

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		10	2f		15
1b		5	3a		8
1c		5	3b		8
1d		10	3c		4
1e		15			
2a		10			
2b		5			
2c		5			
2d		10			
2e		5			
TOTAL					100

Problem 1, 30 points

You will be working on the circuit below:



The transistor has

L_g=45nm, μ=400 $\mathrm{cm^2/V\text{-}s}$, $\varepsilon_{r,ox}$=3.8, T_{ox}=1nm, v_{sat}=10^7cm/s, $V_{th}=0.284V$,

$1/\lambda=10\mathrm{V}$,

From which we calculate:

$c_{ox}v_{sat}$=3.36 mA/V/μm, $\mu c_{ox}/2L_g$=15 $\mathrm{mA/V^2/\mu m}$, $\Delta V=L_g v_{th}/\mu$=0.113V,

The supplies are +1V and -1 V

You are to bias the transistor at 1mA drain current,

with 0.5V DC drain voltage, and with -0.35 V DC source voltage.

$R_{SAC}=10\,\Omega$, R_G=1 MΩ, R_{gen}=100 kΩ, $R_L=10\,\mathrm{k\Omega}$

C_S and C_{out} are very large (AC short-circuit)

Part a, 10 points

DC bias.

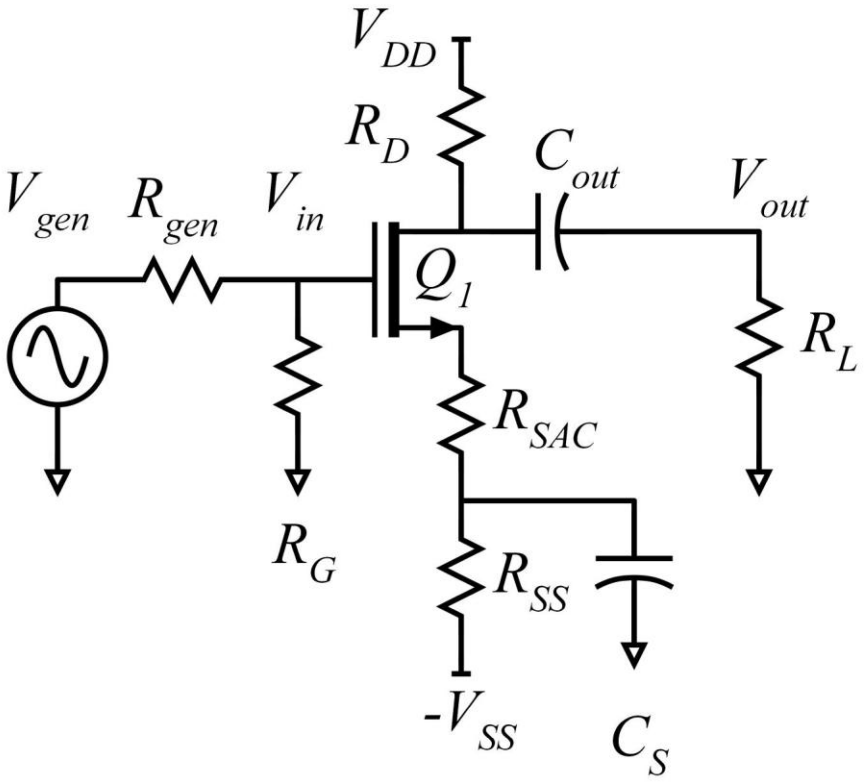
Use this approximation: Ignore (i.e. set to zero) the FET λ parameter in the DC bias calculation.

Find the following:

FET gate width Wg=_____ Rss=_____ RD=_____

Part b, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes** and the DC currents through **ALL resistors**

b

Part c, 5 points

Using the actual (nonzero) FET λ parameter, find the FET small signal parameters
gm=_____ Rds=_____

Part d, 10 points.

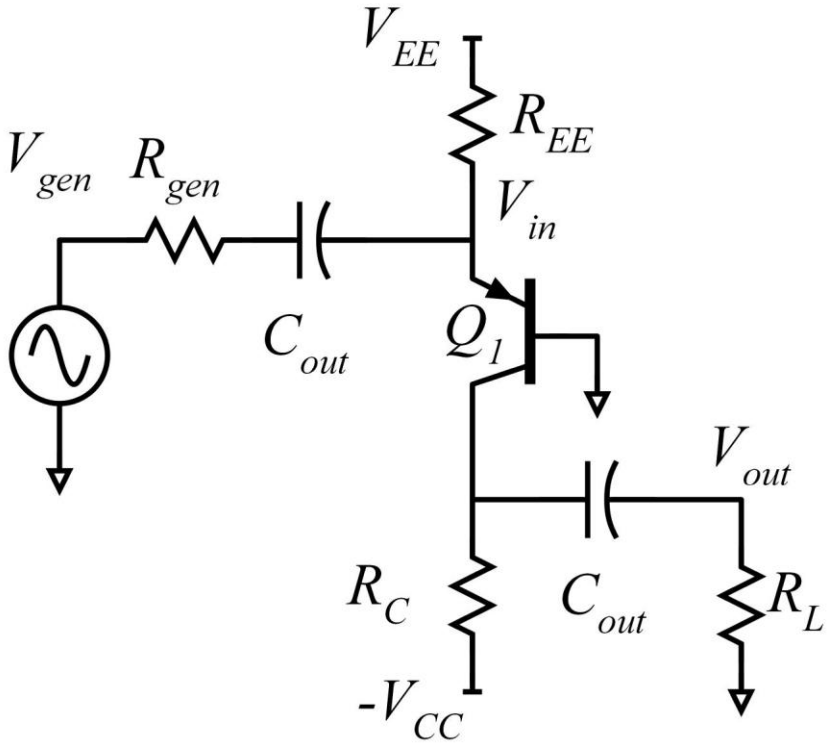
Find the small signal voltage gain Vout/Vin and the amplifier small-signal input resistance.

Vout/Vin=_____

Rin, amplfier = _____

Problem 2, 50 points

You will be working on the circuit below:



Q1: $\beta = 100$, V_A = infinity V
The supplies are +7.5V and -7.5 V.
You will bias the transistor with 1mA collector current.
The DC collector bias voltage is -4V.
R_L is 10 kΩ, R_{gen} is 75 Ω

Part a, 10 points

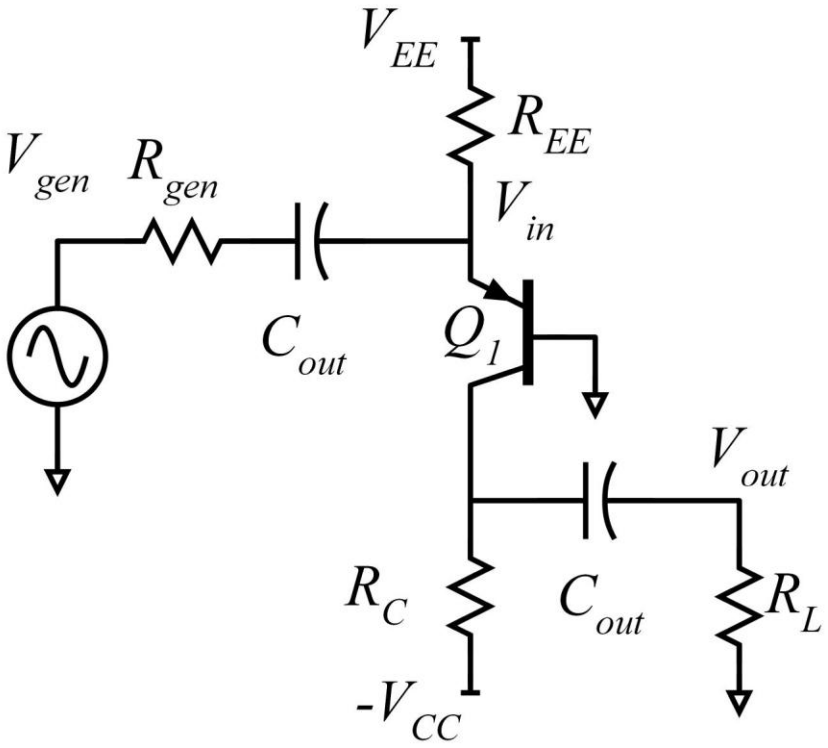
DC bias.

Find the following:

R_{EE} =_____ R_C =_____

Part b, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes** and the DC currents through **ALL resistors**

Part c, 5 points

Find the small signal parameters of Q1.
gm=_____ Rce=_____ Rbe=_____

Part d, 10 points.

Find the small signal voltage gain (Vout/Vin) of Q1 and the amplifier small-signal input resistance.

Vout/Vin=_____

Rin,amp= _____

Part e, 5 points

Find (Vin/Vgen) and (Vout/Vgen)

(Vin/Vgen) = _____

(Vout/Vgen) = _____

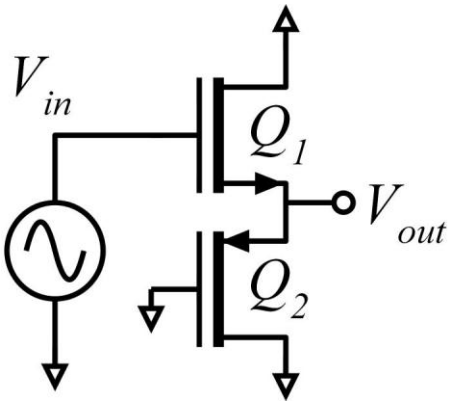
Part f, 15 points

Now you must find the maximum signal swings. Find the output voltage due to saturation and cutoff in Q2. ***Give the sign (+ or -) in your answers below.***

Cutoff of Q1; Maximum ΔVout resulting = _____

Saturation of Q1; Maximum ΔVout resulting = _____

Problem 3, 20 points
nodal analysis



You will be working on the circuit to the left.

Ignore DC bias analysis. You don't need it.

Transistor 1 has transconductance gm1.
Transistor 2 has transconductance gm2.

The drain-source resistances Rds of both transistors are infinity (so you don't need to draw it!)

Part a, 8 points

Draw the small-signal equivalent circuit

Part b, 8 points

Find, by nodal analysis, a small-signal expression for Vout/Vin.

Vout/Vin= _____

Part c, 4 points

gm1= 1 mS gm2= 2 mS
Give a numerical value for Vout/Vin.

Vout/Vin= _____