

## ECE 137 A Mid-Term Exam

Thursday February 5, 2015

Do not open exam until instructed to.

Closed book: Crib sheet and 1 page personal notes permitted

There are 3 problems on this exam, and you have 75 minutes.

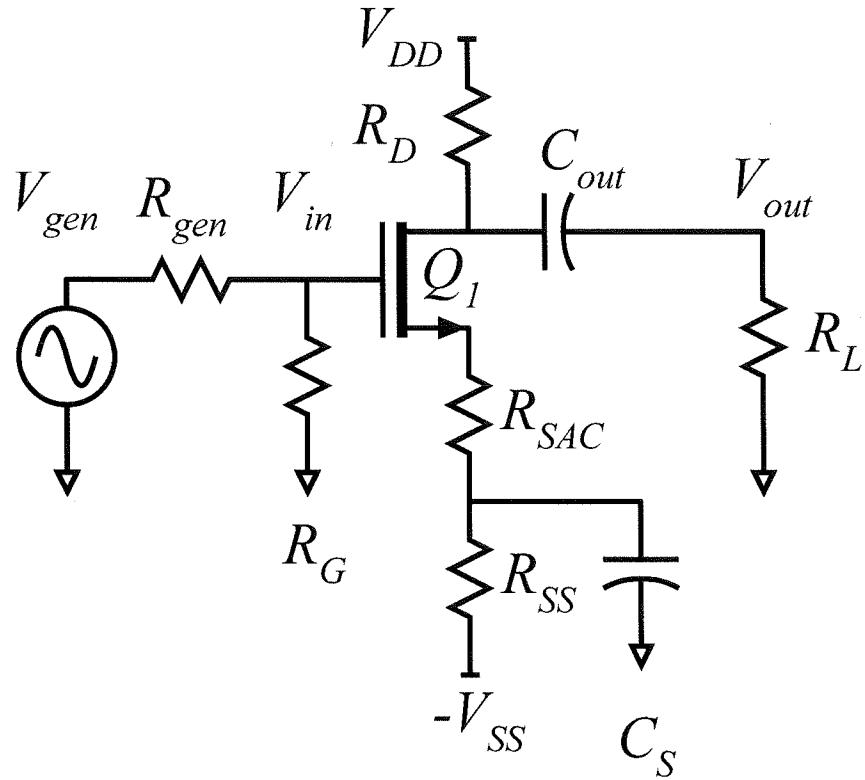
Use any and all reasonable approximations (5% accuracy is fine. ),  
**AFTER STATING and approximately Justifying them.**

Name: Solatich B.

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		10	2f		15
1b		5	3a		8
1c		5	3b		8
1d		10	3c		4
1e		15			
2a		10			
2b		5			
2c		5			
2d		10			
2e		5			
TOTAL					100

### Problem 1, 30 points

You will be working on the circuit below:



The transistor has

$$L_g = 45 \text{ nm}, \quad \mu = 400 \text{ cm}^2/\text{V}\cdot\text{s}, \quad \varepsilon_{r,ox} = 3.8, \quad T_{ox} = 1 \text{ nm}, \quad v_{sat} = 10^7 \text{ cm/s}, \quad V_{th} = 0.284 \text{ V},$$

$$1/\lambda = 10 \text{ V},$$

From which we calculate:

$$c_{ox}v_{sat} = 3.36 \text{ mA/V}/\mu\text{m}, \quad \mu c_{ox} / 2L_g = 15 \text{ mA/V}^2/\mu\text{m}, \quad \Delta V = L_g v_{th} / \mu = 0.113 \text{ V},$$

The supplies are +1V and -1 V

You are to bias the transistor at 1mA drain current,  
with 0.5V DC drain voltage, and with -0.35 V DC source voltage.

$$R_{SAC} = 10 \Omega, \quad R_G = 1 \text{ M}\Omega, \quad R_{gen} = 100 \text{ k}\Omega, \quad R_L = 10 \text{ k}\Omega.$$

$C_S$  and  $C_{out}$  are very large (AC short-circuit)

Part a, 10 points

DC bias.

Use this approximation: Ignore (i.e. set to zero) the FET  $\lambda$  parameter in the DC bias calculation.

Find the following:

FET gate width  $W_g = 15.3 \mu m$      $R_{SS} = 640 \Omega$      $R_D = 500 \Omega$

FET.     $V_g = 0V$  so  $V_{GS} = 0.35V$

1 [note]  $V_{th} + \Delta V = 0.284V + 0.113V = 0.397V$ .

1 [so, we are mobility-limited.]

2 [ $I_D = \frac{15mA}{V^2 \cdot \mu m} \cdot W_g \cdot (V_{GS} - V_{th})^2$ ]  
 $0.35V - 0.284V$

1 [ $\rightarrow W_g = \frac{I_D}{\frac{15mA}{V^2 \cdot \mu m} (V_{GS} - V_{th})^2} = 15.3 \mu m$ ]

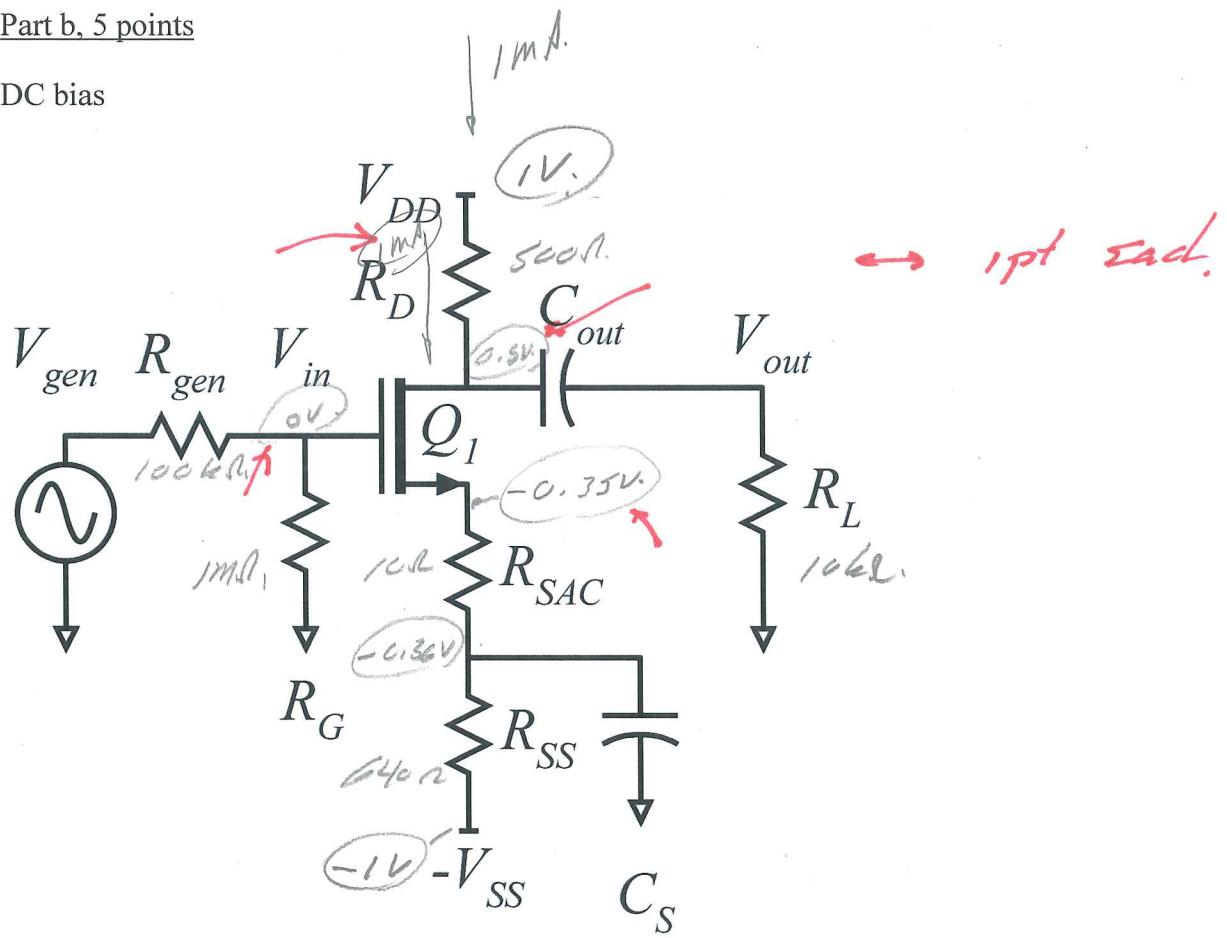
2 [ $R_{SS} + R_{SAC} = \frac{IV - 0.35V}{1mA} = \frac{0.65V}{1mA} = 650 \Omega$ ]

$R_{SS} = 650 \Omega - R_{SAC} = 640 \Omega$

2 [ $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{IV - 0.5V}{1mA} = 500 \Omega$ ]

Part b, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes** and the DC currents through **ALL resistors**

Part c, 5 points

Using the actual (nonzero) FET  $\lambda$  parameter, find the FET small signal parameters  
 $gm = \underline{\hspace{2cm}}$        $R_{ds} = \underline{\hspace{2cm}}$

we are mob. lty-lmted, so

$$\begin{aligned}
 3 \quad g_m &= \frac{wq}{Lg} \mu C_{ox} (V_{gs} - V_{th}) (1 + \lambda V_{ds}) \\
 &= 2 \cdot \frac{15 \text{ mA}}{\text{V}^2 \cdot \mu\text{m}} \cdot 15.3 \mu\text{m} \cdot (0.35\text{V} - 0.284\text{V}) \left(1 + \frac{0.85\text{V}}{10\text{V}}\right) \\
 &= 30 \text{ mS} \cdot (1 + \lambda V_{ds}) = 32.9 \text{ mS} \\
 &\quad \text{ok to omit } (1 + \lambda V_{ds} \text{ term}) \\
 &= 1/30.4 \Omega
 \end{aligned}$$

$$2 \quad R_{ds} = \frac{V_{ds} + 1/\lambda}{I_D} \approx \frac{1}{\lambda I_D} = \frac{10\text{V}}{1\text{mA}} = 10 \text{ k}\Omega$$

Part d, 10 points.

Find the small signal voltage gain  $V_{out}/V_{in}$  and the amplifier small-signal input resistance.

$$V_{out}/V_{in} = \underline{\hspace{10cm}}$$

$$R_{in, \text{amplifier}} = \underline{\hspace{10cm}}$$



$$\begin{aligned} \boxed{2} \quad g_m &= \frac{g_m}{1 + g_m R_{SAC}} = \frac{1}{1/g_m + R_{SAC}} = \frac{1}{30.4\Omega + 10\Omega} \\ &= \frac{1}{40.4\Omega} \end{aligned}$$

$$\boxed{2} \quad R_{DS} = R_{DS}(1 + g_m R_{SAC}) = 10k\Omega \left(1 + \frac{10\Omega}{40.4\Omega}\right) = 12.5k\Omega.$$

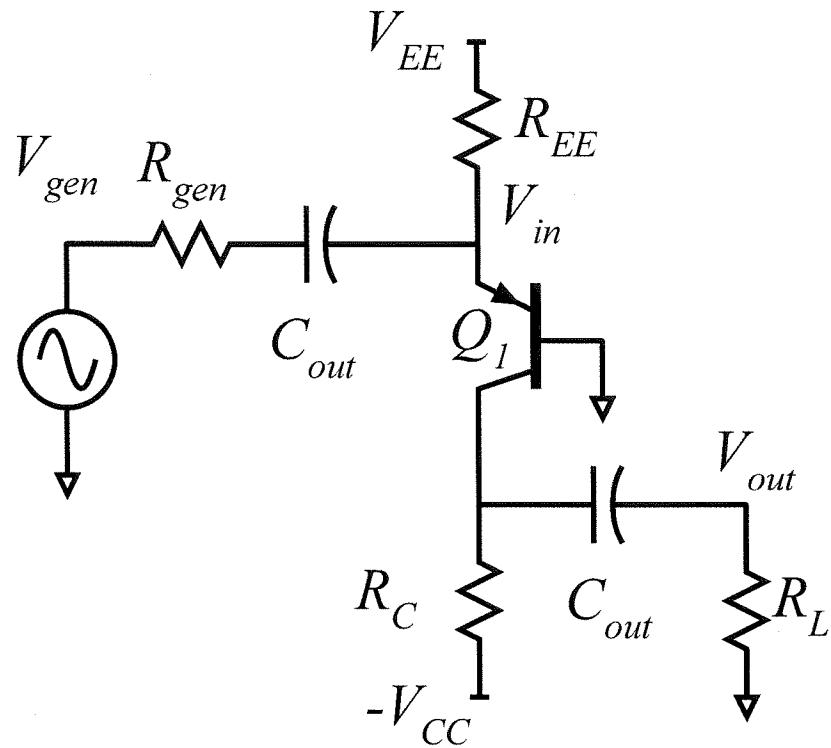
$$\boxed{1} \quad R_{leg} = R_{DS} \parallel R_D \parallel R_L = 12.5k\Omega \parallel 500\Omega \parallel 10k\Omega. \\ = 459\Omega.$$

$$\boxed{2} \quad \frac{V_o}{V_{in}} = -g_m R_{leg} = -\frac{459\Omega}{40.4} = -11.4.$$

$$\boxed{1} \quad R_{in, \text{amp}} = R_g = 1M\Omega.$$

**Problem 2, 50 points**

You will be working on the circuit below:



Q1:  $\beta = 100$ ,  $V_A = \infty$  V

The supplies are +7.5V and -7.5 V.

You will bias the transistor with 1mA collector current.

The DC collector bias voltage is -4V.

$R_L$  is  $10\text{ k}\Omega$ ,  $R_{gen}$  is  $75\ \Omega$

Part a, 10 points

DC bias.

Find the following:

$$R_{EE} = \underline{\hspace{2cm}} \quad R_C = \underline{\hspace{2cm}}$$

5 [

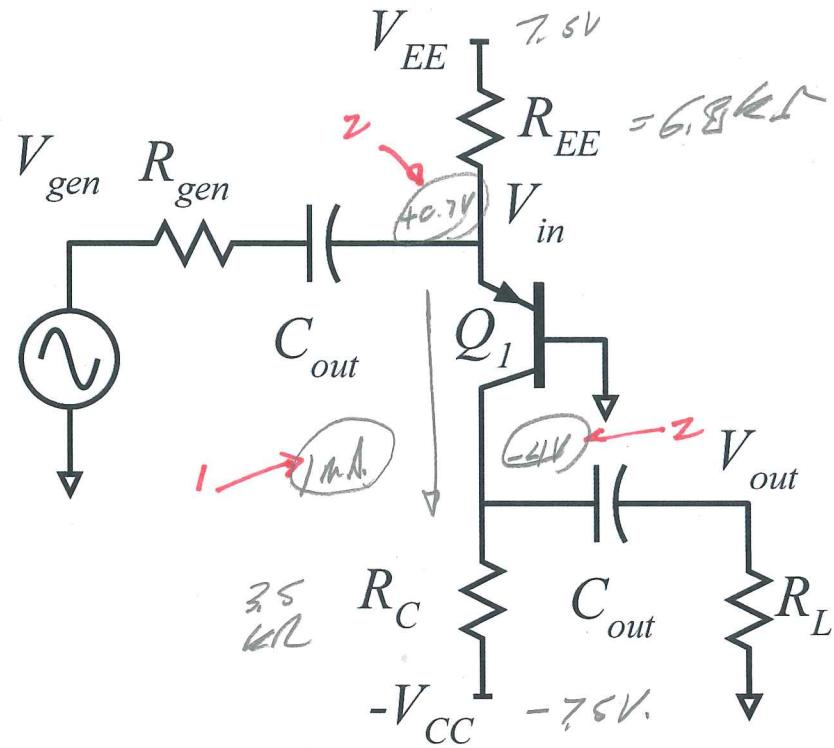
$$R_{EE} = \frac{7.5V - 0.7V}{1mA} = \frac{6.8V}{1mA} = 6.8k\Omega$$

6 [

$$R_C = \frac{3.5V}{1mA} = 3.5k\Omega$$

Part b, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes** and the DC currents through **ALL resistors**

Part c, 5 points

Find the small signal parameters of Q1.

$$gm = \underline{\hspace{2cm}} \quad R_{ce} = \underline{\hspace{2cm}} \quad R_{be} = \underline{\hspace{2cm}}$$

1. 
$$g_m = \frac{1mA}{26mV} = \frac{1}{26\Omega} = 38mS.$$

1. 
$$R_{ce} = \beta/g_m = 100 \cdot 26\Omega = 2.6k\Omega$$

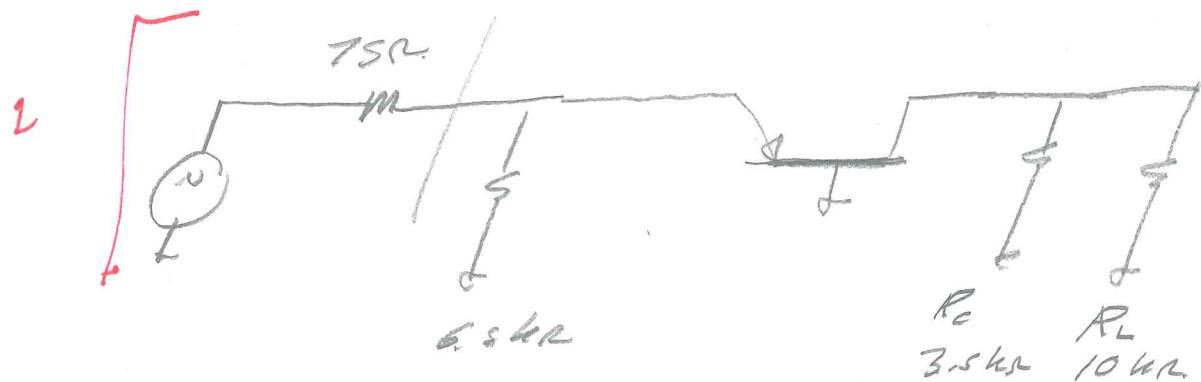
2. 
$$R_{ce} = \frac{v_{ce} + v_s}{I_c} \rightarrow \infty$$

Part d, 10 points.

Find the small signal voltage gain ( $V_{out}/V_{in}$ ) of Q1 and the amplifier small-signal input resistance.

$V_{out}/V_{in} = \underline{\hspace{10cm}}$

$R_{in,amp} = \underline{\hspace{10cm}}$



$$R_{in,amp} = 10k\Omega \parallel 3.5k\Omega = 2.6k\Omega.$$

$$R_{in,amp} = \left( \frac{1}{g_m} + \frac{R_E}{\beta} \right) \left( \frac{R_{CE} + R_{B2}}{R_{CE}} \right) = \frac{1}{g_m} = 26\Omega.$$

$$A_{voltage} = g_m R_{out} = \frac{26\Omega}{26\Omega} = 100.$$

$$R_{in,amp} = R_B + 6.8k\Omega = 26\Omega \parallel 6.8k\Omega \\ = 25.8\Omega \approx 26\Omega.$$

Part e, 5 points

Find  $(V_{in}/V_{gen})$  and  $(V_{out}/V_{gen})$

$$(V_{in}/V_{gen}) = \underline{\hspace{2cm}}$$

$$(V_{out}/V_{gen}) = \underline{\hspace{2cm}}$$

3 [  $\frac{V_{in}}{V_{gen}} = \frac{26\Omega}{26\Omega + 25\Omega} = \frac{26}{101} = 0.257$  ]

2 [  $\frac{V_o}{V_{gen}} = 0.257 \cdot 100 = 25.7$  ]

Part f, 15 points

Now you must find the maximum signal swings. Find the output voltage due to saturation and cutoff in Q2. *Give the sign (+ or -) in your answers below.*

Cutoff of Q1; Maximum  $\Delta V_{out}$  resulting = \_\_\_\_\_

Saturation of Q1; Maximum  $\Delta V_{out}$  resulting = \_\_\_\_\_

cutoff

$$I_{CQ} = 1mA$$
$$I_{CMQ} = 0mA$$
$$\Delta I_C = 1mA \text{ max}$$
$$R_{Eq} = 2.6k\Omega$$
$$\Delta V_{out} = 2.6k\Omega \cdot 1mA = 2.6V, \text{ negative}$$

4.

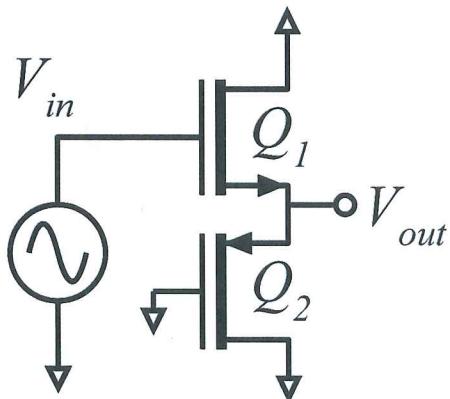
Saturation:

$$3 [V_{CE,Q} = 4.7V]$$

$$3 [V_{CE,mi} - V_{CE,sat} \approx 1.2V]$$

$$1 [ \Delta V_{out} = 4.2V, \text{ positive}]$$

**Problem 3, 20 points**  
*nodal analysis*



You will be working on the circuit to the left.

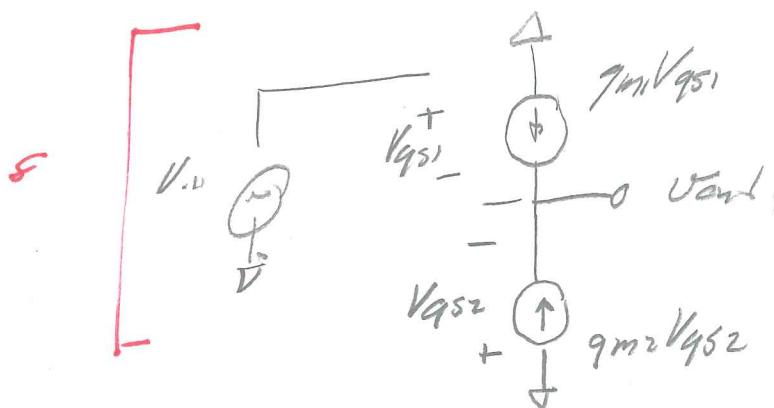
Ignore DC bias analysis. You don't need it.

Transistor 1 has transconductance  $gm_1$ .  
 Transistor 2 has transconductance  $gm_2$ .

The drain-source resistances  $R_{ds}$  of both transistors are infinity (so you don't need to draw it!)

Part a, 8 points

Draw the small-signal equivalent circuit



take off points \* if controlling voltages  
 not shown

\* 3 points for each ~~the~~ controlling control voltage

Part b, 8 points

Find, by nodal analysis, a small-signal expression for  $V_{out}/V_{in}$ .

$V_{out}/V_{in} = \underline{\hspace{2cm}}$

4 [  $\sum I = 0 @ V_{out}$

$$g_{m1}V_{gs1} + g_{m2}V_{gs2} = 0$$

$$\text{but } V_{gs1} = V_{in} - V_{out}$$

$$V_{gs2} = -V_{out}$$

$$g_{m1}(V_{in} - V_{out}) + g_{m2}(-V_{out}) = 0.$$

$$g_{m1} \cdot V_{in} = (g_{m1} + g_{m2})V_{out}$$

4. [  $\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{m2}}$

Part c, 4 points

$$gm_1 = 1 \text{ mS} \quad gm_2 = 2 \text{ mS}$$

Give a numerical value for  $V_{out}/V_{in}$ .

$$V_{out}/V_{in} = \underline{\hspace{2cm}}$$

$$4. \left[ \frac{v_o}{v_{in}} \right] = \frac{g_{m1}}{g_{m1} + g_{m2}} = \frac{1}{3}$$