# Final Exam, ECE 137A

# Wednesday March 22, 2017, 7:30 - 10:30pm

Name: \_\_\_\_\_

Closed Book Exam:

Class Crib-Sheet and 3 pages (6 surfaces) of student notes permitted Do not open this exam until instructed to do so. Use any and all reasonable approximations (5% accuracy), *after stating & justifying them*.

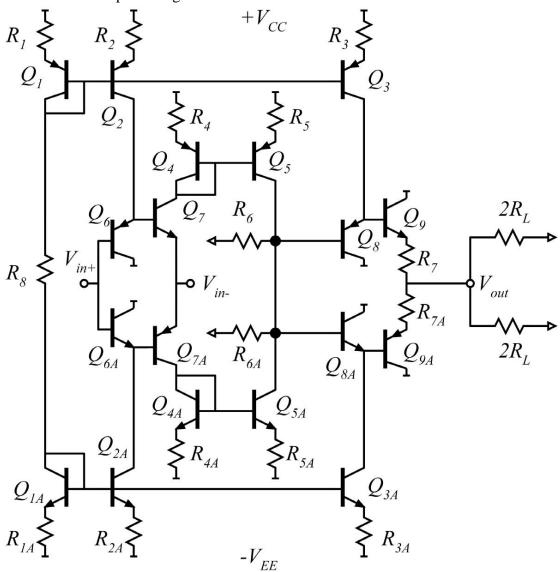
Show your work: Full credit will not be given for correct answers if supporting work is missing. Good luck

Time function	LaPlace Transform
$\delta(t)$ impulse	1
U(t) unit step-function	1/s
$e^{-ct}U(t)$	$\frac{1}{s+\alpha}$
$e^{-\alpha t}\cos(\omega_d t)U(t)$	$\frac{s+\alpha}{\left(s+\alpha\right)^2+\omega_d^2}$
$e^{-\alpha t}\sin(\omega_d t)U(t)$	$\frac{\omega_d}{\left(s+\alpha\right)^2+\omega_d^2}$

Part	Points	Points	Part	Points	Points
	Received	Possible		Received	Possible
1a		5	2c		15
1b		6	2d		10
1c		4	3a		7
1d		10	3b		8
1e		10	3c		7
2a		10	3d		8
2b		10			
total		100			

#### Problem 1, 35 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts



All the transistors have the same (matched)  $I_s$ , have  $\beta = 100$ , and  $V_A = \infty$  Volts.

$$V_{CE(sat)} = 0.5 \mathrm{V}.$$

 $V_{be}$  is roughly 0.7 V, but use  $V_{be} = (kT/q)\ln(I_E/I_S)$  when necessary and appropriate.

The supplies are +3 Volts and -3 Volts.

R1=R1A, R2=R2A, R3=R3A, R6=R6A, R7=R7A.

The voltage drops across R1 and R1A are both 300mV.

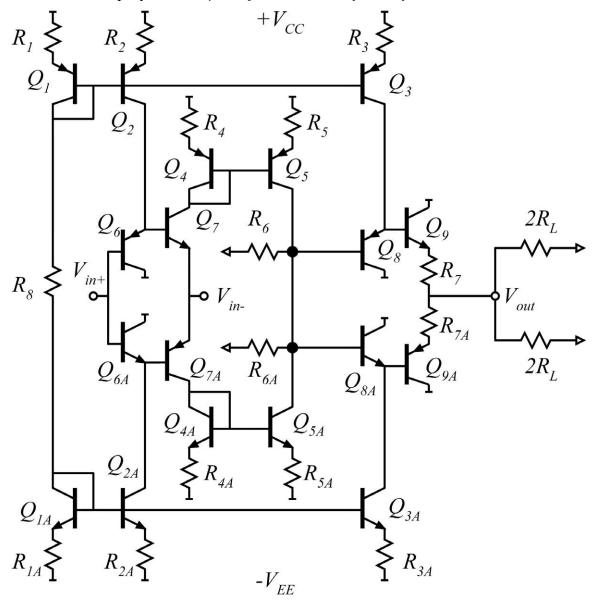
Q1, Q1A, Q6, Q6A, Q7, Q7A, Q5, Q5A, Q8, Q8A : *I*<sub>C</sub> =1mA.

Q9, Q9A: *I*<sub>C</sub> =0.5 mA.

RL=100 Ohms, R6=R6A=1000 Ohms. R4= R4A=R5=R5A=0 Ohms.

Part a, 5 points

DC bias---to simplify ,assume  $\beta = \infty$  for the DC analysis only.



On the circuit diagram above, label the DC voltages at **ALL nodes**, the DC currents through **ALL resistors**, and the DC collector currents of **all transistors**.

Part b, 6 points DC bias:

Find the value of all resistors.

R1/R1A=	_ R2/R2A =	_ R3/R3A =	_ R4/R4A =
R5/R5A =	R6/R6A =	R7/R7A =	R8 =

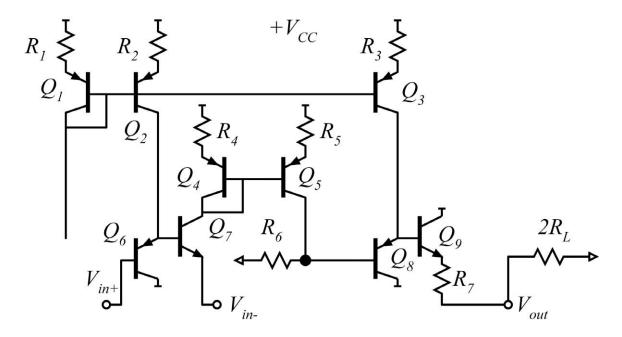
# Part c, 4 points

## find the following

device	Q1/1A	2/2A	3/3A	4/4a	5/5A	6/6A	7/7A	8/8A	9/9A
gm, S									
Rce, $\Omega$									

#### Part d, 10 points.

The circuit is 100% symmetric, and can be represented by the simpler small-signal diagram below;



Find the following, using the actual value of  $\beta$ , i.e.  $\beta = 100$ 

	Voltage Gain	Input impedance
Q9		
Q8		
Q5		
Q7		
Q6		
Overall differential		
Vout/Vin		

Note: with some insight, you can find the combined gain of Q7/Q4/Q5 in a single step. If would would like to do so, omit the separate answers for Q5 and Q7 in the table above, and instead fill in the table below,

	Voltage Gain	Input impedance
Q7/Q4/Q5 combination.		

#### Part e, 10 points

## Maximum peak-peak output voltage (*show all your work*)

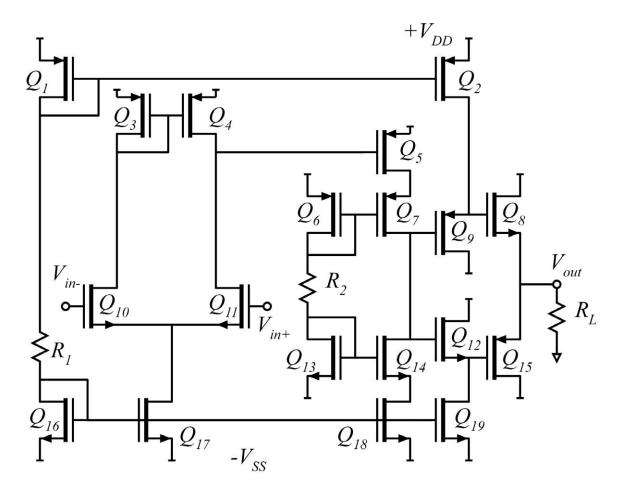
For this, you must use the full circuit diagram, not the half circuit diagram.

	magnitude and sign of	magnitude and sign of
	maximum output signal	maximum output signal
	swing due to <i>cutoff</i>	swing due to <i>saturation</i>
Transistor Q9		
Transistor Q9A		
Transistor Q8		
Transistor Q8A		
Transistor Q5		
Transistor Q5A		
Transistor Q7		
Transistor Q7A		

Be warned: In some cases a limit is not relevant at all. Mark those answers "not relevant". But, give a 1-sentence statement below as to why it is not relevant. Q9/9A form a push pull stage, so be careful about your answer there. *Hint*: There is, effectively, another push-pull stage in the circuit, which will affect two of the other answers.

#### Problem 2, 35 points

*This is an Op-Amp*---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.



The NMOSFETs and the PMOSFETS have a 0.20 V threshold, a 22nm gate length, 200 cm<sup>2</sup>/Vs mobility, a 10<sup>7</sup> cm/s injection velocity, and 1/ $\lambda$  =6 Volts. The gate oxide thickness is 1.0nm and the dielectric constant is 3.8. This gives  $\mu c_{ox} W_g / 2L_g = 15.3 \text{ mA/V}^2 \cdot (W_g / 1\mu \text{m})$  and  $v_{sat} c_{ox} W_g = 3.36 \text{ mA/V} \cdot (W_g / 1\mu \text{m})$  (both are a bit unrealistic for a real technology). and  $v_{sat} L_g / \mu = 0.110 \text{ V}$  $V_{DD} = +1.5 \text{ V}, -V_{SS} = -1.5 \text{ V}, R_L = 20 \text{ kOhm}$  Part a, 10 points DC bias.

#### Approximation: ignore the term $(1 + \lambda V_{DS})$ in DC bias analysis.

Analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.

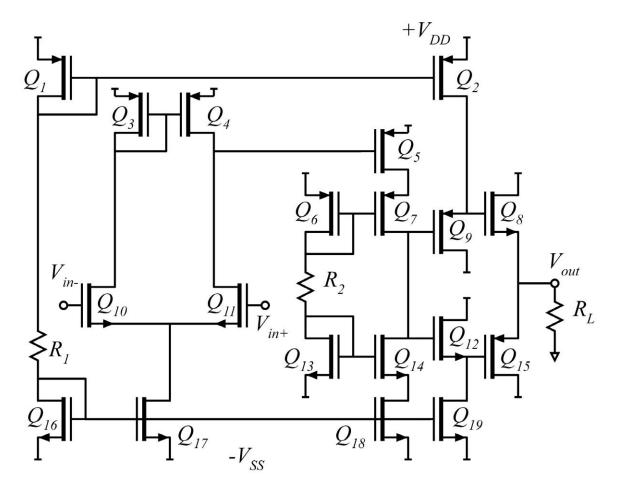
All transisistors *except Q6, Q13* have  $|V_{gs}|=0.3$ V. Q6 and Q13 have Vgs=0.35V. All transisistors *except Q8, Q15, Q17* have  $|I_D|=0.156$ mA. Q8 and Q15 have  $|I_D|=1.56$ mA. You can figure out  $|I_D|$  for Q17.

Find the gate widths of all transistors, plus R1 and R2.

Find:			
Wg1=	Wg2 =	Wg3=	_ Wg4 =
Wg5=	Wg6 =	Wg7=	_ Wg8 =
Wg9=	Wg10=	Wg11=	Wg12 =
Wg13=	Wg14 =	Wg15=	Wg16=
Wg17=	Wg18=	Wg19	
R1=	_R1=		

### Part b, 10 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes**, the drain currents of **ALL transistors**, and the gate widths of **ALL transistors** 

### Part c, 15 points.

You will now compute the op-amp differential gain. You must consider the  $(1 + \lambda V_{DS})$  term in the FET IV characteristics when you do this.

#### Find the following

	Voltage Gain	Input impedance
Transistor combination		
Q3,4,10,11		
Q5,7		
Q9 or Q12.		
Q8 or Q15		
Overall differential		
Vout/Vin		

Notes:

1) You can analye Q5 and Q7 as separate stages, or as a combined stage using Norton/Thevenin methods. Don't ask for hints as to how to do this.

2) For Q9/12 and for Q8/15, you can assume that Q9 and Q12 are on for the positive signal swing and Q8 and Q15 are on for the negative signal swing. More accurately, you can assume, for the signal swing near zero volts, that all are on. If you take the latter approach (and do it correctly), you will receive a couple of extra credit points. One hint (don't ask for any other hints): use symmetry.

b

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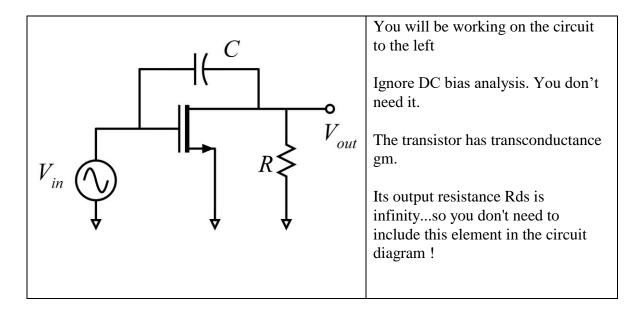
## Part d, 10 points

### Maximum peak-peak output voltage at the positive output Vo+ (*show all your work*)

	magnitude and sign of	magnitude and sign of
	maximum output signal	maximum output signal
	swing due to <i>cutoff</i>	swing due to:
		<i>knee voltage</i> (saturation)
Transistor Q8		
Transistor Q15		
Transistor Q9		
Transistor Q12		
Transistor Q2		
Transistor Q19		
Transistor Q7		
Transistor Q14		

Be warned: in some cases a limit is not relevant. Mark those answers "not relevant"...

### Problem 3, 30 points



### Part a, 7 points

Draw a small-signal equivalent circuit of the circuit.

#### Part b, 8 points

### gm=10 mS. C=1 nF. R= 1000 Ohms

Find, by nodal analysis, a small-signal expression for Vout/Vin. Be sure to give the answer with \*\*correct units\*\* and in ratio-of-polynomials form, i.e.

$$\frac{V_{out}(s)}{V_{gen}(s)} = K \cdot \frac{1 + b_1 s + b_2 s^2 + \dots}{1 + a_1 s + a_2 s^2 + \dots} \text{ or (as appropriat e)} \frac{V_{out}(s)}{V_{gen}(s)} = K \cdot (s\tau)^n \cdot \frac{1 + b_1 s + b_2 s^2 + \dots}{1 + a_1 s + a_2 s^2 + \dots}$$

Note that an expression like

 $\frac{V_{out}(s)}{V_{gen}(s)} = \frac{1}{1 + (3 \cdot 10^{-6})s}$  is dimensionally wrong;  $\frac{1}{1 + (3 \cdot 10^{-6} \text{ seconds })s}$  is dimensionally correct

Vout(s)/Vin(s)=\_\_\_\_\_

Part c, 7 points

\_\_\_\_\_

Find any/all pole and zero frequencies of the transfer function, in Hz:

Draw a clean Bode Plot of Vout/Vin, LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes

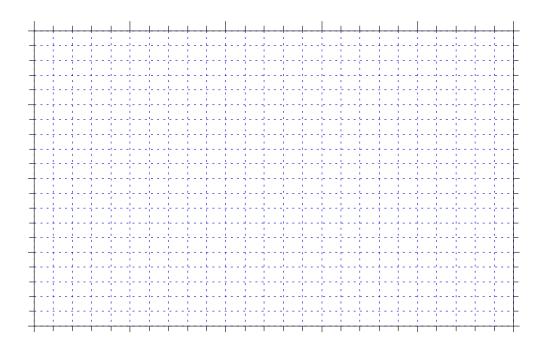
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Part d, 8 points

Vin(t) is a 0.1 V amplitude step-function.

Find Vout(t)=\_\_\_\_\_

Plot it below. Label axes, show initial and final values, show time constants.



b

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