Final Exam, ECE 137A

Thursday March 17, 12 - 3 p.m.

Name: ___________________________

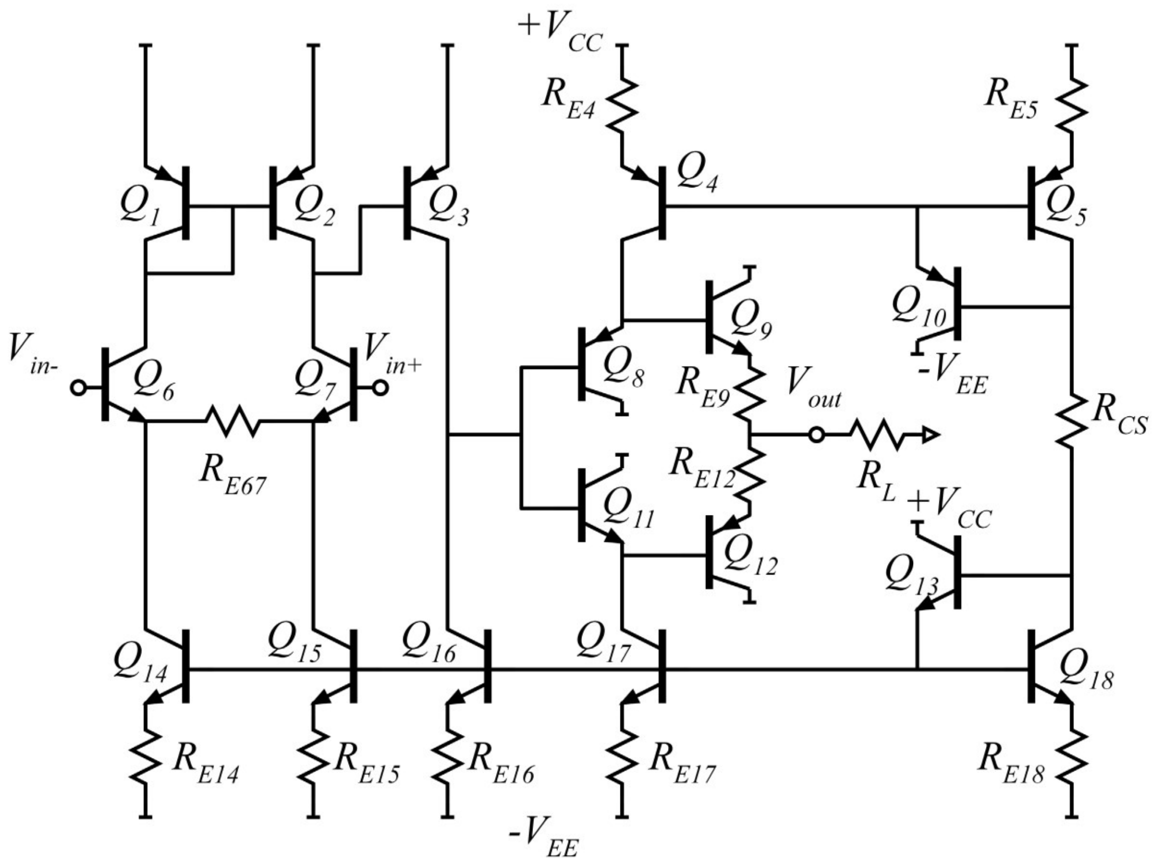
Closed Book Exam:
Class Crib-Sheet and 4 pages (4 surfaces) of student notes permitted
Do not open this exam until instructed to do so. Use any and all reasonable approximations (5% accuracy), ***after stating & justifying them***.
Show your work:
Full credit will not be given for correct answers if supporting work is missing.
Good luck

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		6	2c		10
1b		5	2d		10
1c		4	3a		10
1d		10	3b		10
1e		10	3c		10
2a		10			
2b		5			
total		100			

b

Problem 1, 35 points

This is an Op-Amp---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.



All the transistors have the same (matched) I_S, have $\beta = 100$, and $V_A =$ *infinity* Volts . $V_{CE(sat)} = 0.5\text{V}$. V_{be} is approximately 0.7 V, but use $V_{be} = (kT/q)\ln(I_E / I_S)$ when necessary or appropriate. The supplies are +3 Volts and -3 Volts.

All transistors have the same I_S .

The resistors RE5 and RE18 have a 300mV DC voltage drop acoss them.

Re67=100 Ohms, RL=1000 Ohms.

DC bias currents: Ic6=Ic7=Ic9=Ic12=Ic18=0.1 mA. Ic3=Ic8=Ic11=0.2mA

Part a, 6 points

DC bias---to simplify ,assume $\beta = \infty$ ***for the DC analysis only.***

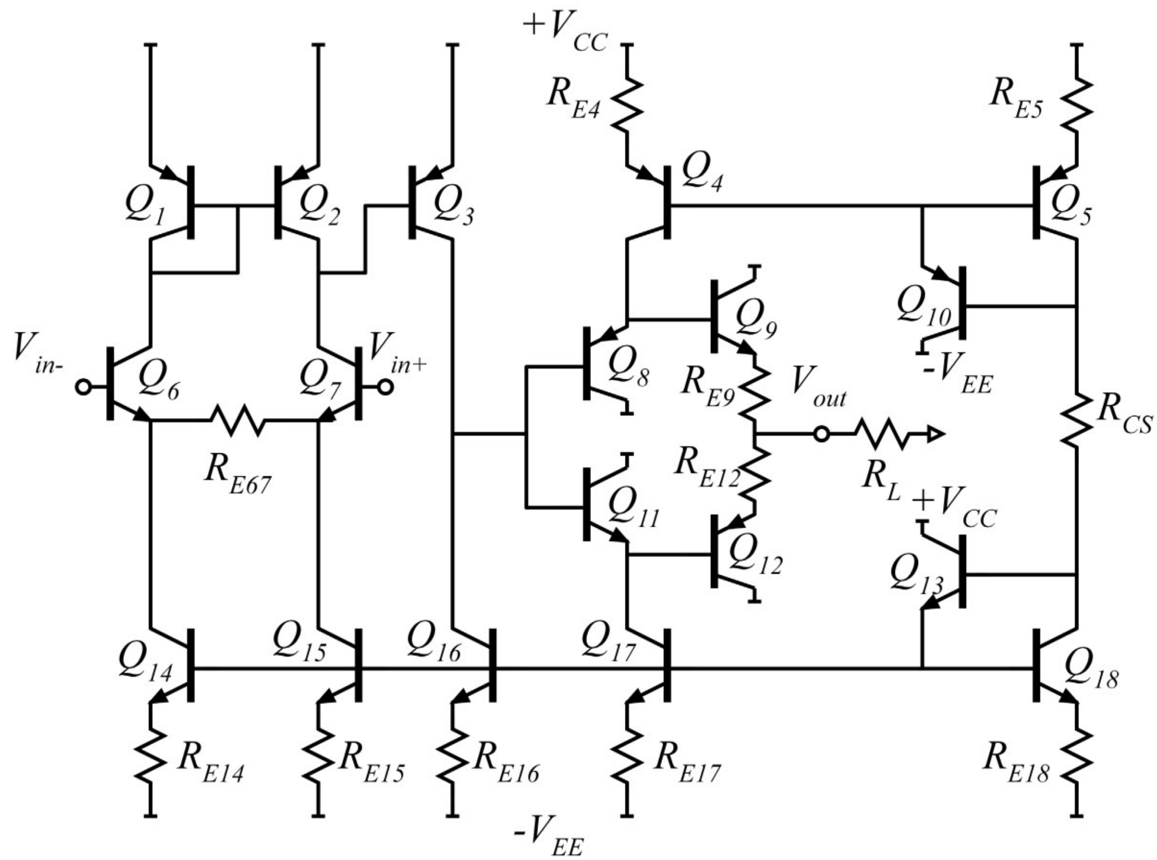
Analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.

(Hint, this should give Vi- = 0V)

Find the value of the following resistors:

Re4=________, Re5=________, Re9=________, Re12=________, Re14=________,
Re15=_______, Re16=_______, Re17=_______, Re18=________, Rcs=________,

Part b, 5 points



On the circuit diagram above, label the DC voltages at **ALL nodes**, and the DC collector currents of **all transistors**. Label the values of all resistors.

b

Part c, 4 points

find the following

device	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
gm, mS								

device	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16
gm, mS		don't bother*			don't bother*			

device	Q17	Q18
gm, mS		

*don't bother calculating these

b

Part d, 10 points.

Find the following, ***using the actual value of*** β***, i.e.*** β***=100***

	Voltage Gain	Input impedance
Q9 or Q12		
Q8 or Q11		
Q3		
Q1,2,6,7 combination.		
Overall differential Vout/Vin		

Part e, 10 points

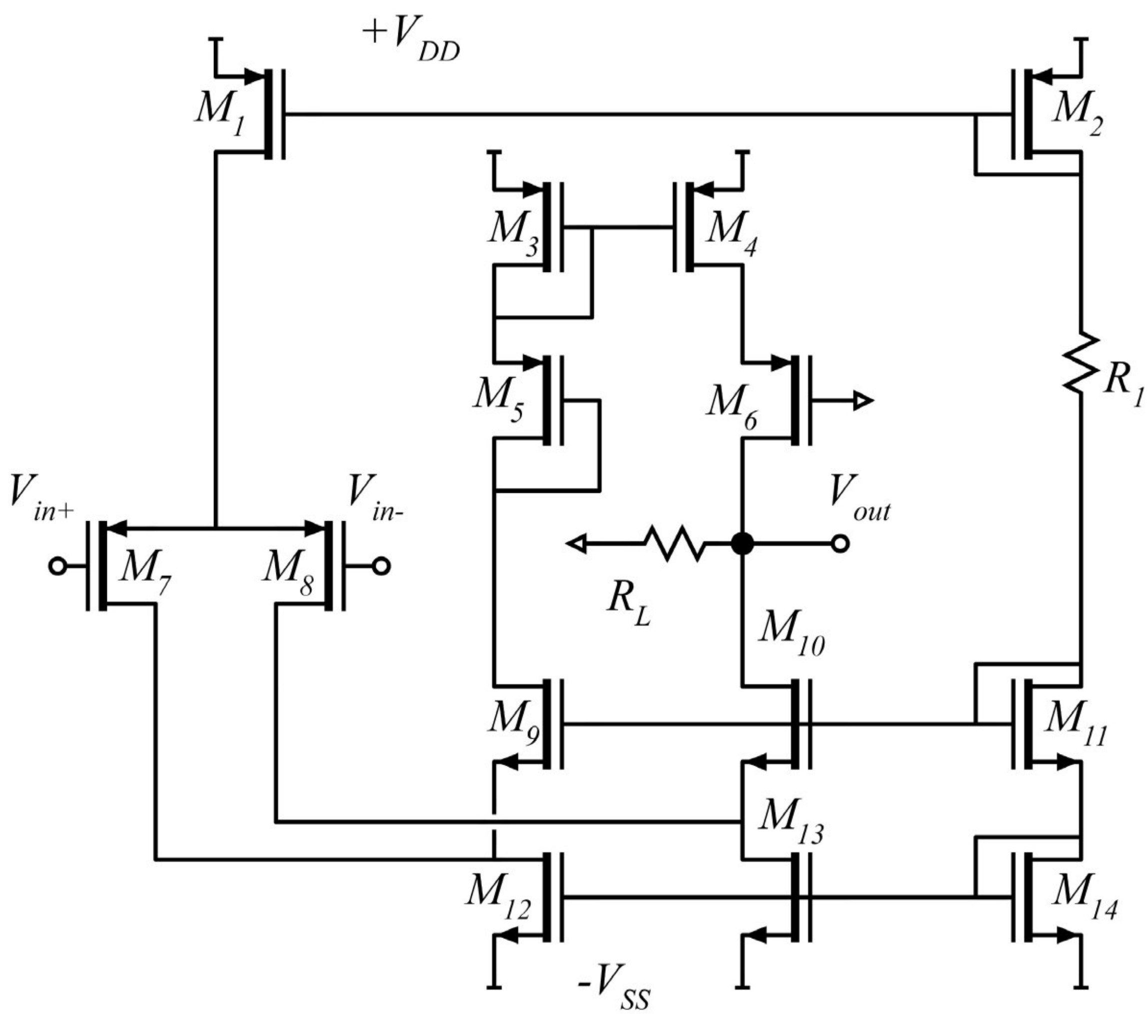
Maximum peak-peak output voltage (***show all your work***)
For this, you must use the full circuit diagram, not the half circuit diagram.

	magnitude and sign of maximum output signal swing due to ***cutoff***	magnitude and sign of maximum output signal swing due to ***saturation***
Transistor Q9		
Transistor Q12		
Transistor Q8		
Transistor Q11		
Transistor Q4		
Transistor Q17		

Be warned: In some cases a limit is not relevant at all. Mark those answers "not relevant". But, give a 1-sentence statement below as to why it is not relevant. Q9/12 form a push pull stage, so be careful about your answer there. .

Problem 2, 35 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts



The NMOSFETs have $K_\mu = \mu c_{gs} W_g / 2L_g = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$

$K_v = c_{gs} v_{inj} W_g = 2.0\text{mA/V} \cdot (W_g / 1\mu\text{m})$, $\Delta V = v_{inj} L_g / \mu = 0.10\text{V}$, $V_{th} = 0.3\text{V}$,

$1/\lambda = 5\text{V}$

The PMOS have identical parameters, except, of course, V_{th} is negative.

V_{DD} = +0.8 V, $-V_{SS}$ = -0.8 V, R_L=10kOhm

All transistors have $|V_{gs}|$=0.4V

M7,8 are biased at I_D=50 µA.

M5,6,9,10,11 are biased at I_D=200 µA

b

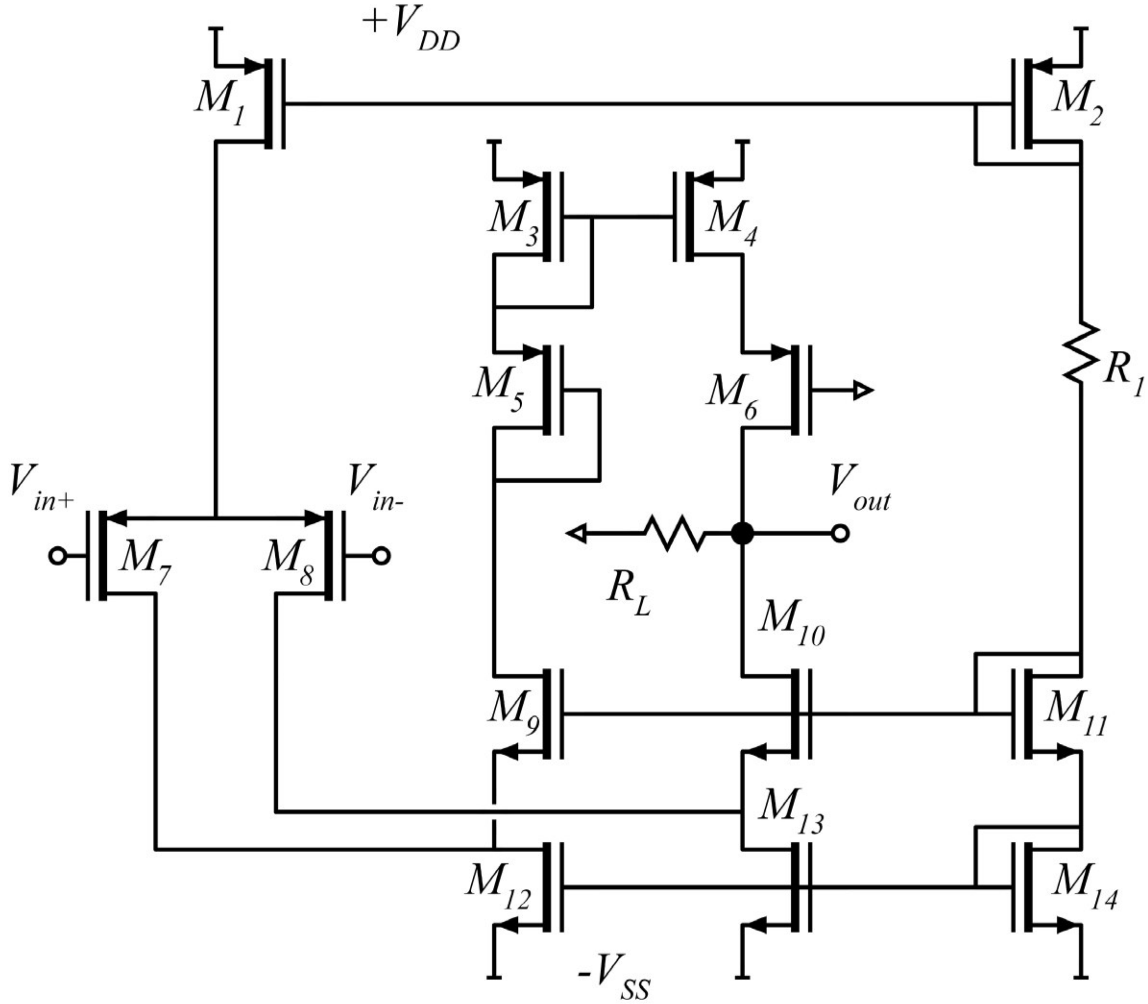
Part a, 10 points
DC bias.

Find the Gate widths, in μm, of
M1____________, M7________

Note that, by using the mobility-limited formula $g_m = 2I_D / (V_{gs} - V_{th})$, we can solve the exam without calculating any of the FET widths. ***So, there's no reason to spend time calculating other FET widths.***

Part b, 5 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes,** the drain currents of **ALL transistors**

Part c, 10 points.
This amplifier has *two* signal paths between input and output.
One is the path (M7 and M8, M9, M3, M4, M6, output).
The other is the path (M7 and M8, M10, output).

You will now compute the differential gain for the path (M7 and M8, M10, output).

Find the following

	Voltage Gain	Input impedance
Transistor M10		
M7-M8 differential pair		
Overall differential Vout/Vin for this path		

b

Part d, 10 points

This amplifier has *two* signal paths between input and output.
One is the path (M7 and M8, M9, M3, M4, M6, output).
The other is the path (M7 and M8, M10, output).

You will now compute the differential gain for the path (M7 and M8, M9, M3, M4, M6, output). Find the following

	Voltage Gain	Input impedance
Transistor M6		
Transistor M4		
Transistor M9		
M7-M8 differential pair		
Overall differential Vout/Vin for this path		

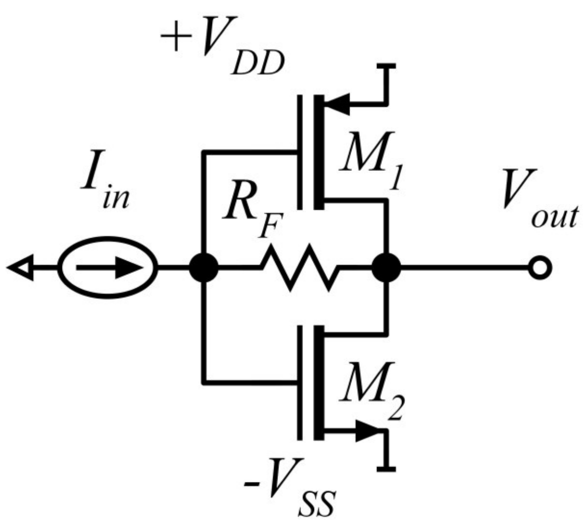
(the overall amplifier gain is the sum of the answers for parts c and d, but you are not asked to calculate this.

b

Problem 3, 30 points

Nodal analysis: optical receiver preamplifier as real-world example.

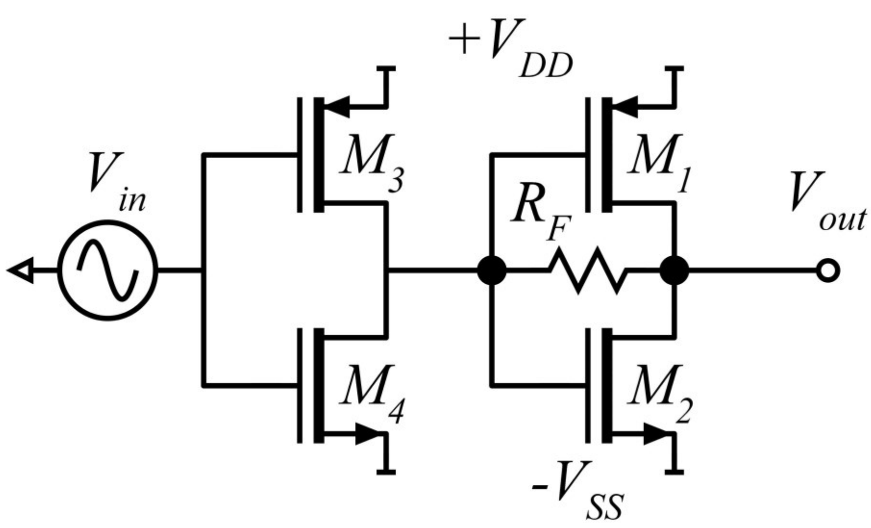
Part a, 10 points

 	You will be working on the circuit to the left Ignore DC bias analysis. You don’t need it. The NFET and the PFET each have transconductance gm. The NFET and the PFET each have output resistance Rds of infinity...so you don't need to include this element in the circuit diagram ! gm=0.5 mS Rf=11 kOhm

Compute, from nodal analysis, the small-signal gain Vout/Iin. This is called a transimpedance gain.

Vout/Iin = __________________

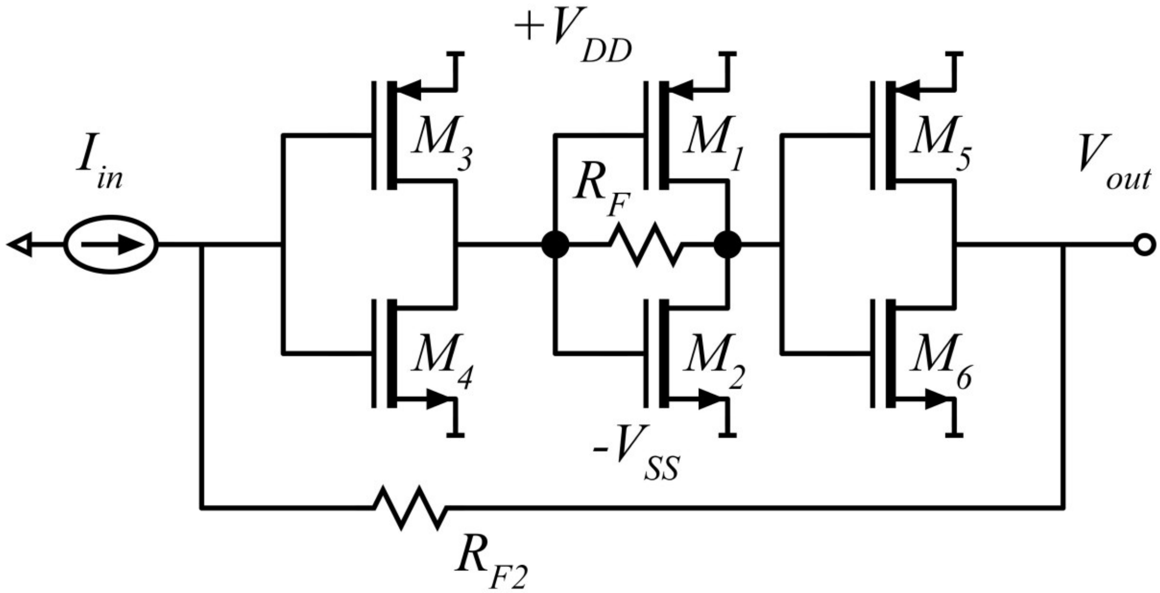
Part b, 10 points

	The NFETs and the PFETs all have transconductance gm. The NFETs and the PFETs have have output resistance Rds of infinity gm=0.5 mS Rf=11 kOhm

Compute, from nodal analysis, the small-signal gain Vout/Vin. This is a voltage gain.
Hint: you can save some work by using the result from part A.

Vout/Vin = _________________

Part c, 10 points



The NFETs and the PFETs all have transconductance gm. The NFETs and the PFETs have have output resistance Rds of infinity.
gm=0.5 mS, Rf=11 kOhm, Rf2=1 kOhm.

Compute, from nodal analysis, the small-signal gain Vout/Iin. This is a transimpedance gain. Hint: you can save a great deal of work by using the results from parts A and B.

Vout/Iin = _________________